MICROROC
A MICROMEGAS Readout Chip

RD51 mini-week
CERN
13-15 June 2012

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FRANCE

13 june 2012

Outline

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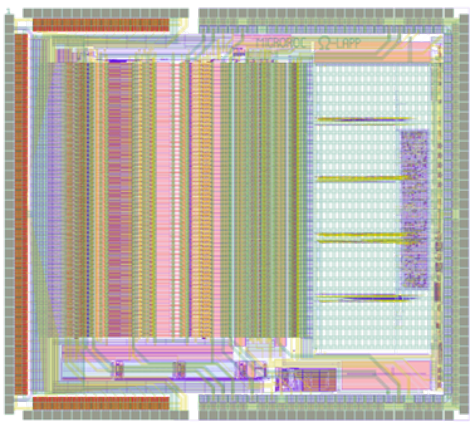
Introduction

MICROROC is a 64 channels integrated circuit packaged in TQFP160 intended to be used with MPGD-based DHCAL (MICROMEGAS or GEM).

- MICROROC is the fruit of the collaboration between LAPP and LAL/OMEGA based on the experience of previous ASICs (DIRAC and HARDROC) and on multiple test beam results
- Same Digital part as HARDROC2b, but charge preamplifier input stage + sparks protection [R. Gaglione] and slower shaping + 4-bit DAC offset correction per channel [N. Seguin]
- MICROROC is pin a pin compatible with the HARDROC2b to minimize boards modifications.



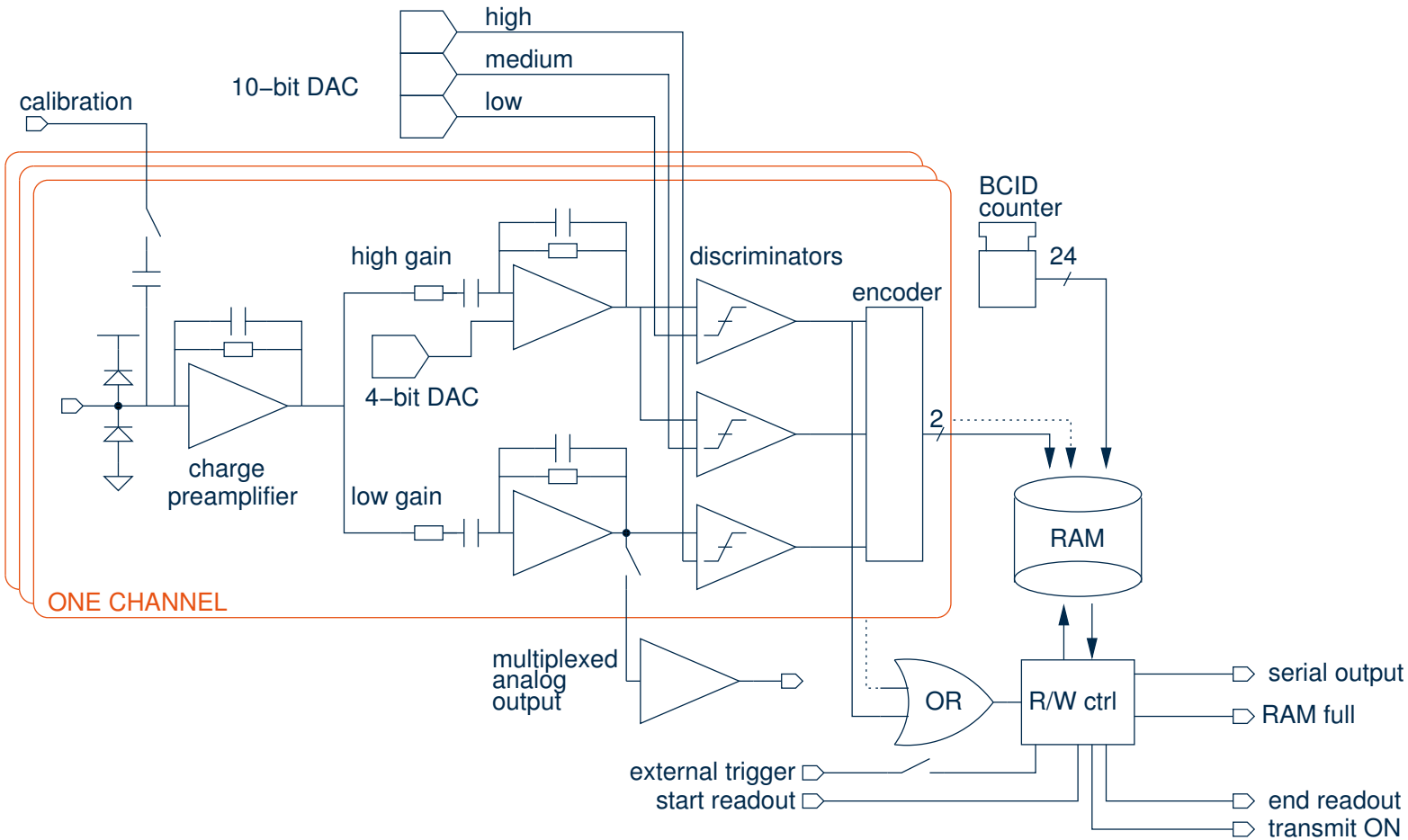
Functioning

MICROROC operation is tight by ILC beam structure requirements, and divided into two main phases.

- During the first phase the beam is on: each channel collect detector signal and compare the charge to the three defined thresholds, then the result is stored inside digital memory if at least one channel as a charge bigger than lowest threshold (auto-trigger mode).
- During the second phase (beam off), the analog part is powered down, and a serial daisy-chained readout is performed.

For beam test operation, an external trigger is available, as well as an analog multiplexed readout for fine detector characterisation.

Global architecture



Different kinds of fast triggers are available.

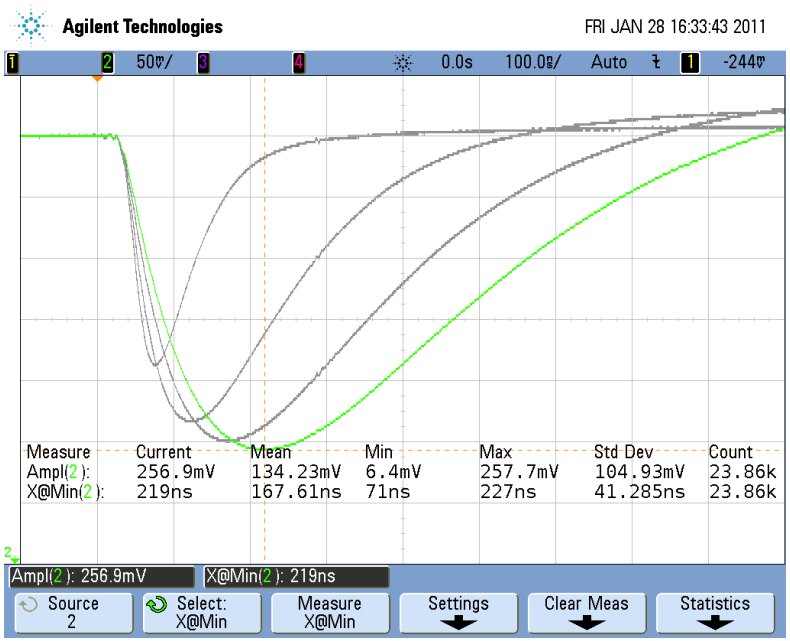
Characteristics and performances summary

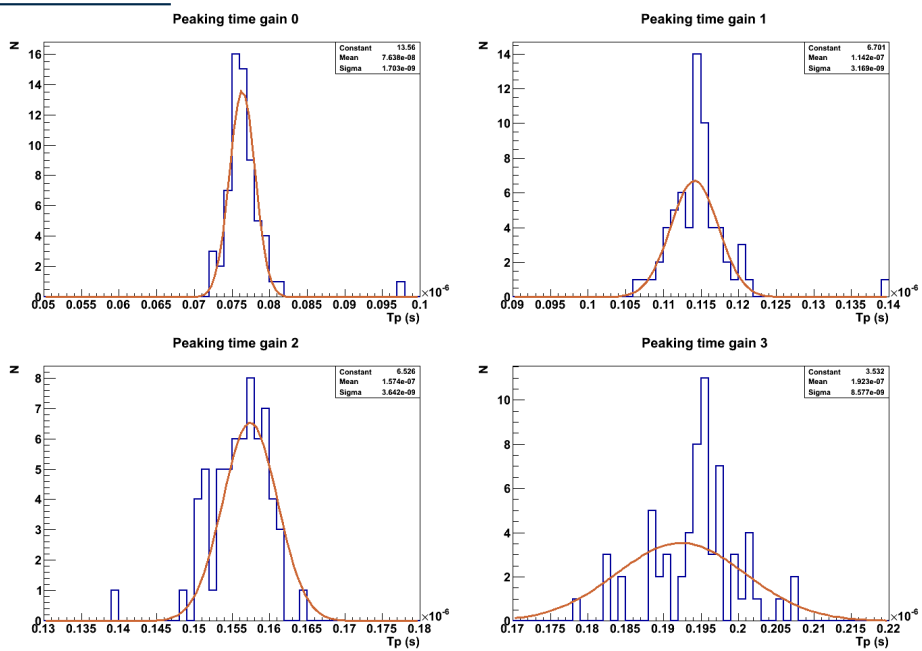
- Technology: AustriaMicroSystem SiGe 0.35 µm
- Die size: 4.85×4.3 mm ($\sim$21 mm^2)
- Dynamic range: 500 fC
- Preamplifier gain: 2.38 mV/fC
- High gain shaper: 12 mV/fC
- Low gain shaper: 2.87 mV/fC
- Peaking times: 30, 50, 100 and 200 ns
- C_{det}: 80 pF (now: C_{det}=60 pF)
- Noise rms: 1 fC at preamplifier output, 0.24 fC with 200 ns shaping (@C_{det}: 80 pF)
- Minimum threshold: $\sim$1 fC (MIP Landau MPV @ $\sim$20 fC)
- Power consumption: 68 mA@3.5 V$\rightarrow$240 mW
- Memory: 127 events (64 channels + 24bits BCID@200 ns)

Outline

Shapers

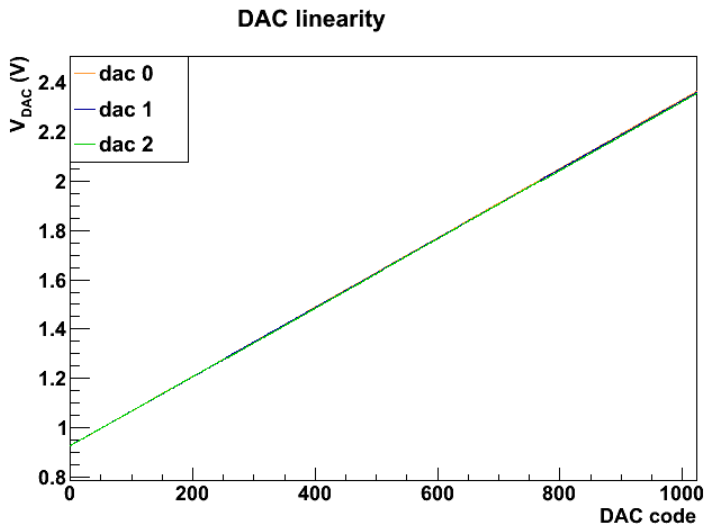
Setting	Measure Gain (mV/fC)	Measure Tp (ns)	Simulation Gain (mV/fC)	Simulation Tp (ns)
00	7.6	76.3	10.5	30
01	9.7	114.2	11.0	100
10	9.8	157.4	11.1	150
11	10.2	192.3	11.2	200

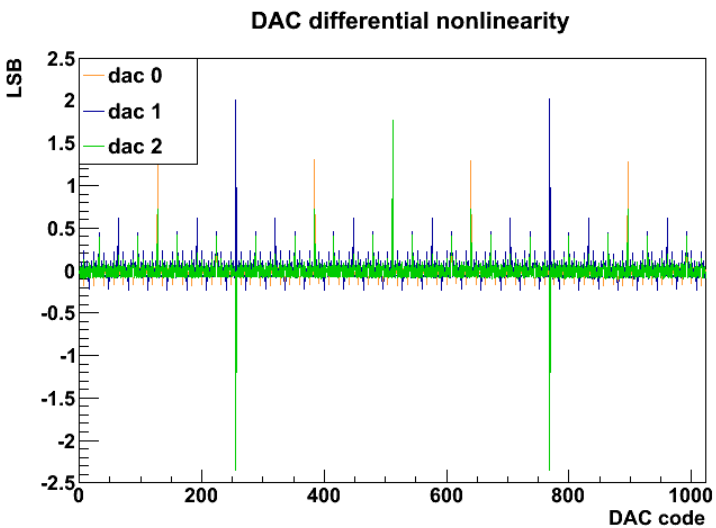


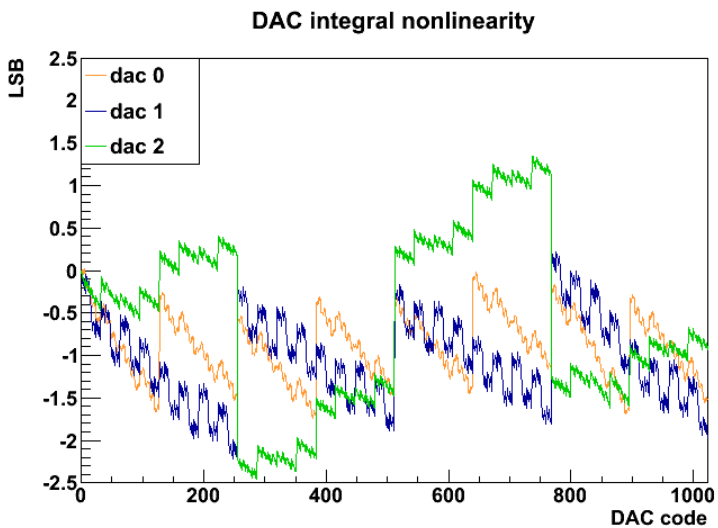


Good agreement between simulation and real behaviour.

Thresholds DAC

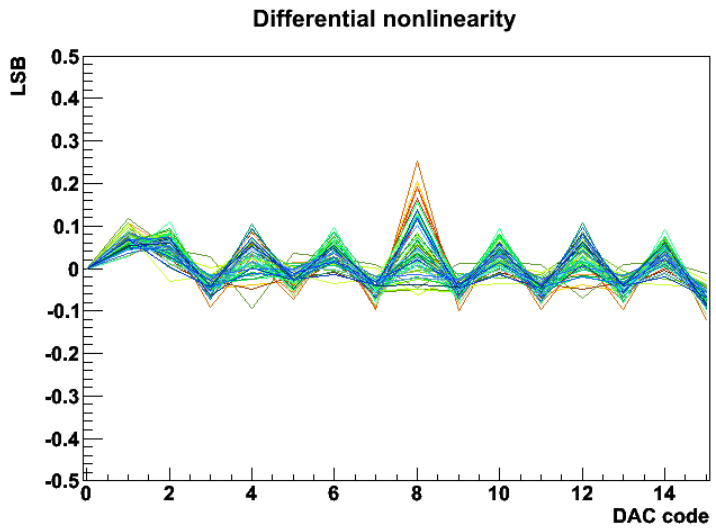


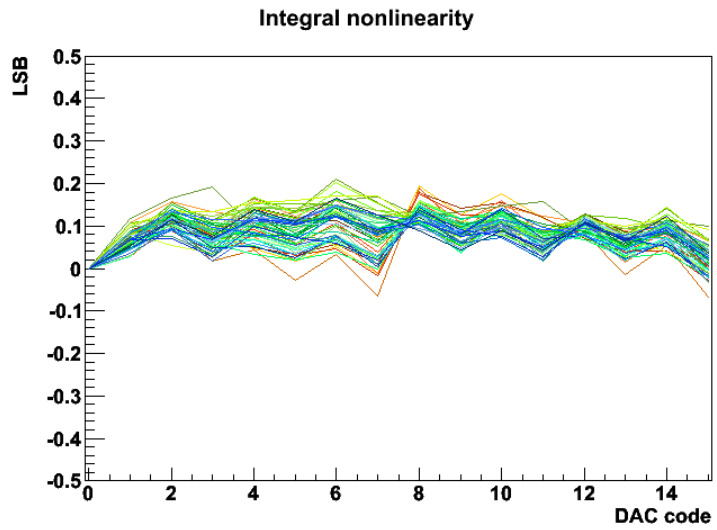


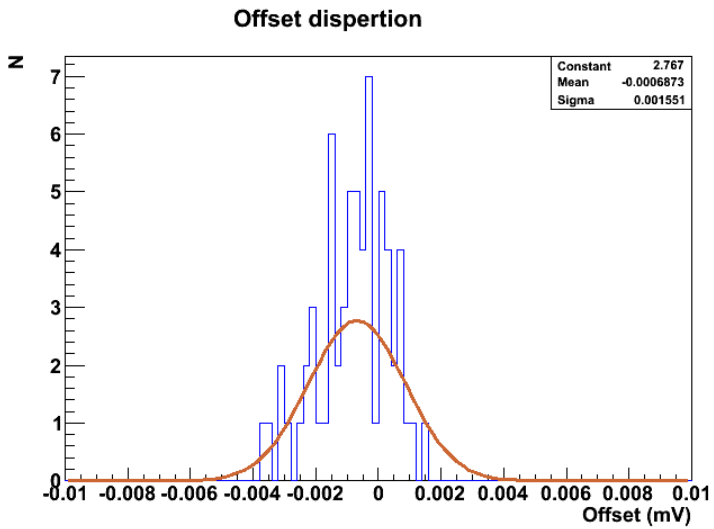


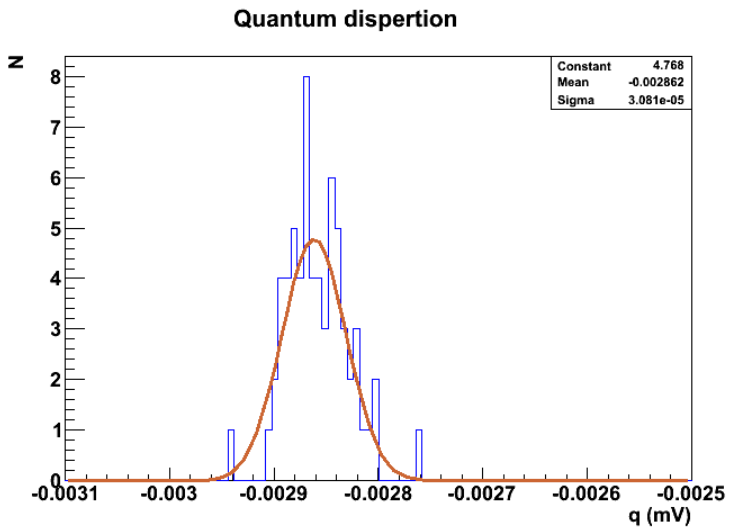
For each DAC, the linearity is about 3 DACU.

Offset correction DAC





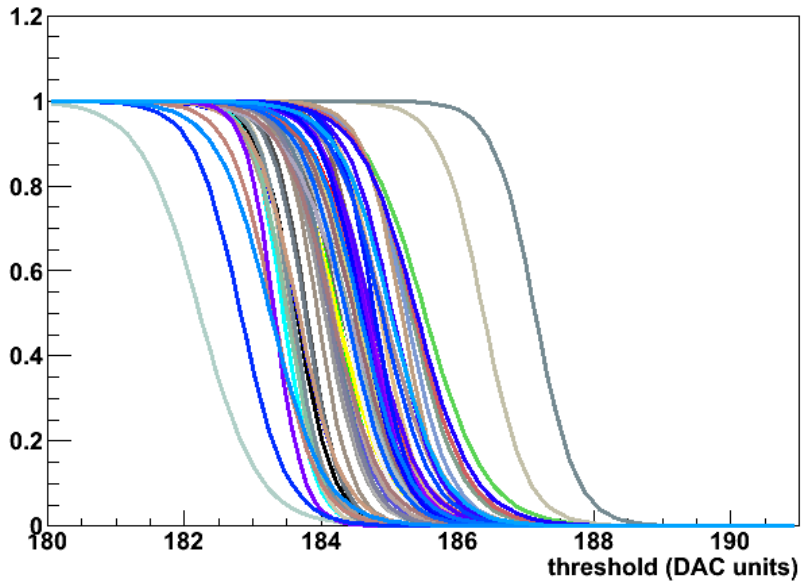


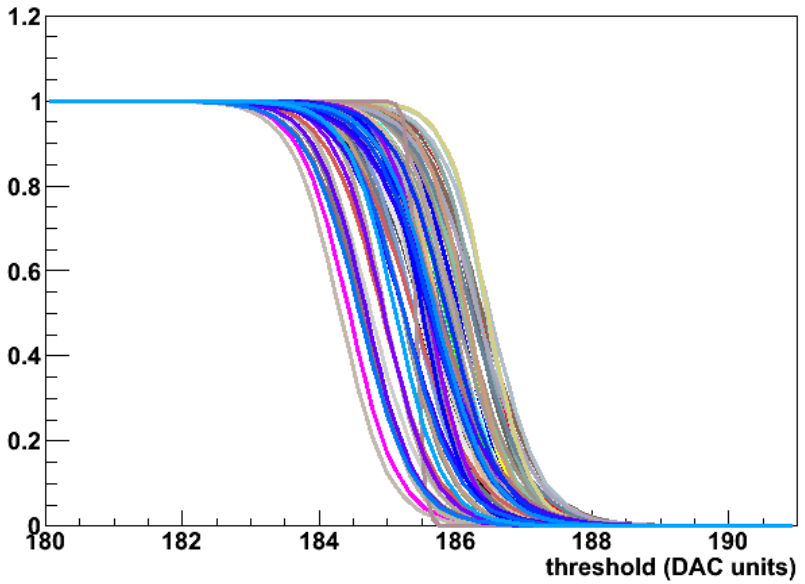


The linearity is better than 1 DACU and q=2.8 mV.

Offset correction

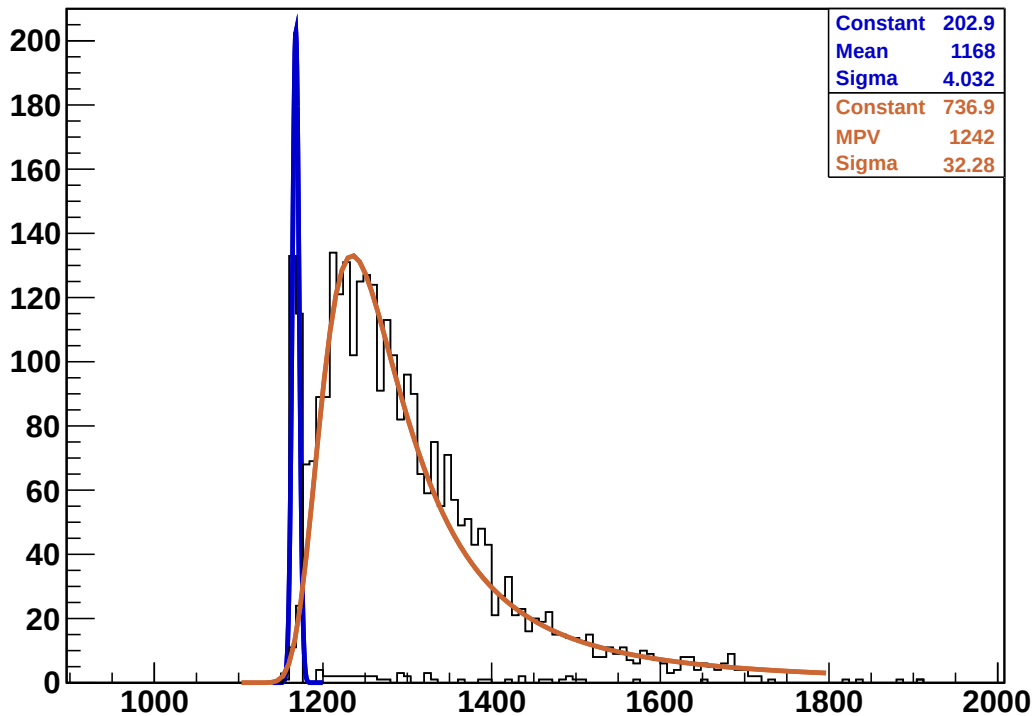
The offset correction allows to divide by 2 the thresholds dispersion inside each chip (thus reducing efficiency disparities of the detector).





Analog Readout

The analog readout has been tested with muon beam at CERN/SPS. The Landau distribution and the pedestal are clearly separated. This feature is very important to calibrate full readout chain and set the 3 threshold with accuracy.



This plot is preliminary!

Outline

Status

Prototypes tests

The chip has been sent in MPW run in June 2010 and 5 prototypes have been received in September 2010. The behaviour of the prototypes is very satisfaying.

Production 1

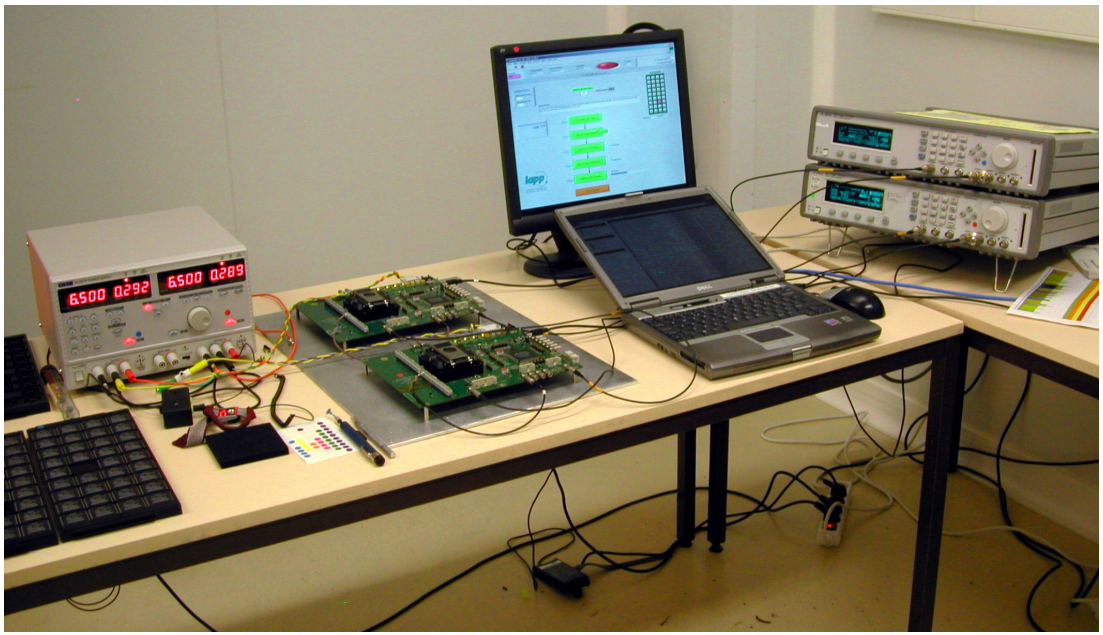
After prototypes tests in LAL and LAPP, a reorder has been placed for 350 chips (packaged in TQFP160) in October 2010. 341 chips have been received in February 2011.

Production 2

Then, a second production has been ordered in November 2011 for 830 chips (still in TQFP160).

Test bench

Three test boards with DIF[1] firmware, and controlled by LAPP Labview DAQ. Thus, data are analysed with MICROMEGAS ROOT framework (used to analyse detector data).



[1]Data Inter-Face Board: the acquisition board designed at LAPP used to read detectors within CALICE collaboration

Test procedure

For each channel of each chip (peaking time: 200 ns, pedestal DAC @7):

- Test input bondings (inject to all channels at the same time with an external capacitor);
- Measure pedestals;
- Inject 22.5 fC with internal C_{test} *vs.* threshold.

Then, analyze data off line with MICROMEGAS data analysis framework:

- Verify bonding of each input;
- Plot S-Curve for each charge, for each channel;
- Plot inflexion point of S-Curves *vs.* input charge;
- Verify gain for each channel (must be nominal $\pm 10\,\%$).

1136 chips have been tested and analysed.

Test results

Production 1

- Packaging: 341/350 yield 97.4 %
- 4 faulty chips (configuration errors);
- 0 with bad bonding;
- 8 with bad gain;
- 329 OK;

Yield: 96.5 %.

Production 2

- Packaging: 794/830 yield: 95.6 %
- 9 faulty chips;
- 0 with bad bonding;
- 33 with bad gain;
- 753 OK;

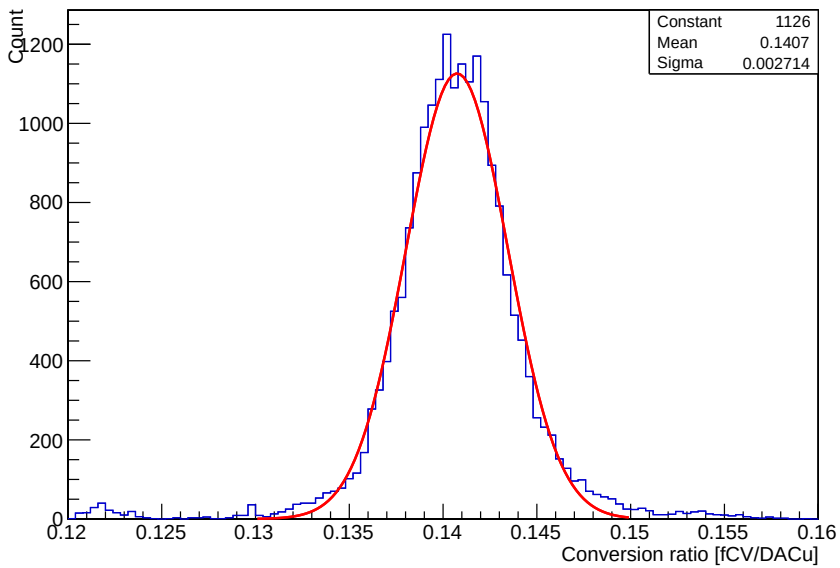
Yield: 94.7 %.

The LAPP use 600 chips at the moment $\rightarrow$ some spares are available for the community!

Gain dispersion

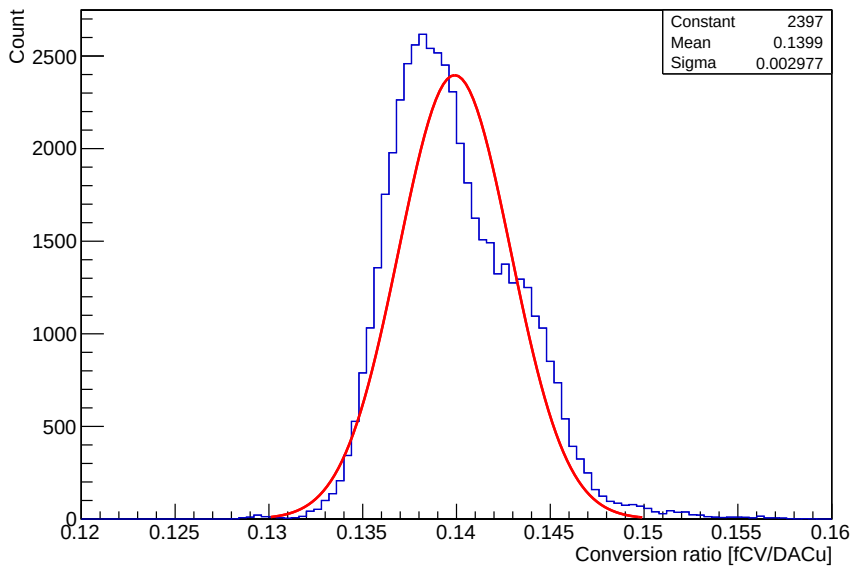
Convertion ratio dispersion, for all channels, @ T_p=200 ns:

Production 1



Mean: 0.14 fC/DAC
Sigma: 0.002 fC/DAC

Production 2

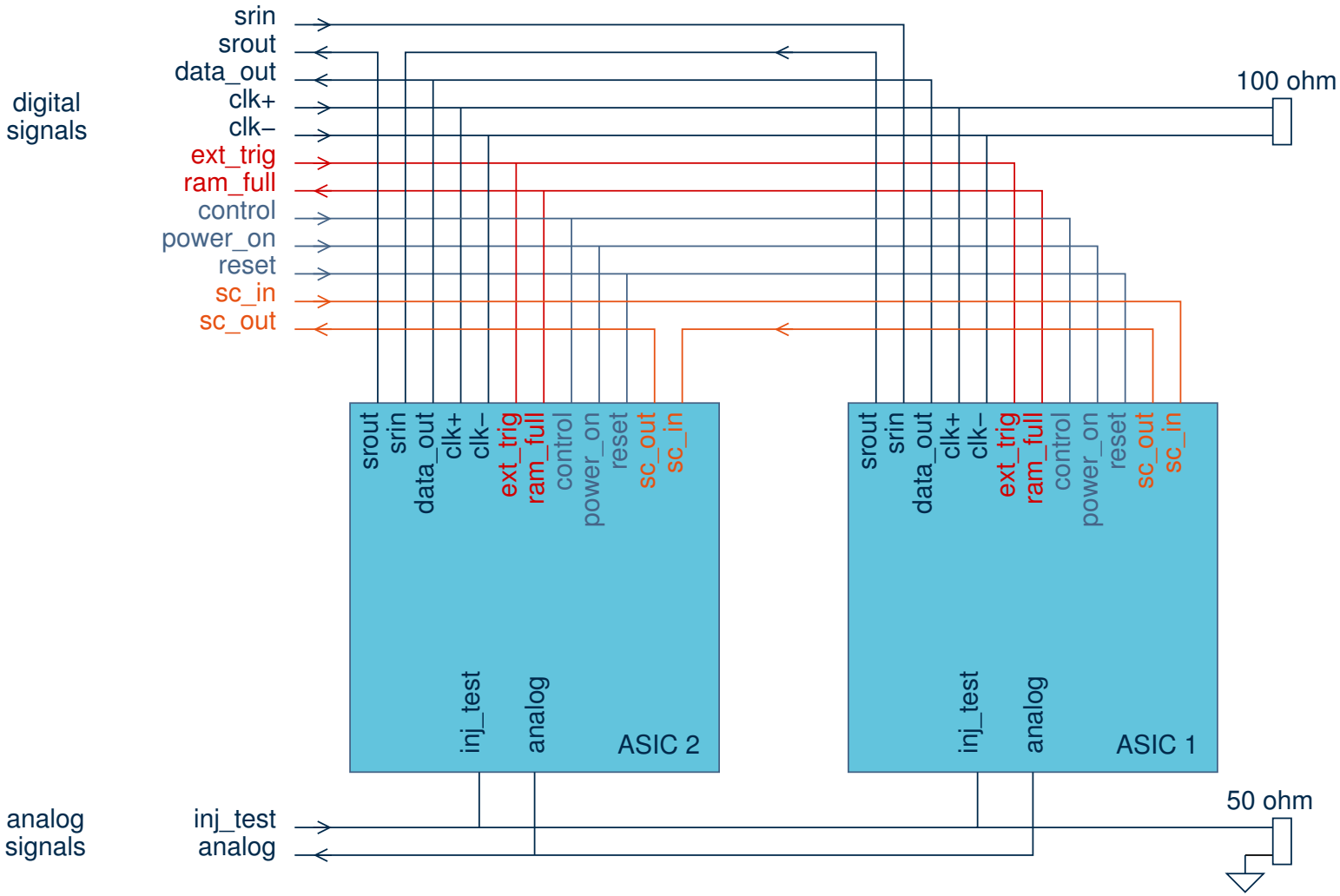


Mean: 0.14 fC/DAC
Sigma: 0.003 fC/DAC
Not gaussian $\rightarrow$ 3 generators not aligned!

Outline

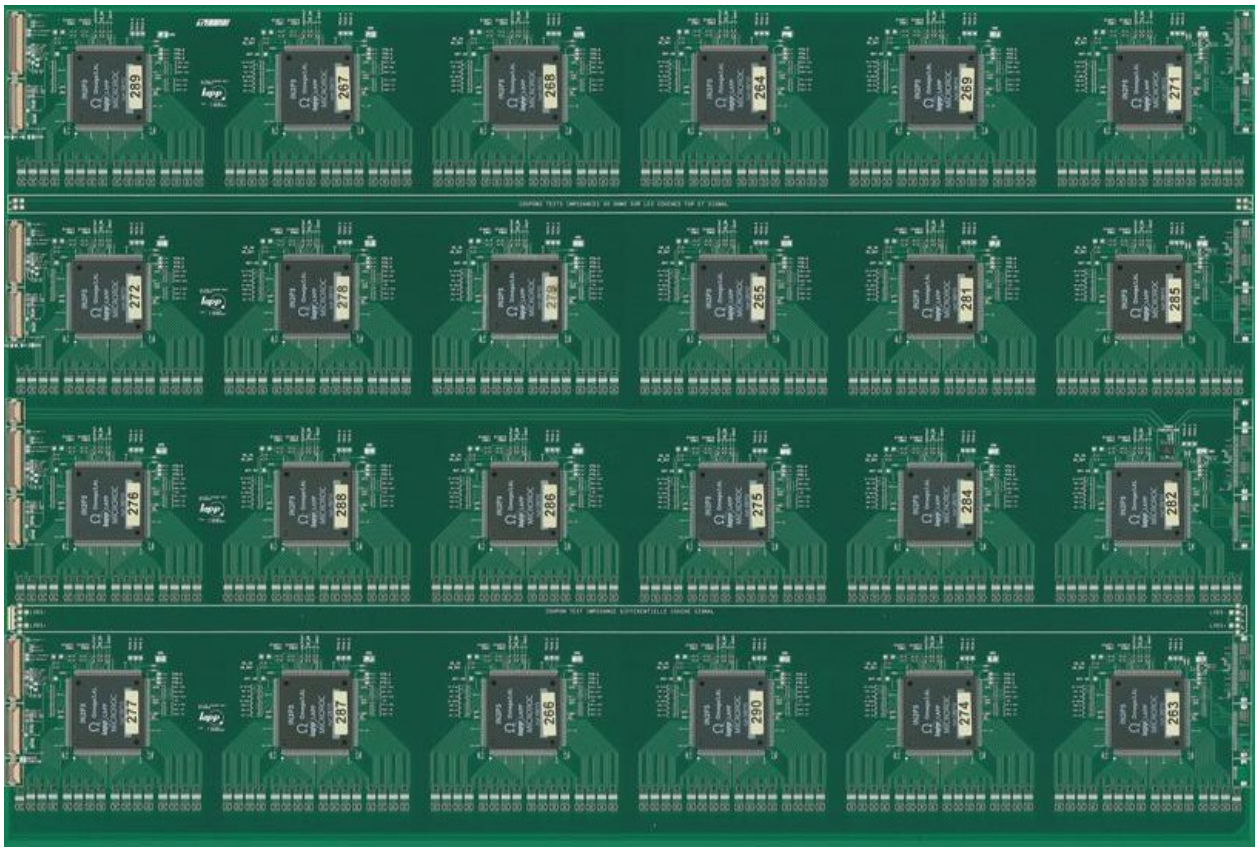
Overview

MICROROC is designed to be daisy chained without any external circuitry, thanks to open collector output signals.



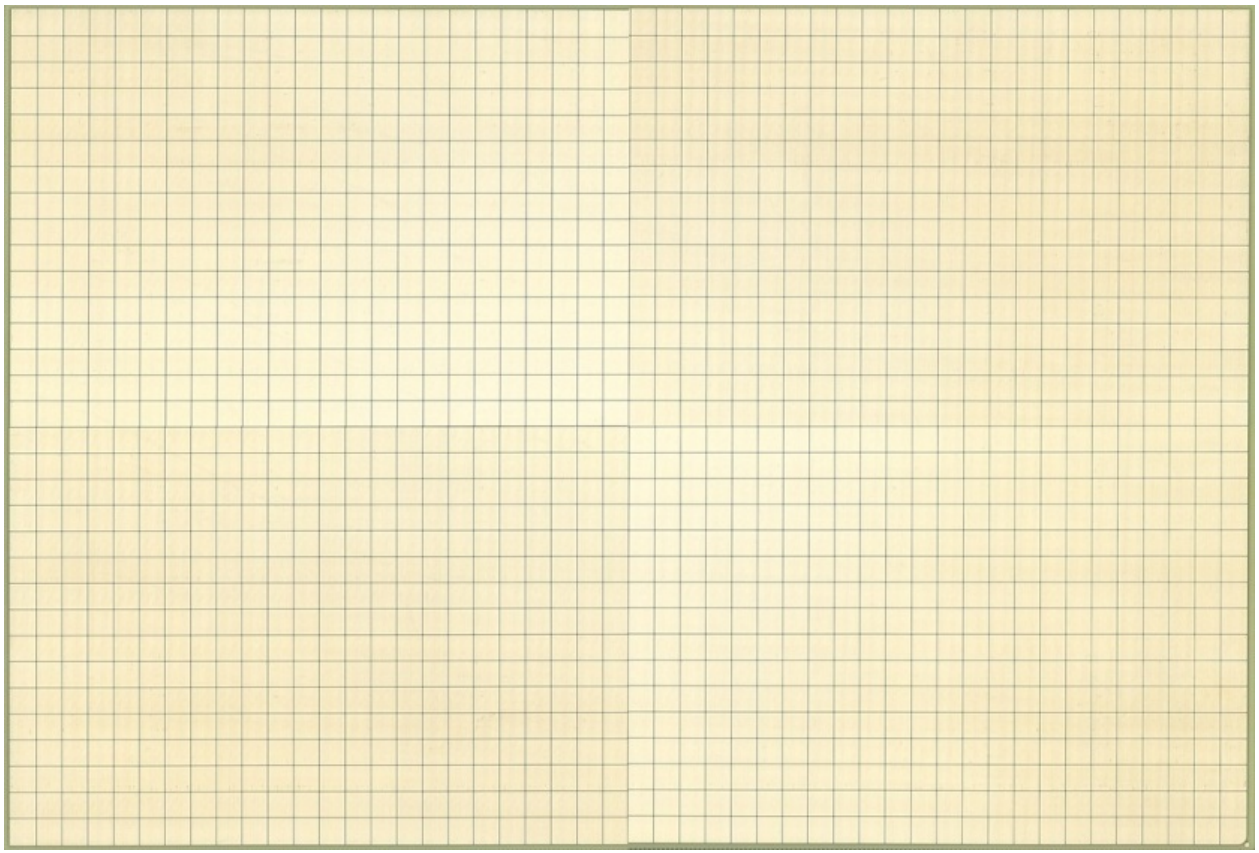
ASU: Active Sensor Unit: top

The PCB hosts 24 chips (1536 channels). A detector (1 m^2 is made of 6 ASUs.



ASU: Active Sensor Unit: bottom

On the other side: the mesh is laid (bulk type) on the 1536 1 cm^2 pads.
Dimensions 32×48 cm^2.

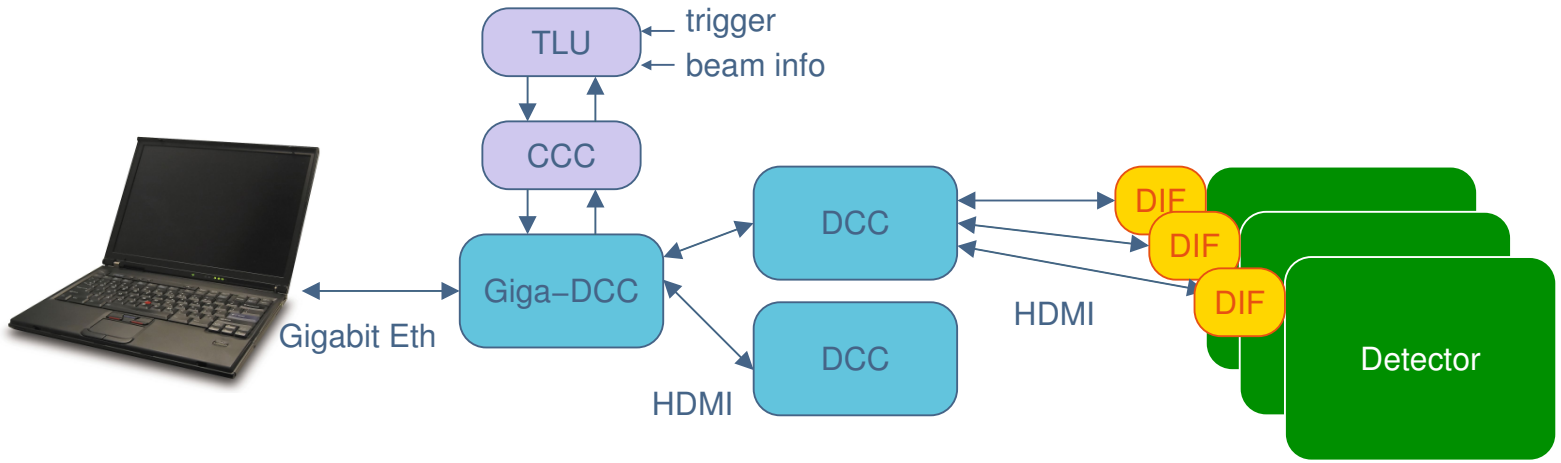


One spare PCB is available to the community as well as a gas-tight test box.

ASU: complete detector

A detector: 1 m^2 is made of 6 ASUs (144 chips).

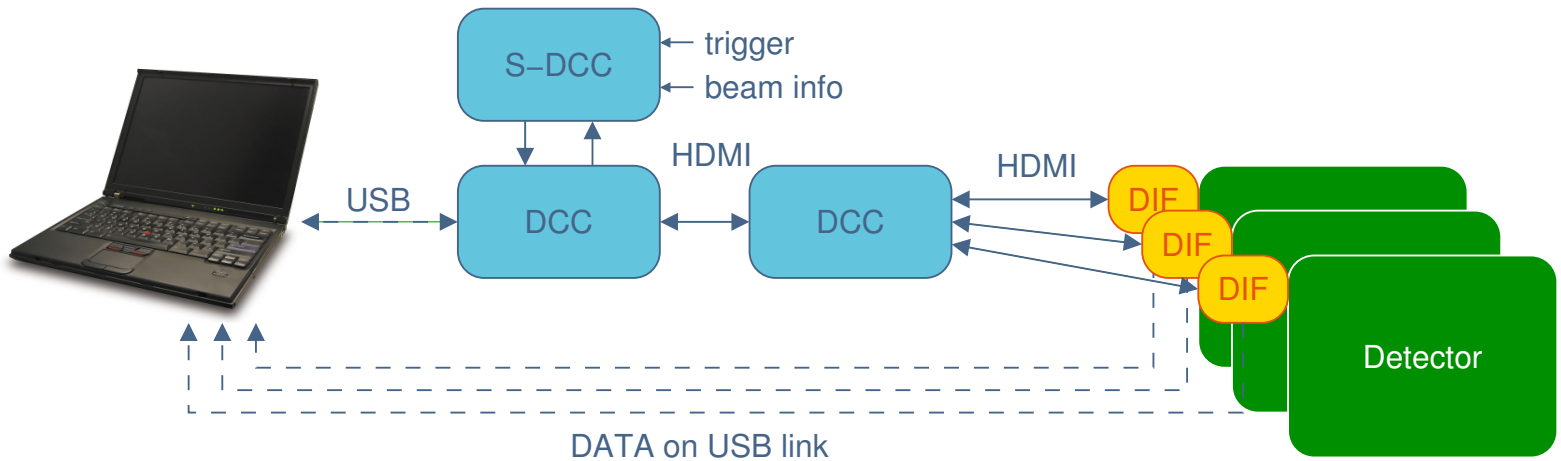
CALICE Readout System



DCC: Data Concentrator Board
DIF: Detector InterFace
TLU: Trigger and Logic Unit
CCC: Clock and Control Card
All boards are 6U and are powered thanks to VME crate.
Software: X-DAQ

DIF Readout with USB

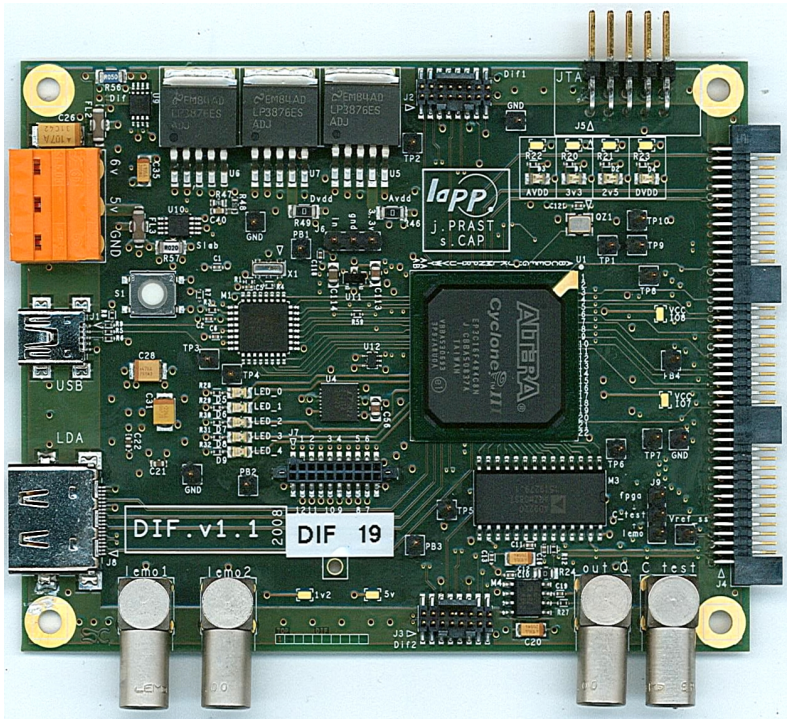
As the whole system CALICE acquisition is not ready yet, an USB readout scheme is used, either with Labview or with XDAQ:



Although not elegant, this system works with 150 DIF!

DIF

The DIF (Detector InterFace boards) handles digital and analog signals, thanks to onboard ADC.
An USB link has been implemented for detector tests and debugging, with a Labview software.



Each DIF manage up to about 150 MICROROC $\rightarrow$ 3 DIF are used for 1 m^2 detector.
Cost: about 200€ (depend on FPGA size, ADC. . .).

MICROROC SRS integration

DIF board use HMDI connector with:

- one pair for clock
- one pair for command
- one pair for busy (state)
- one pair for ramfull (state)

It is foreseen to move trigger signal from command to the free wire of HDMI cables.

No hardware development necessary to use MICROROC with SRS?

Outline

Conclusion

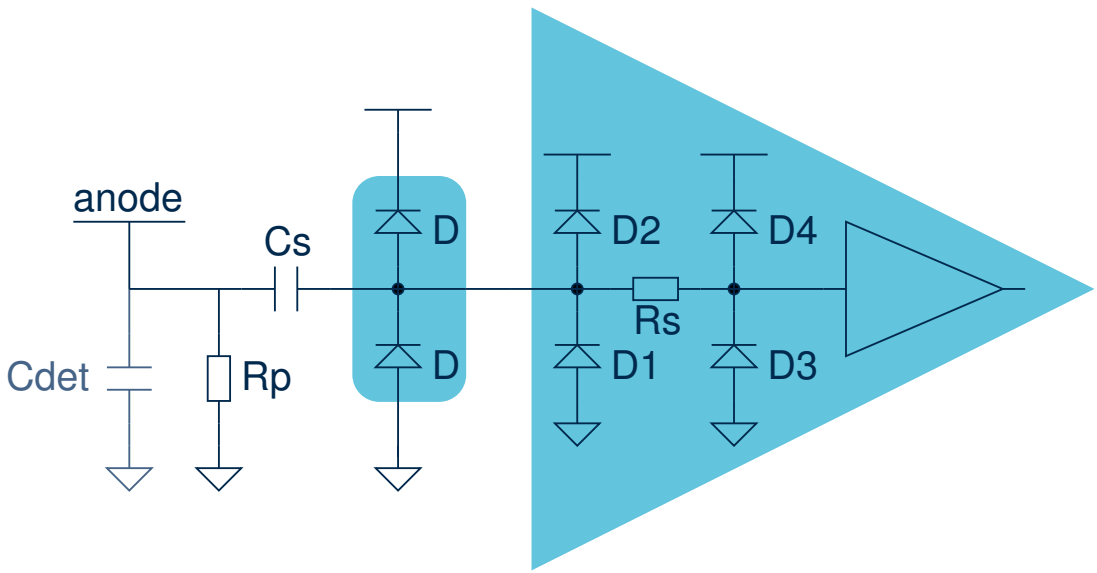
MICROROC chip gives very good performances with MICROMEGAS detectors (see WG2 talks at previous RD51 meetings).
But some improvements are already listed:

- Add zero suppression inside ASIC
- Add one TDC per channel (CLIC requirement)
- Allow a better offset correction (reduce DAC bias)
- Add serial number inside PROM
- Add temperature sensor
- I2C-like configuration

A test with a THGEM detector should be performed this year (autumn RD51 test beam).
Any suggestion or request from RD51 collaboration is welcome!

External protection network

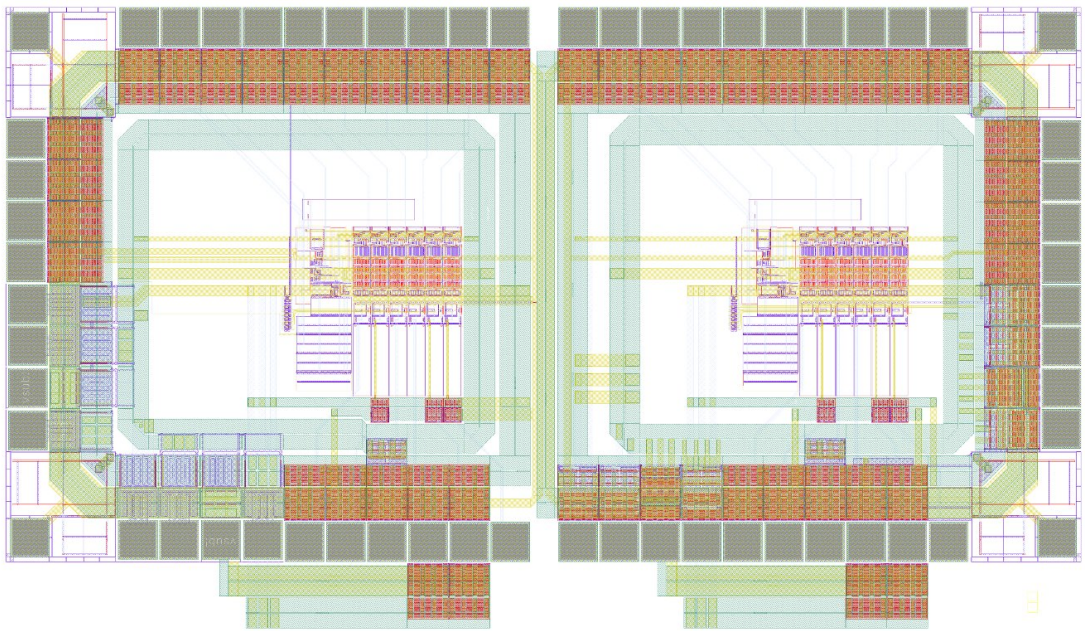
At the moment, an external protection network is used on PCB, to block the remaining surge of spark inside detector. In addition, new protection diodes (Dx) have been included for each channel.
No more dead channels after 3 testbeams.



Rp=1 MΩ, Rs=10 Ω, Cs=470 pF, D are ON-Semiconductor NUP 4114.

Protection benchmark ASIC

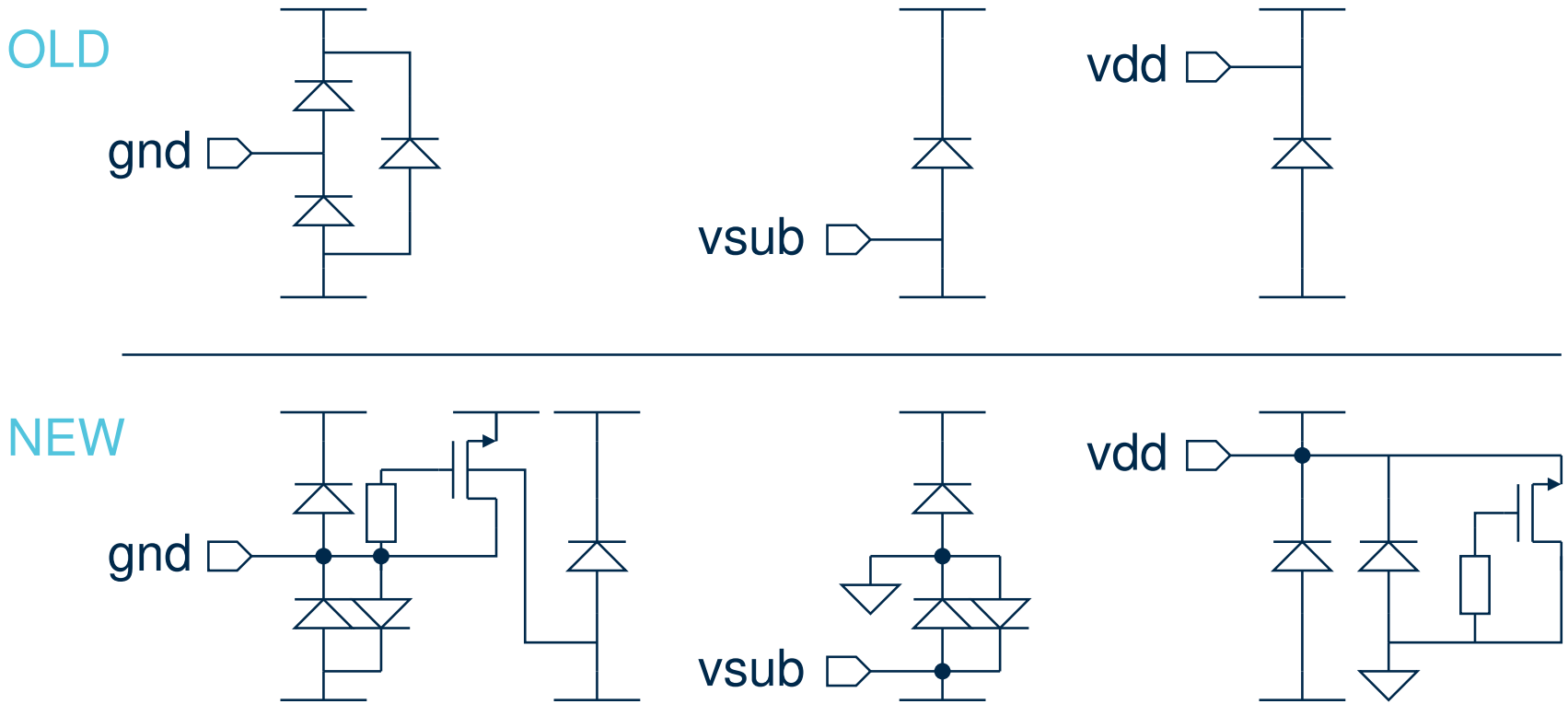
Two savours of power supply pads, 6 kinds of i/o pads for each. Each i/o is connected to a MICROROC CPA.



A dedicated testboard has been designed, to be used with spark generator.
Diodes from CEA Saclay have been packaged to be compatible with this testboard.

Power supply pads

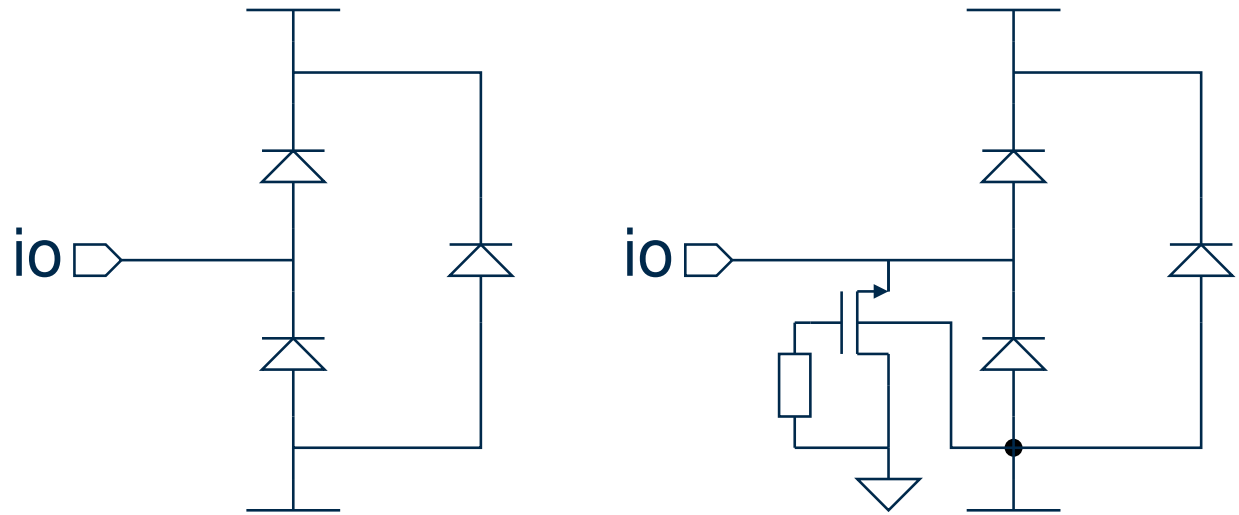
Each power supply pad set consists in 3 pads: vdd, vsub and gnd



OLD type is included in MICROROC.

Input/Output pads

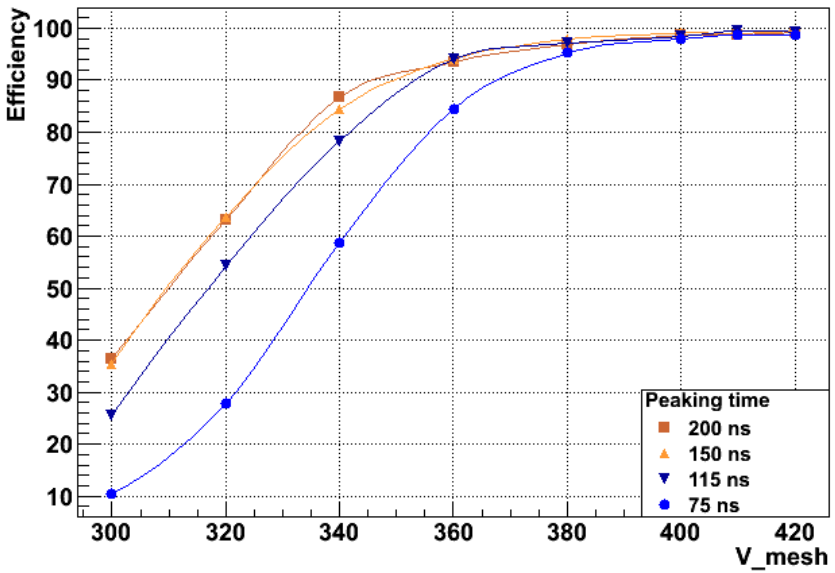
6 kinds of i/o pads for each. Each i/o is connected to a MICROROC PA.
Mainly variation of diode size for 5 inputs, and active protection for 1 input.

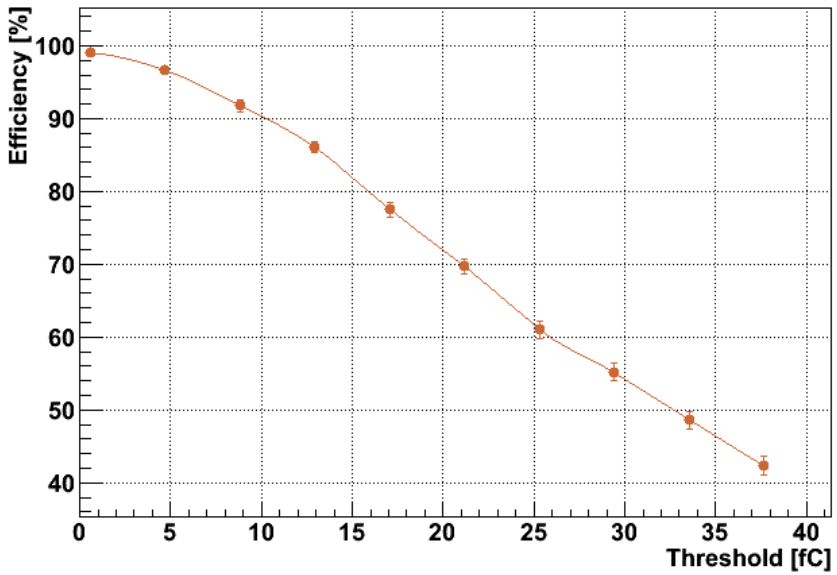


No result yet: tests have just started!

Results with detector

Some great results:



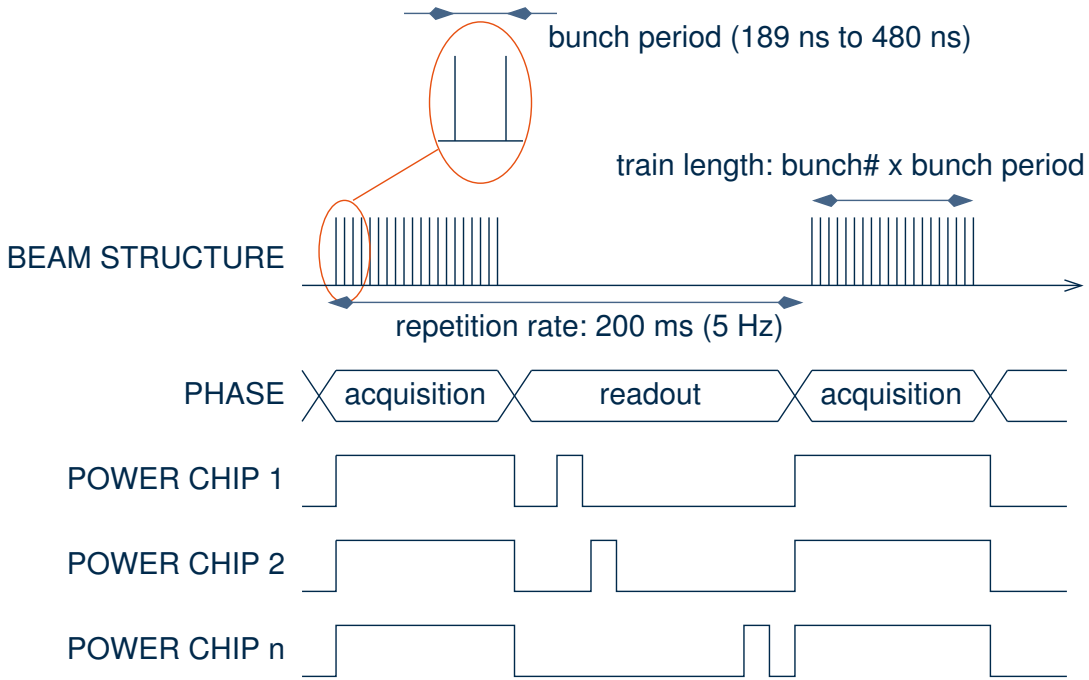


Pedestal correction allows to reach very low bad hit contamination (5 Hz for 9216 channels) in auto-trigger mode.

Detailed power consumption

Stage	Number of stage	Stage Consumption (µA)	Total consumtion including bias (mA)
Preamplifier	64	850	54.7
Shapers	3×64	53	1.13
Discriminators	3×64	40	7.7
DAC	3	173	0.52
Bandgap	1	1200	1.2
Digital (FSM+RAM)	1	2400	2.4
Digital (Data tranmission)	1	400	0.4
Total			68

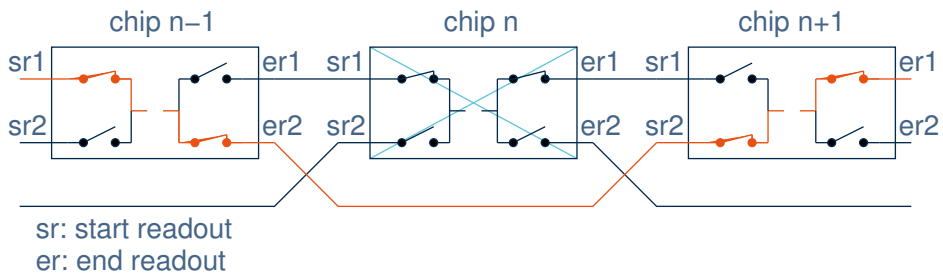
Chip readout



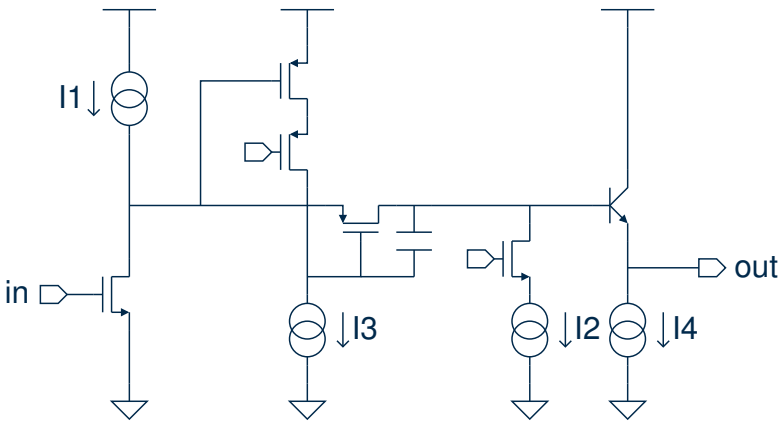
There is one serial output which is transferred to the DAQ during the inter bunch. Moreover, during this inter bunch, the transceivers of chip which are not transmitting data are shut down to save power thanks to the POD (Power-On Digital) module. The data format is: $depth \times (data \times channels + BCID + chipID)$

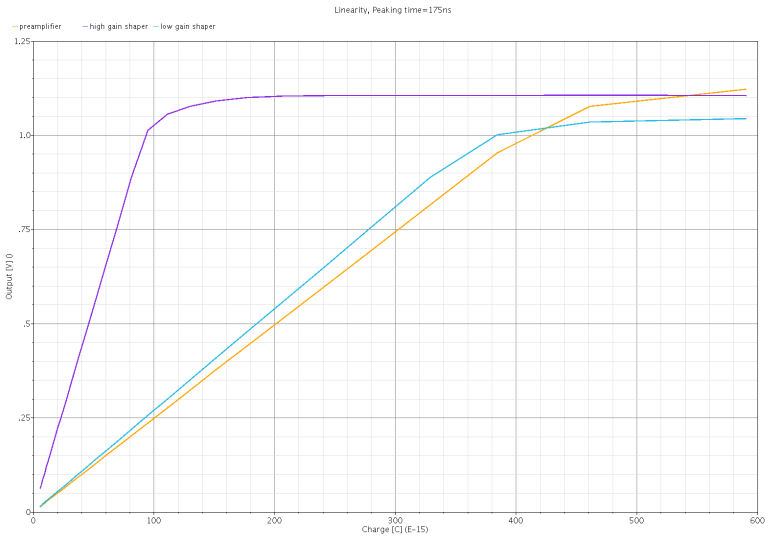
Chip by-passing

MICROROC is designed to be daisy chained without any external circuitry, thanks to open collector output signals, to limit to a bare minimum the number of output lines on the detector.
Redundant readout lines allow a defect chip to be bypassed.

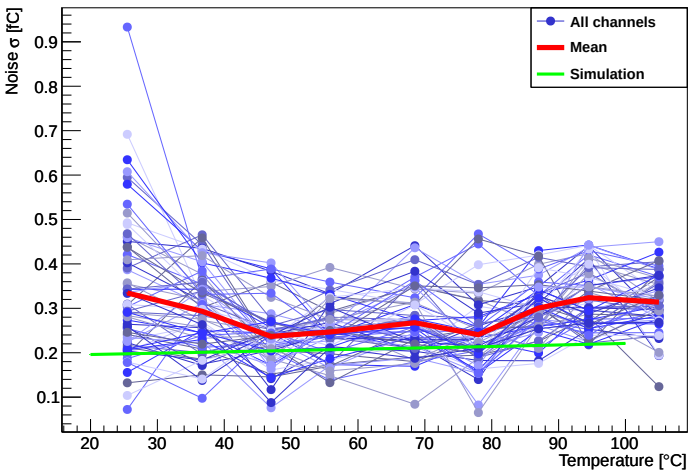


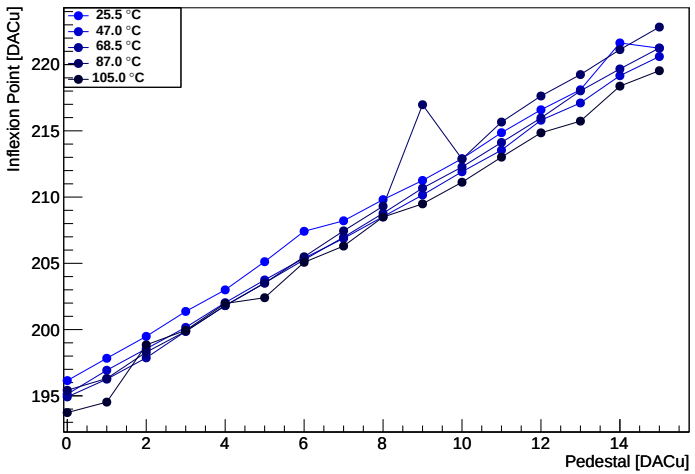
CSA amplifier

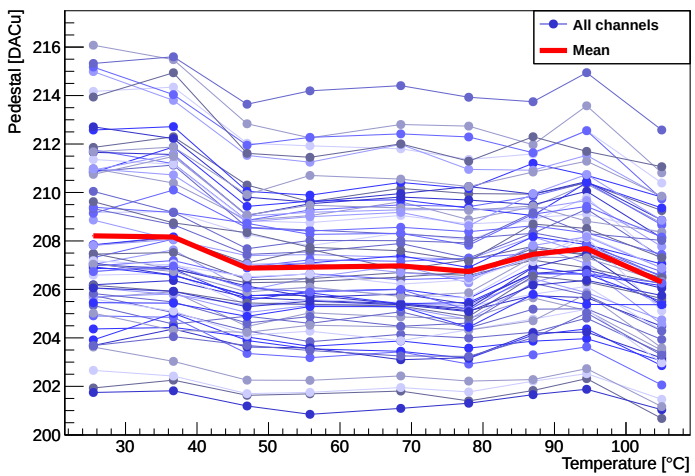




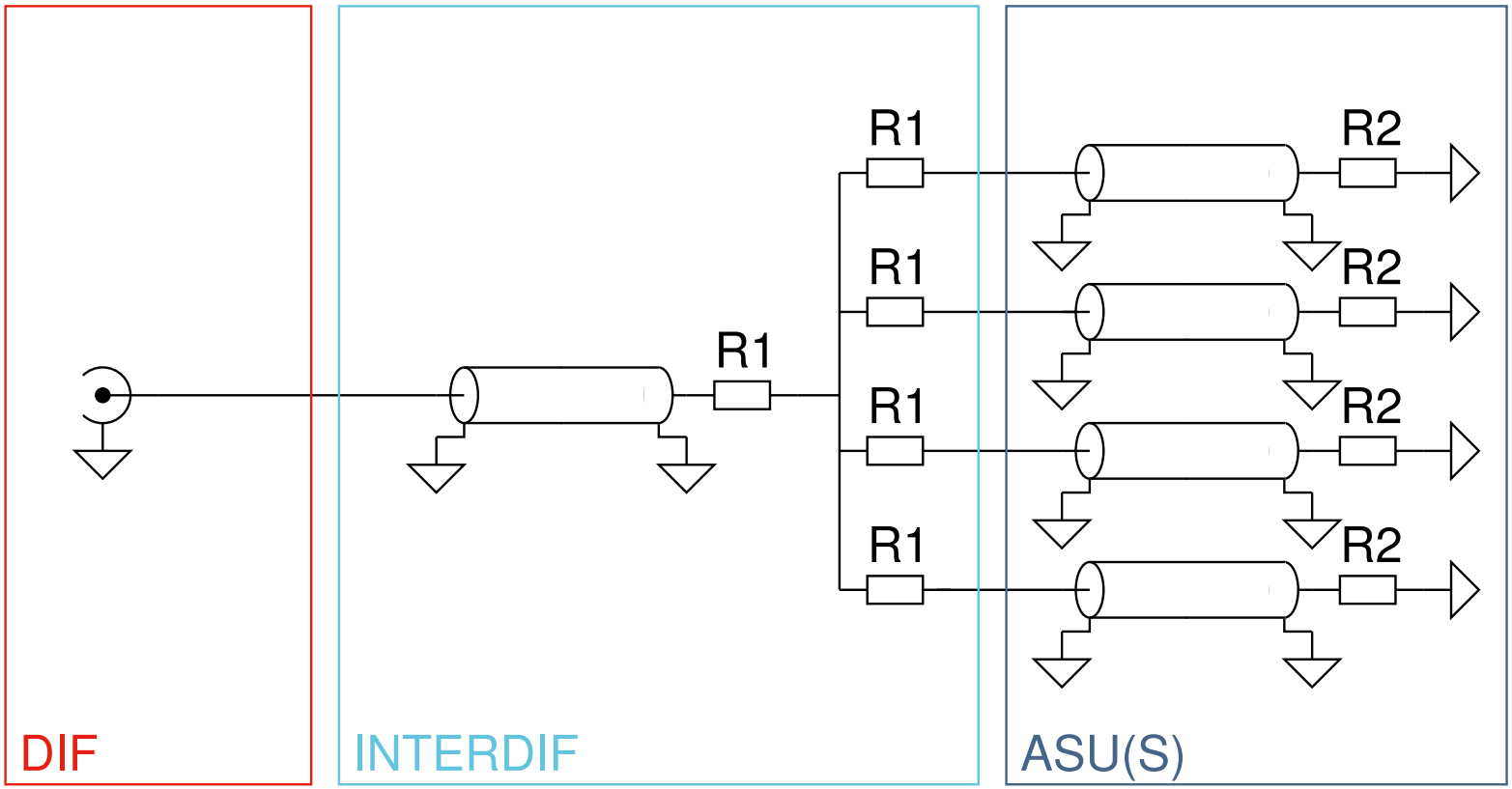
Temperature study







Calibration path



Strips are 50 Ω, R2=50 Ω and R1=30 Ω.
Pulse amplitude is divided by 4.

Calibration path tests

100 mV test pulse seen with 1 GHz active probe (left: begining of line, right: end of line).

Attenuation of line length has been measured and is corrected during inter-calibration.
Line mismatch is also taken into account.

I/O Pads