

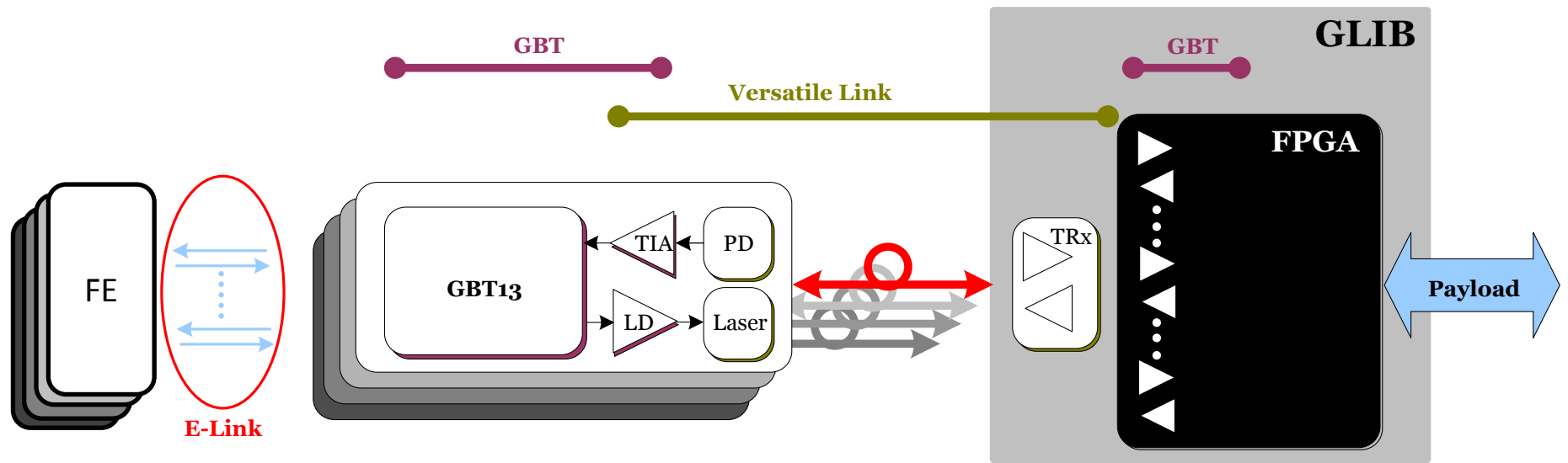
# **The Gigabit Link Interface Board (GLIB)**

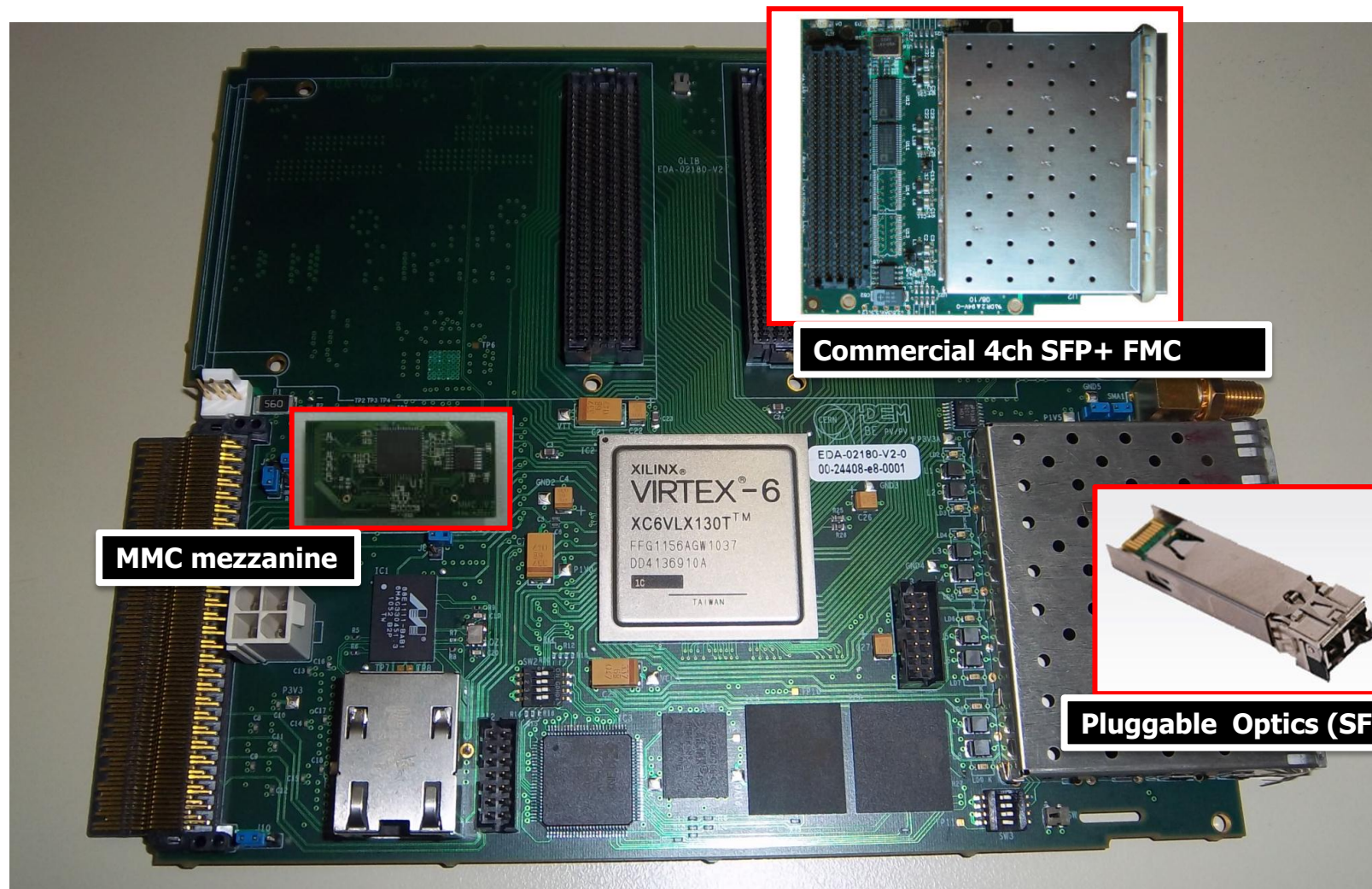
Paschalis Vichoudis, PH-ESE-BE

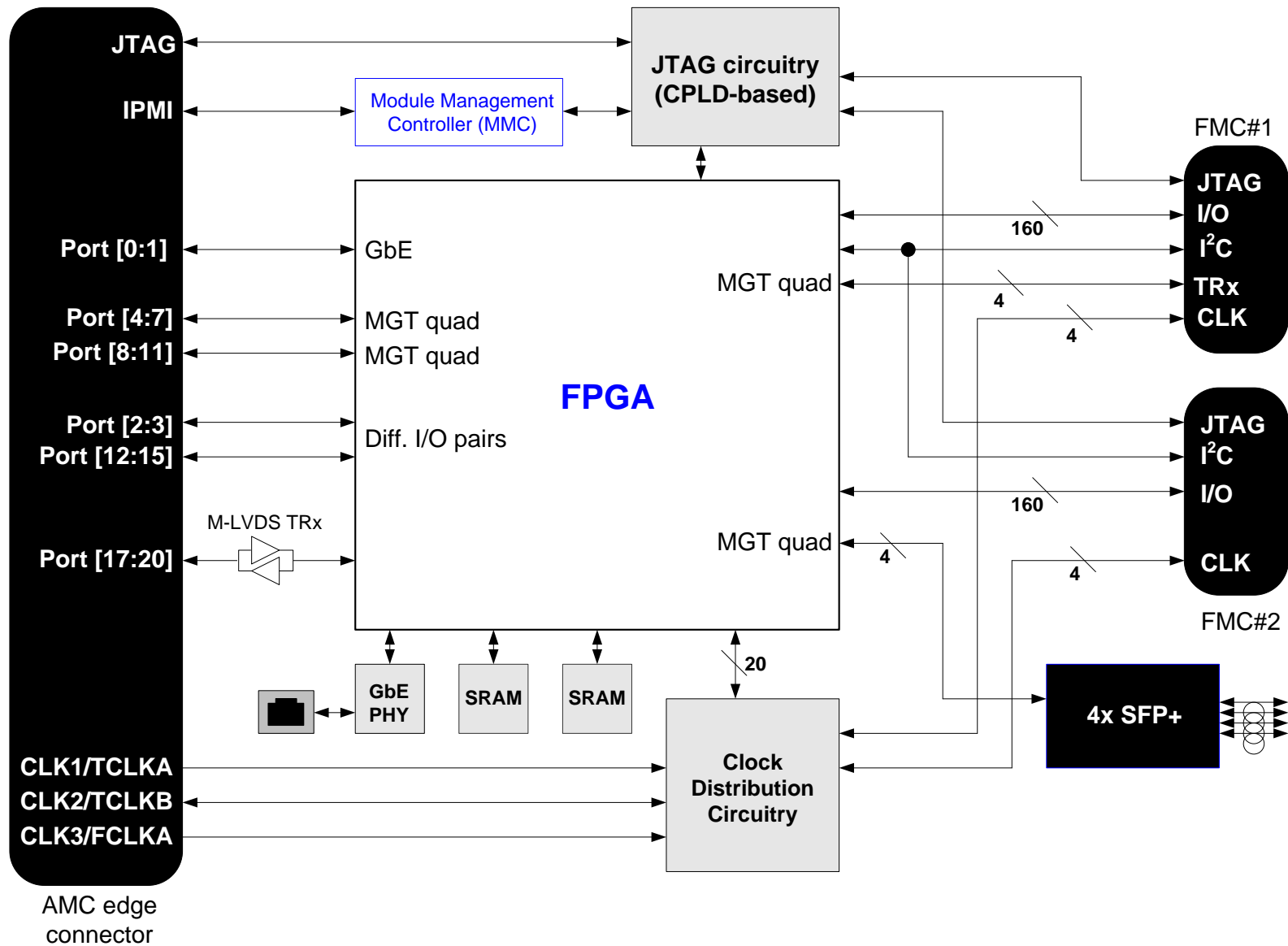
**THE GLIB IS:** an evaluation platform and an easy entry point for users of high speed optical links

**THE GLIB IS TARGETED FOR:**

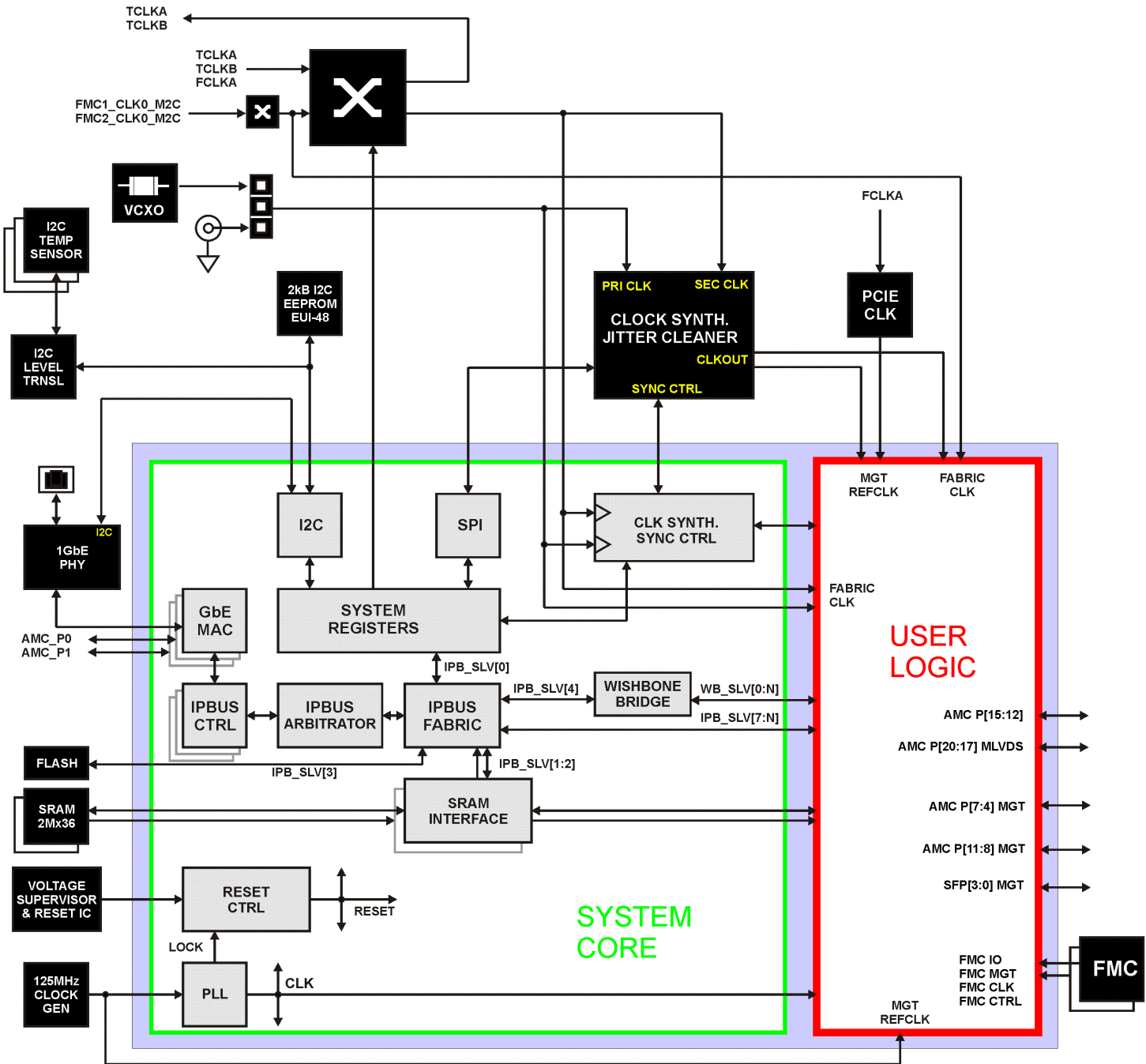
- optical link evaluation in the laboratory
- control, triggering and data acquisition from remote modules in beam or irradiation tests







# FIRMWARE



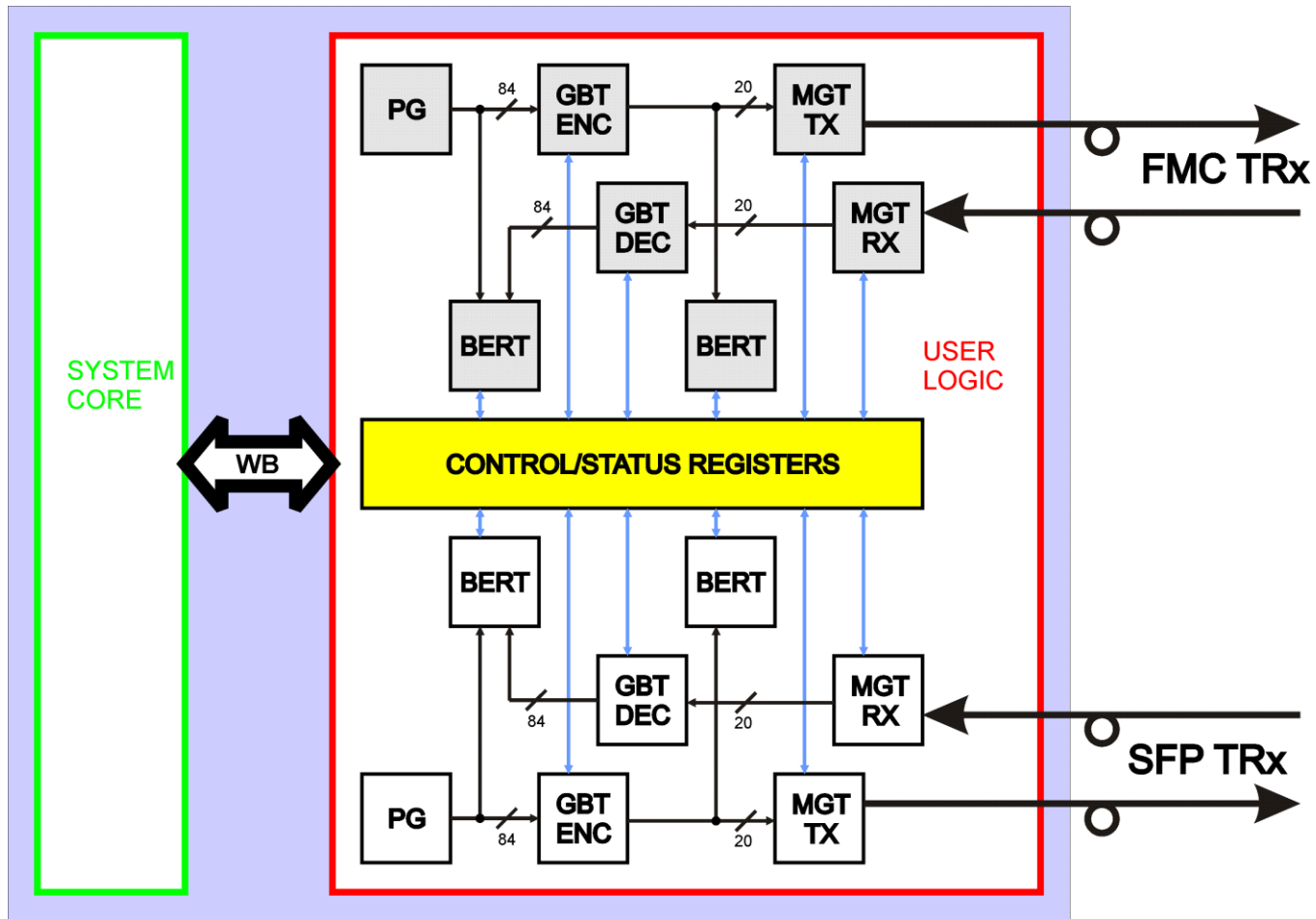
## INCLUDES



## COMPATIBLE



[more info](#)



WebSVN - ph-ese - Rev 413 - , x

← → ↻ [https://svnweb.cern.ch/cern/wsvn/ph-ese/be/amc\\_glib/tags/amc\\_glib\\_1.1.0/firmware/src/?#a1c5048215fbc23964f](https://svnweb.cern.ch/cern/wsvn/ph-ese/be/amc_glib/tags/amc_glib_1.1.0/firmware/src/?#a1c5048215fbc23964f) ☆ 🔍

SSO Logout

### SUBVERSION REPOSITORIES PH-ESE

English - English

**(root)/be/amc\_glib/tags/amc\_glib\_1.1.0/firmware/src/ - Rev 413** Rev

◀ Rev 403 | ✎ Last modification | 📄 Compare with Previous | 📖 View Log | 📄 Download | 📡 RSS feed

#### LAST MODIFICATION

Rev 411 2012-06-06 09:39:43

**Author:** vichoudi

**Log message:**

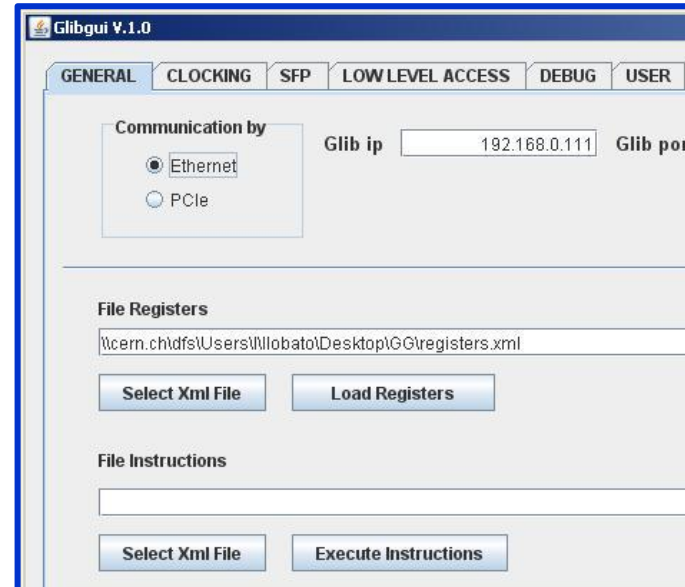
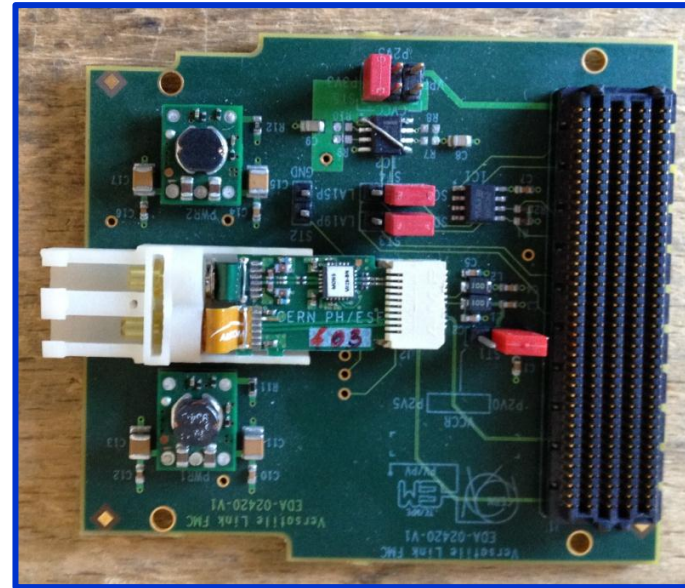
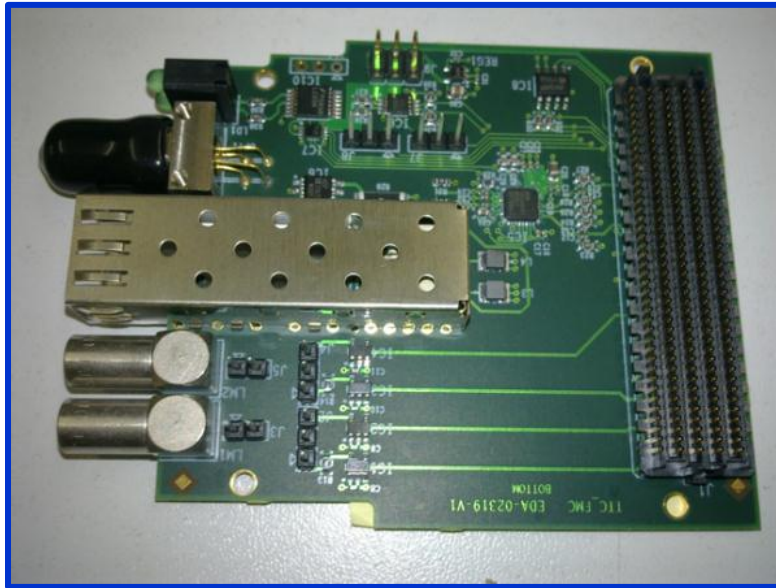
Path	Last modification	Log	Download	RSS
☐ <a href="#">be/</a>	413 1d 00h llobato	<a href="#">Log</a>		<a href="#">RSS</a>
☐ <a href="#">amc_glib/</a>	411 1d 06h vichoudi	<a href="#">Log</a>	<a href="#">Download</a>	<a href="#">RSS</a>
☐ <a href="#">branch/</a>	201 127d 01h vichoudi	<a href="#">Log</a>	<a href="#">Download</a>	<a href="#">RSS</a>
☐ <a href="#">tags/</a>	411 1d 06h vichoudi	<a href="#">Log</a>	<a href="#">Download</a>	<a href="#">RSS</a>
☐ <a href="#">amc_glib_1.0.0/</a>	254 99d 23h vichoudi	<a href="#">Log</a>	<a href="#">Download</a>	<a href="#">RSS</a>
☐ <a href="#">amc_glib_1.0.7/</a>	361 43d 00h vichoudi	<a href="#">Log</a>	<a href="#">Download</a>	<a href="#">RSS</a>
☐ <a href="#">amc_glib_1.1.0/</a>	411 1d 06h vichoudi	<a href="#">Log</a>	<a href="#">Download</a>	<a href="#">RSS</a>
☐ <a href="#">doc/</a>	410 1d 07h vichoudi	<a href="#">Log</a>	<a href="#">Download</a>	<a href="#">RSS</a>
☐ <a href="#">firmware/</a>	403 2d 02h vichoudi	<a href="#">Log</a>	<a href="#">Download</a>	<a href="#">RSS</a>
☐ <a href="#">projects/</a>	403 2d 02h vichoudi	<a href="#">Log</a>	<a href="#">Download</a>	<a href="#">RSS</a>
☐ <a href="#">src/</a>	403 2d 02h vichoudi	<a href="#">Log</a>	<a href="#">Download</a>	<a href="#">RSS</a>
☐ <a href="#">system/</a>	403 2d 02h vichoudi	<a href="#">Log</a>	<a href="#">Download</a>	<a href="#">RSS</a>
☐ <a href="#">user/</a>	403 2d 02h vichoudi	<a href="#">Log</a>	<a href="#">Download</a>	<a href="#">RSS</a>
☐ <a href="#">software/</a>	410 1d 07h vichoudi	<a href="#">Log</a>	<a href="#">Download</a>	<a href="#">RSS</a>
☐ <a href="#">trunk/</a>	410 1d 07h vichoudi	<a href="#">Log</a>	<a href="#">Download</a>	<a href="#">RSS</a>

# MAJOR ACHIEVEMENTS

- **GBT FPGA HDL core improvements**
  - Minimized the latency (20-bit MGT interface instead of 40)
  - Adapted the HDL core to Virtex-6 features for deterministic operation
- **Demonstration of GBT communication**
  - between a GLIB and the GBT evaluation board
  - between two GLIB cards with unrelated clocks
- **Successful implementation of GLIB PC interface**
  - Gigabit Ethernet in Stand alone mode and in a  $\mu$ TCA crate
- **Successful integration of FMC modules for I/O expansion**
- **Firmware architecture for facilitating user development**
  - Separated system/user parts
  - All complexity interfacing/controlling on-board circuitry transparent for user
- **Delivery to beta users**
  - GLIB HW/FW/SW/doc to CMS, ATLAS & ALICE
  - continuous support
- **Big interest from the community**
  - 4 experiments, 10 projects, 20 users, 30 GLIB by end 2012

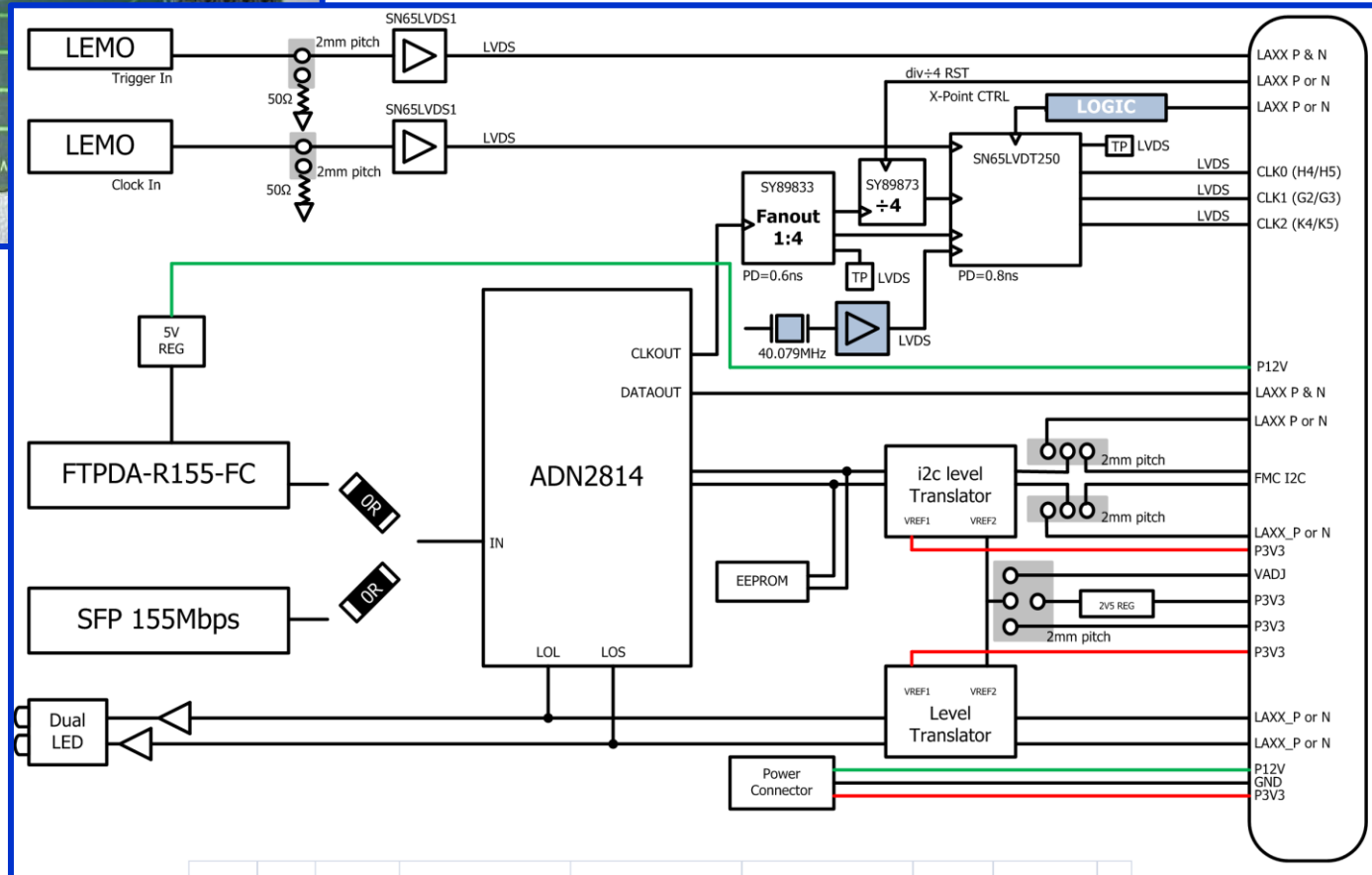
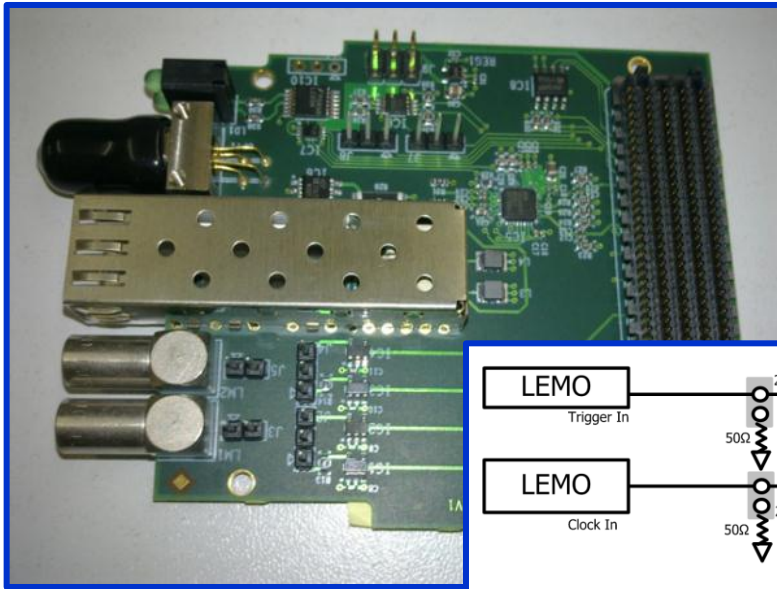


# THE GLIB ECOSYSTEM



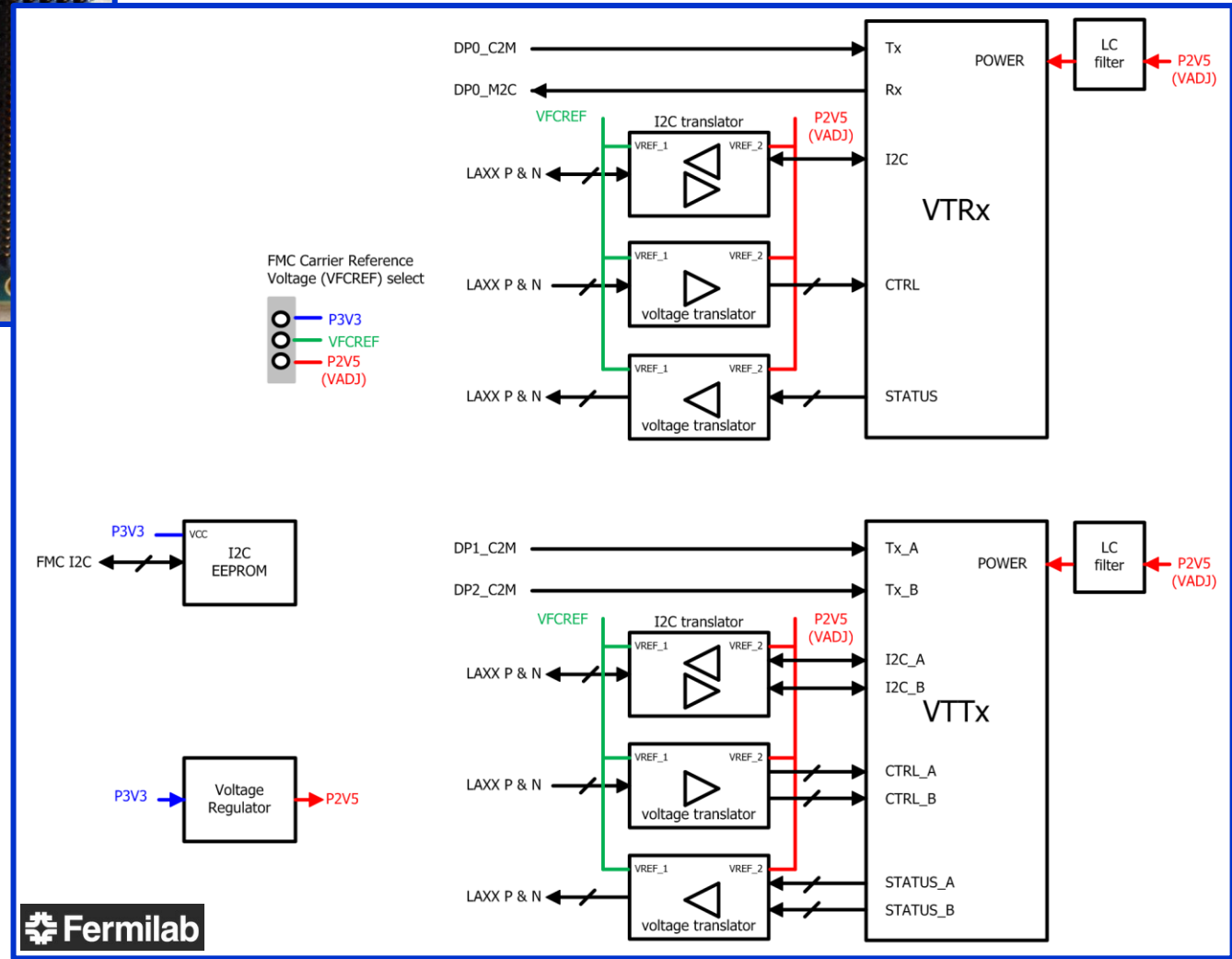
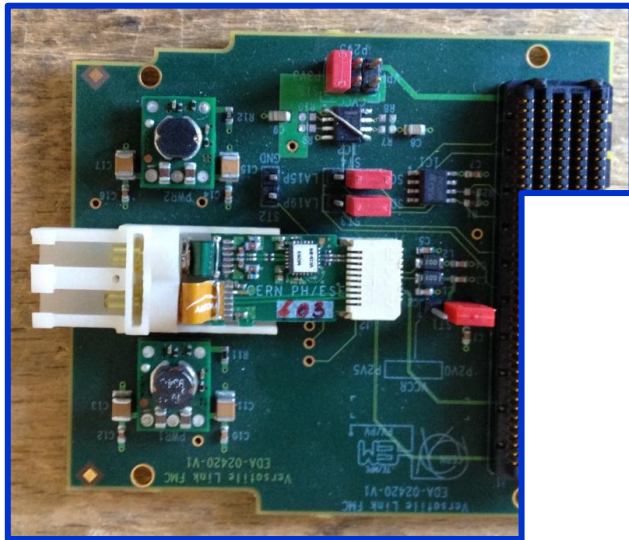
# THE GLIB ECOSYSTEM

## TTC FMC



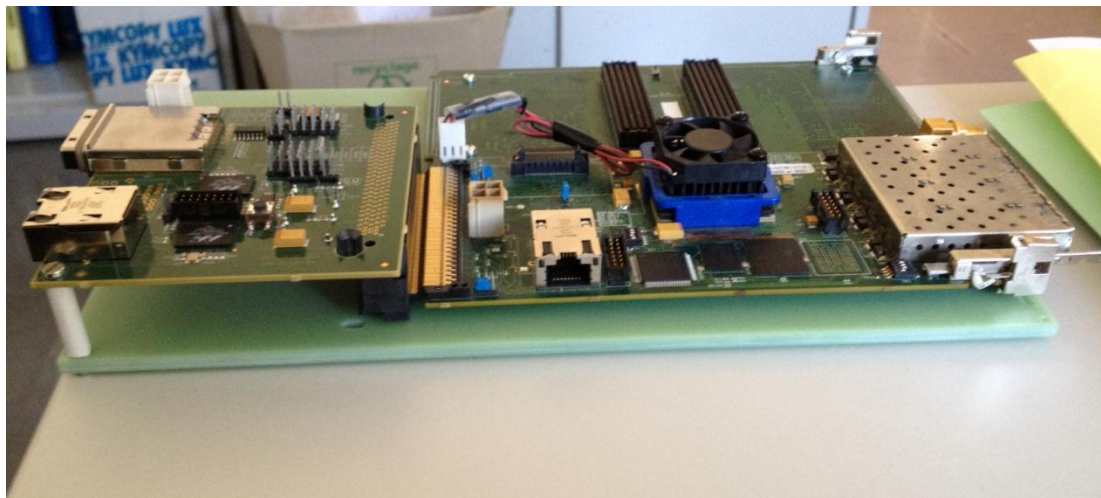
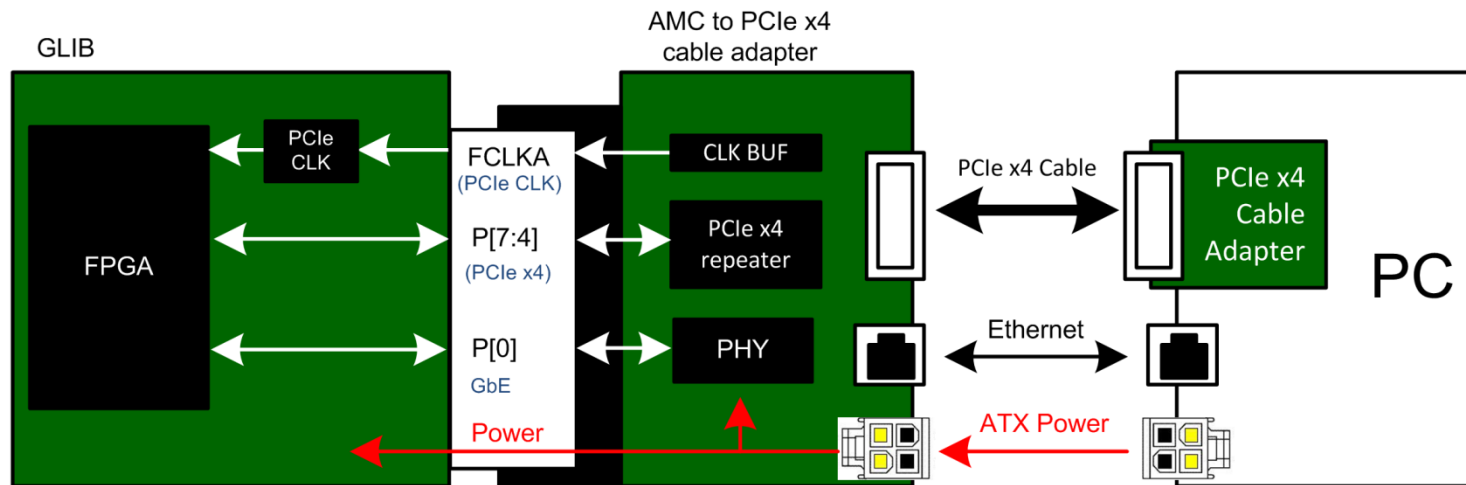
# THE GLIB ECOSYSTEM

## VERSATILE LINK FMC



# THE GLIB ECOSYSTEM

## PCIe ADAPTER



# THE GLIB ECOSYSTEM

## GUI

Glibgui V.1.0

**GENERAL** CLOCKING SFP LOW LEVEL ACCESS DEBUG USER

Communication by  
 Ethernet  
 PCIe

Glib ip  Glib port

---

**File Registers**

**File Instructions**

---

**Board Info**

Version

Serial Number

board\_id

sys\_id

FMC1 presence  
 FMC2 presence

**Board Temperature**

FPGA  
 FRONT  
 REAR

Clock Synthesizer Locked  
 Clock Synthesizer Phase Status

Loading Registers..  
Finished.

# THE GLIB ECOSYSTEM

## GUI

Glibgui V.1.0

GENERAL CLOCKING SFP LOW LEVEL ACCESS DEBUG USER

FCLKA

TCLKA

CLOCK FROM FMC

FMC1\_CLK0  
FMC1\_CLK0  
FMC2\_CLK0

X-POINT SWITCH

LOAD

CLOCK TO SYNTHESIZER

FCLKA  
FCLKA  
TCLKA  
CLOCK FROM FMC

CLOCK TO TCLKB

NOT USED  
NOT USED  
FCLKA  
TCLKA  
CLOCK FROM FMC

CLOCK TO FPGA FABRIC

FCLKA  
FCLKA  
TCLKA  
CLOCK FROM FMC

Loading Registers..  
Finished.

Clear

**Registers**

- FPGA1
  - system\_regs
    - board\_id**
    - sys\_id
  - firmware\_id
  - test\_reg
  - ctrl
    - ctrl\_2
  - status
    - status\_2
  - ctrl\_sram
  - status\_sram
  - spi\_bdata
  - spi\_command
    - spi\_rdata
  - i2c\_settings
    - i2c\_command
    - i2c\_reply
  - sram1\_space
  - sram2\_space
  - user\_ipb\_space
  - user\_wb\_space

**Register Details**

Type	Address	Mask	Offset	Width
LEAF	0x00000000	n/a	n/a	n/a

Register Address:

Bitfield    Offset:     Width:

Number of Words:     **Read Register/Bitfield**

Transaction Completed:

Number of Words:     Data:

**Write Register/Bitfield**

**Start Recording**    **Stop Recording**

Loading Registers..  
Finished.  
\*\*\*\*\*  
Starting the communication  
Connecting to GLIB to read the register  
Data 0 received= 474C4942  
Data 1 received= 4C414220  
Data 2 received= 080C1001  
Data 3 received= 80D600F1  
Data 4 received= 80D600F2

**Clear**

# STATUS AND SUMMARY

**Very advanced stage:** although only 2-year old project

**Prototypes are already delivered to beta users:** since 2011

**Big interest from the community:** 4 experiments, 10 projects, 20 users, 30 GLIB

**Production:** first batch before end 2012

**Spin-offs:** TTC FMC, improvements of GBT-FPGA HDL core