Using FPGA with embedded transceivers for optical link valuation

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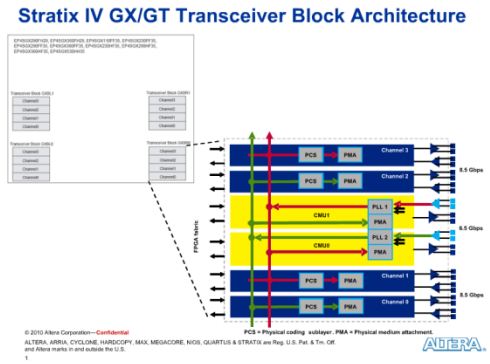
SMU PHYSICS LAB
Annie Xiang
Datao Gong
Andy Liu
Kent Liu
Jingbo Ye

Outline

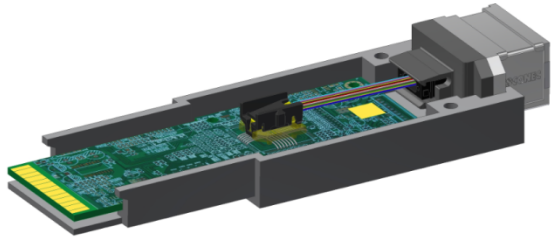
- Introduction
- BERT implementation
- Transceiver Instantiation
- Optical link demonstration
- Tests and results
- Summary and future work

Introduction

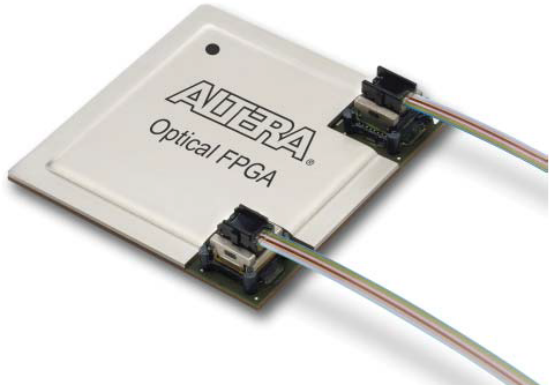
- FPGA with embedded transceivers developed for 100GbE systems is an affordable option for the testing of a multi-lane 10Gbps system
  - Custom parallel front-end components are proposed in several upgrade programs
  - Parallel back-end candidates are commercially maturing



- System evaluation of these transceiver channels provides necessary insights on
  - Power/jitter budget which results from the signal integrity characteristic electrical and optical parameters
  - Protocol compatibility and implementation considerations on candidate device families



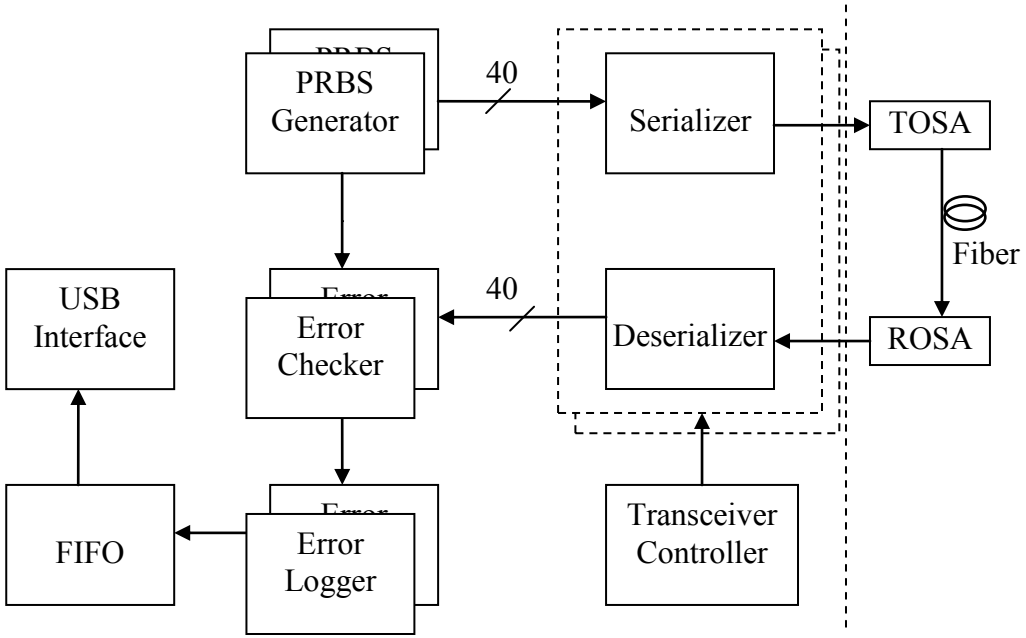
- Results and numbers are for typical use case of Altera devices. Optimization will depend on the specific implementation.



BERT implementation

- The objective is to build a 8-12 channel, 10Gbps / channel unframed physical layer bit-error-rate testing (BERT) capable FPGA-based platform
- Use vendor developed transceiver toolkit to survey the transceiver channel characteristics
- Configure the transceiver in simplified basic mode (as serializer, deserializer and clocking hardware) and build custom firmware for protocols and DAQs

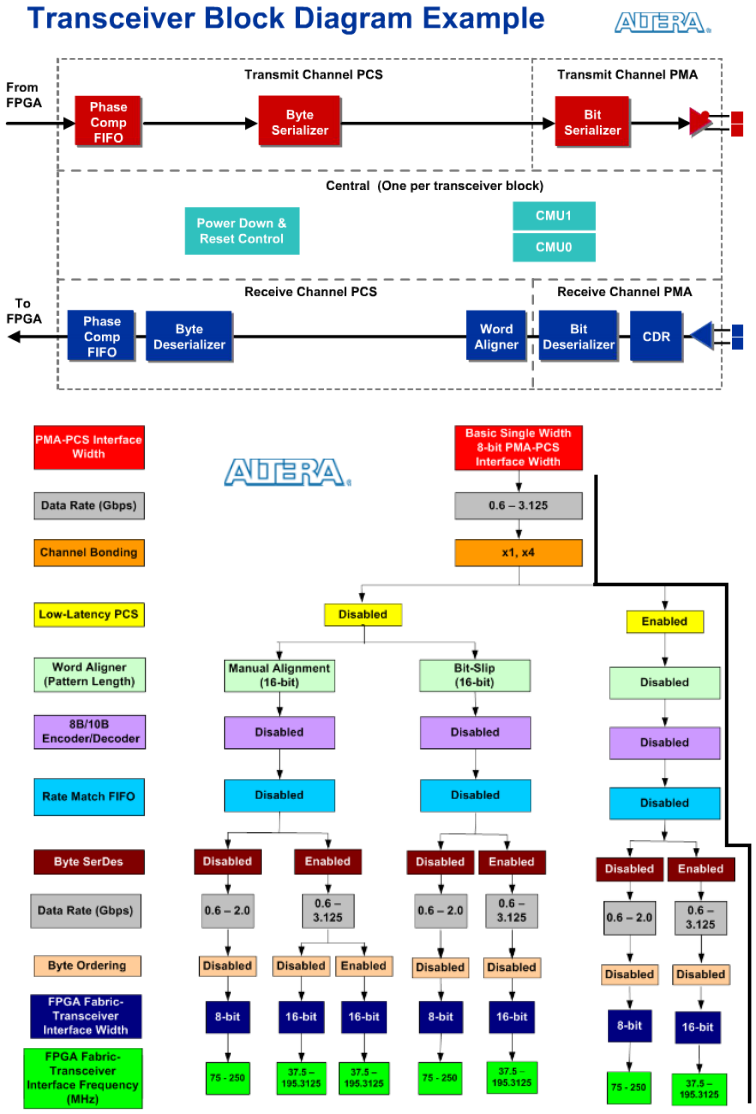
- PRBS generator, error checker, error logger function blocks are platform agonistic
- The PRBS generator./checker produces long stress patterns without using a lot of memory and self-aligns without boundary acquisition
- The error logging FIFO buffers both bit error data and link status data for in situ process and offline analysis.
- Transceiver and user interface implementations are hardware dependent



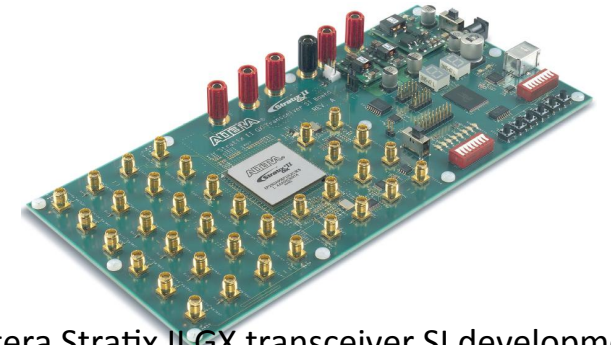
Transceiver Instantiation

- The transceiver instantiation flow in Altera devices is:
  - Create transceiver and reconfiguration controller instances using MegaWizard manager
  - Build reset and power control logic
  - Place multiple channel with transceiver block hardware constraint

- All PCS (physical coding sublayer) function blocks are to be bypassed for the GT blocks to run up data rate above 8Gbps
  - All Data processing and control logic and communication protocols are to be implemented in FPGA fabric.
  - The GT blocks is running up to 9.6Gbps
  - Investigate the clock and data paths constrains during compilation

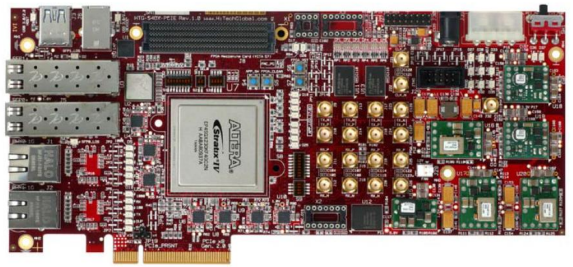


FPGA and Carrier Boards



Altera Stratix II GX transceiver SI development board features:

- Altera Stratix II GX EP2SGX90 device
- Six duplex transceiver channels at up to 6.375 Gbps each channel via on board SMA connections
- The Stratix II FPGA device available in production today, but the development kit is updated to Stratix IV edition

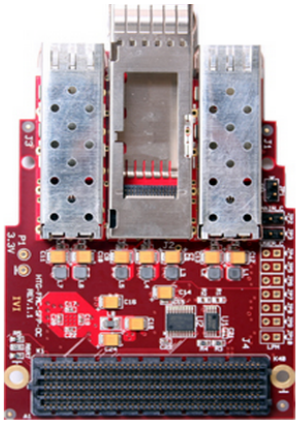


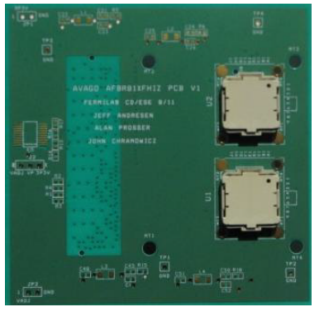
HiTech Global Stratix IV GT development platform features:

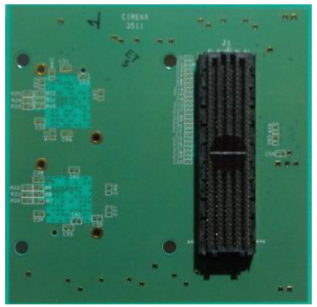
- Stratix IV GT EP4S100G2 device
- Twenty-four duplex transceiver channels at up to 11.3 Gbps each channel. Four are SMAs.
- One high speed FMC for hosting custom modules
- Two SFP+ (including dual channel EDC chip) hosts

FMC (FPGA Mezzanine Card) HPC (high pin count connector) accommodates:

- up to 10 multi-gigabit lanes (>9GHz)
- 80 differential pairs (or 160 single ended)
- clocks, JTAG, I2C and power connections
- Standard mapping for compatibility

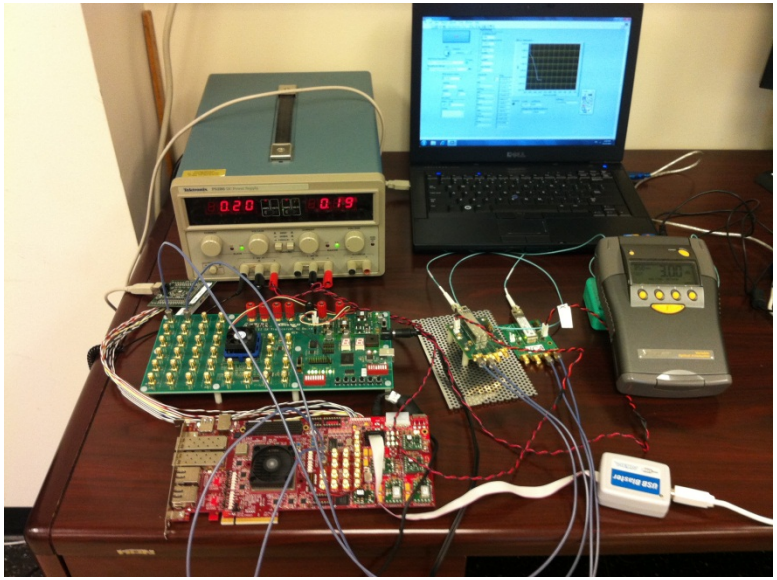






Optical link Demonstration

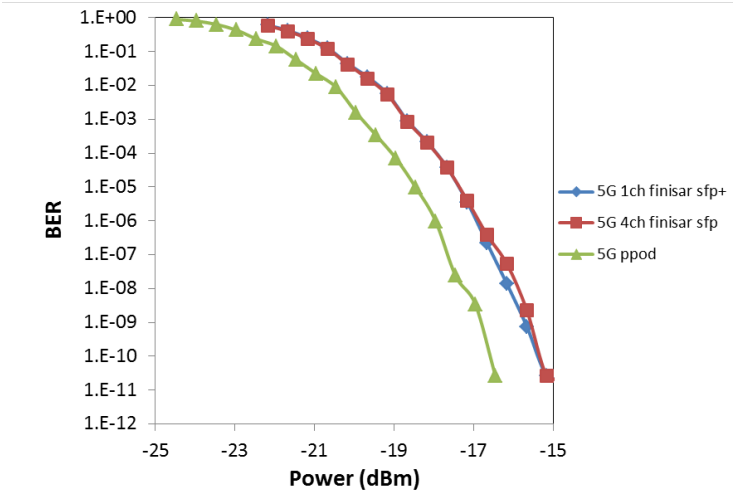
- This demonstration offers up to 8 x 10Gbps parallel optical transmission over 150 meters.
  - Limited by the HTG S4GT EVM hardware placement
- The FPGAs (Stratix II GX/Stratix IV GT or both) send and receive PRBS7/23 streams to the optical modules SFP+, QSFP+ and PPOD.
- FPGA resource utilization by the transceivers is low due to hardware dedication
- Reference clock inputs provided by off board clock synthesizer. Jitter performance limited by FPGA internal PLL
- The eye diagram indicates minimal configuration impact on performance. Default configuration at 10Gbps are used in this demonstration
- Error free over 30 minutes are achieved on all optical links.

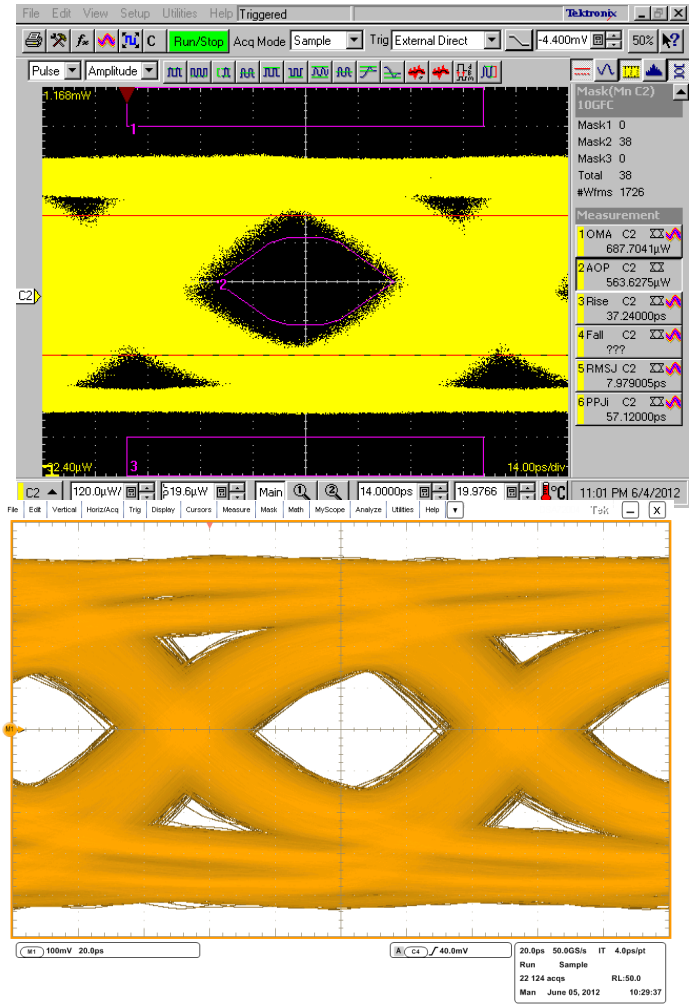


Flow Status	Successful - Mon Jun 04 11:37:50 2012
Quartus II 32-bit Version	11.1 Build 216 11/23/2011 SP 1 SJ Full Version
Revision Name	vbert_s4gt
Top-level Entity Name	vbert_s4gt
Family	Stratix IV
Device	EP4S100G2F40I2
Timing Models	Final
Logic utilization	3 %
Combinational ALUTs	2,129 / 182,400 (1 %)
Memory ALUTs	0 / 91,200 (0 %)
Dedicated logic registers	6,192 / 182,400 (3 %)
Total registers	6192
Total pins	37 / 798 (5 %)
Total virtual pins	0
Total block memory bits	204,288 / 14,625,792 (1 %)
DSP block 18-bit elements	0 / 1,288 (0 %)
Total GXB Receiver Channel PCS	4 / 24 (17 %)
Total GXB Receiver Channel PMA	4 / 36 (11 %)
Total GXB Transmitter Channel PCS	4 / 24 (17 %)
Total GXB Transmitter Channel PMA	4 / 36 (11 %)
Total PLLs	0 / 8 (0 %)
Total DLLs	0 / 4 (0 %)

Test results

- Electrical signal of the SMA wired channels and optical signal of the SMA driven transceivers are measured with oscilloscope.
- Signal of the FMC driven channels are not measured due to access difficulty of the electrical contacts and the requirement of trigger by sampling scopes
- BER vs. OMA (optical modulation amplitude) measured with automated LabVIEW routine
- The BER measurement of a number of optical channels matches among FPGA EVMs and the sensitivity specification of the optical receivers. Therefore the system does not introduce any performance degradation





10G electrical eye of FPGA output and 10G optical eye of TRx output

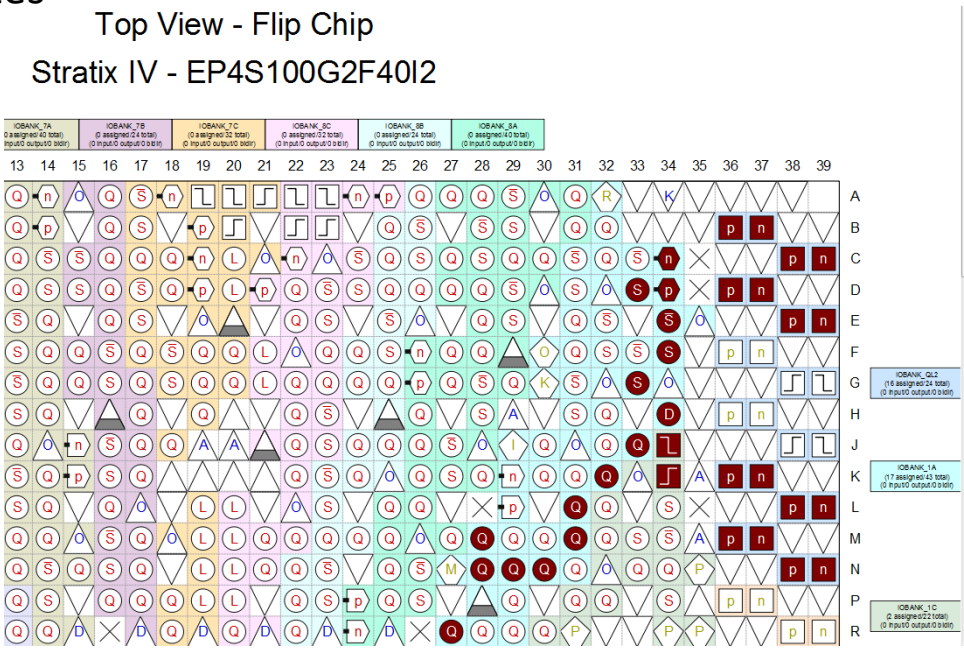
The eye quality is degraded because no direct pll clk signal is available from the FPGA EVM to be used for trigger

FPGA crosstalk

- Literature reported crosstalk effects in FPGA transceivers up to 20ps BUJ, which translates into ~0.9dB extra power penalty at 10G (< 0.1dB at 5G)

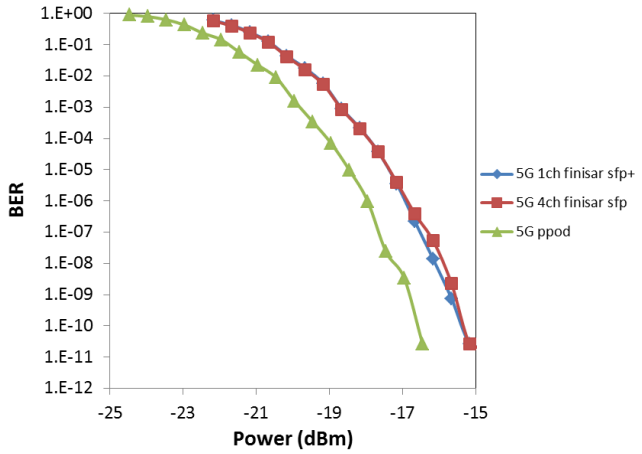
- Source of crosstalk likely from
  - On board crosstalk via inductive coupling
  - On chip crosstalk via synchronous switching noise

- Stratix IV GT EVM on board SMAs transceivers are tested
- The four transmitters were located in one quad, one victim and three aggressors
- 10Gbps PRBS 7 & 23
- Output differential voltage set at 800mV
- No Tx emphasis is turned on



FPGA crosstalk

5G baseline PRBS7			5G victim prbs7, aggressors pbrs23	
RJ (RMS)	1.8 ps		RJ (RMS)	1.9 ps
DJ (Pk-Pk)	21.8 ps		DJ (Pk-Pk)	23.9 ps
TJ (Pk-Pk)	43.1 ps		TJ (Pk-Pk)	45.2 ps
10G baseline PRBS7			10G victim prbs7, aggressors pbrs23	
RJ (RMS)	1.4 ps		RJ (RMS)	1.3 ps
DJ (Pk-Pk)	40.7 ps		DJ (Pk-Pk)	42.2 ps
TJ (Pk-Pk)	55.9 ps		TJ (Pk-Pk)	56.2 ps
5G baseline PRBS23			5G victim prbs23, aggressors pbrs7	
RJ (RMS)	2.4 ps		RJ (RMS)	2.5 ps
DJ (Pk-Pk)	16.4 ps		DJ (Pk-Pk)	16.5 ps
TJ (Pk-Pk)	46.1 ps		TJ (Pk-Pk)	46.9 ps
10G baseline PRBS23			10G victim prbs23, aggressors pbrs7	
RJ (RMS)	2.1 ps		RJ (RMS)	2.2 ps
DJ (Pk-Pk)	23.0 ps		DJ (Pk-Pk)	24.9 ps
TJ (Pk-Pk)	48.4 ps		TJ (Pk-Pk)	50.8 ps



No significant crosstalk effect was observed

Future work

- Contact board vendor with regard to hardware constraint
- Investigate the guideline to optimize transceiver instantiation
- Repeat this process on new device families and test boards (Kintex-7) for ATLAS LAr.
- Implement framing protocols and study timing performance, again for ATLAS LAr.

Summary

- Demonstrated the implementation of a multi-channel, 10Gbps/channel BERT based on Stratix IV
- FMC based plug-in module cards are built and optical transceiver links are tested
- The FPGA transceivers and one of the parallel optical transceivers show negligible crosstalk affecting on power penalty

Thanks for your attention