# MP7 – An Avago MiniPOD Application

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#### Andy Rose, Imperial

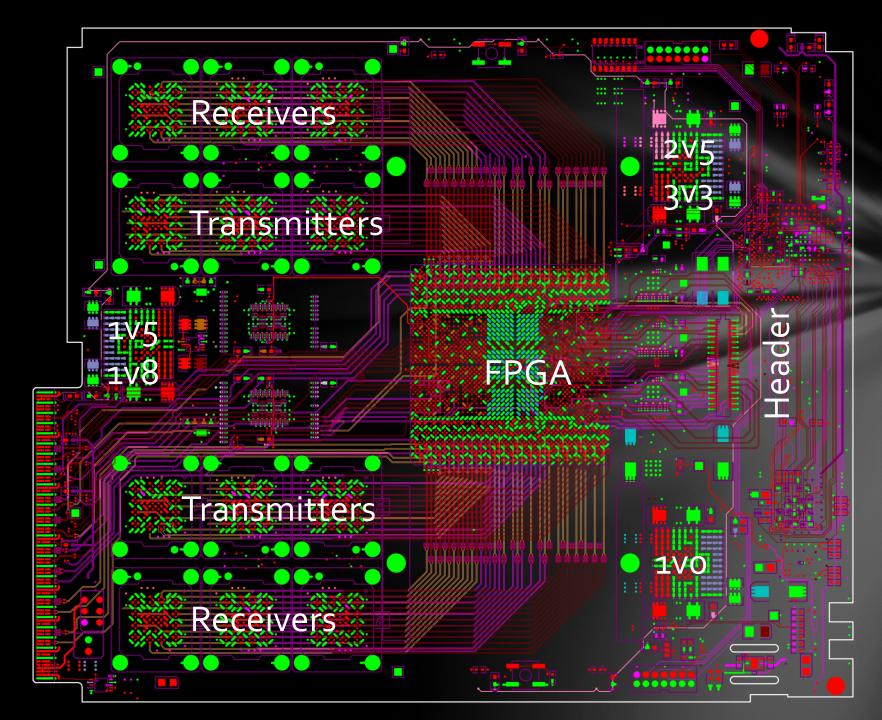
#### MP7

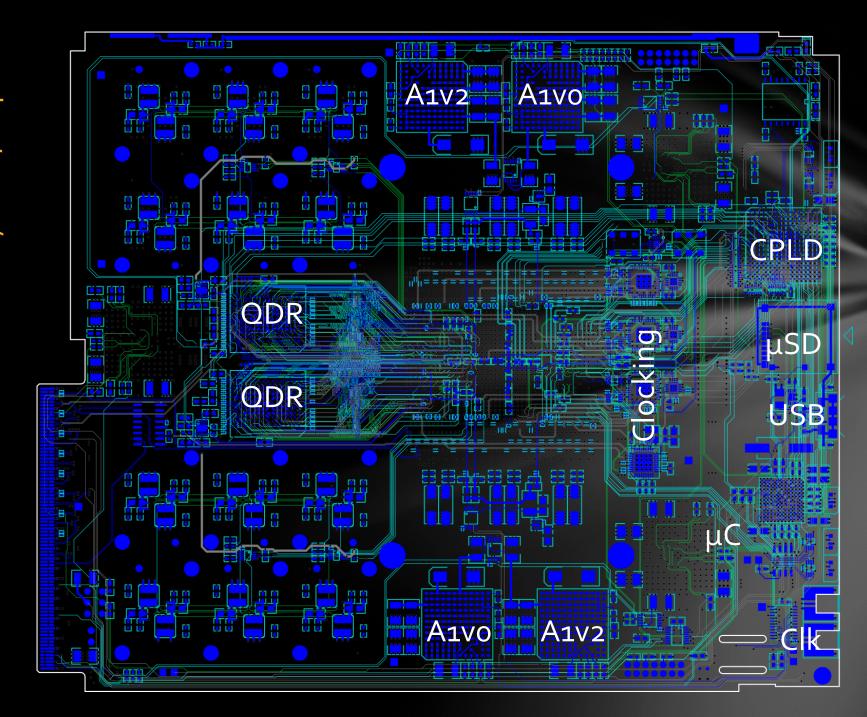
- Full-height, double-width AMC card
- Xilinx Virtex 7 1.6Tb/s of SerDes links
- 6× 12-channel, >10 Gb/s
- 72 bidirectional channels Rx & Tx = 720 Gb/s



Mini-T5-R2
AMC Card, but with Avago PPODs
Rx = 160 Gb/s
Tx = 100 Gb/s

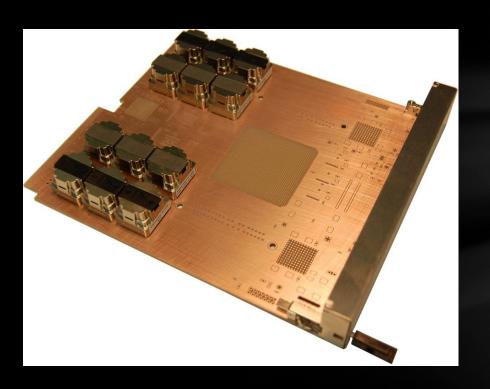


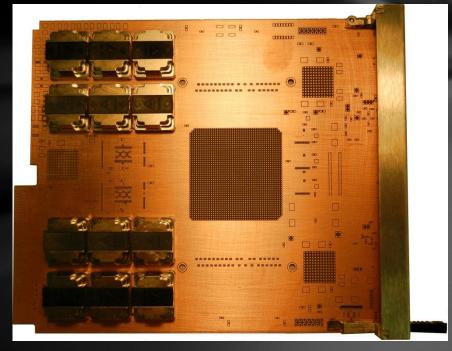




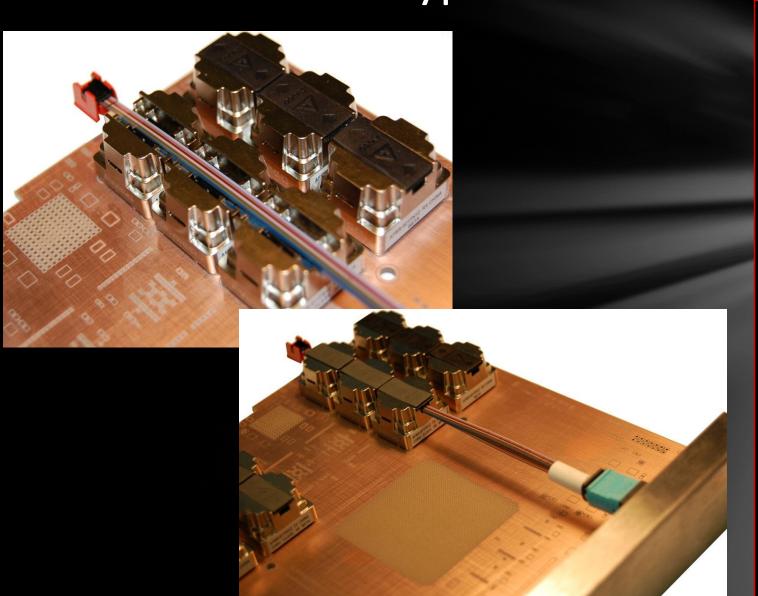
## Mechanical Prototype

No electrical connections, just surfaces and mounting-holes





# Mechanical Prototype

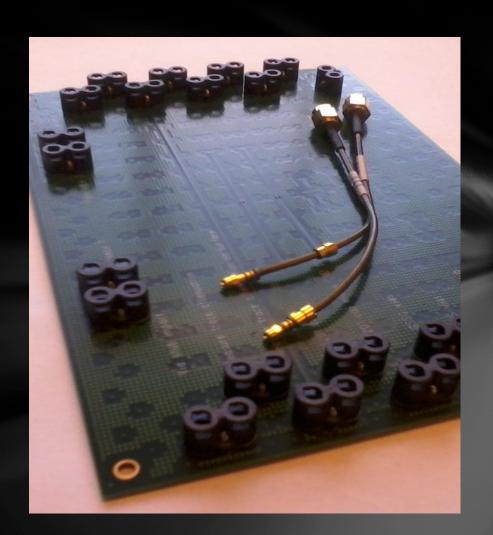




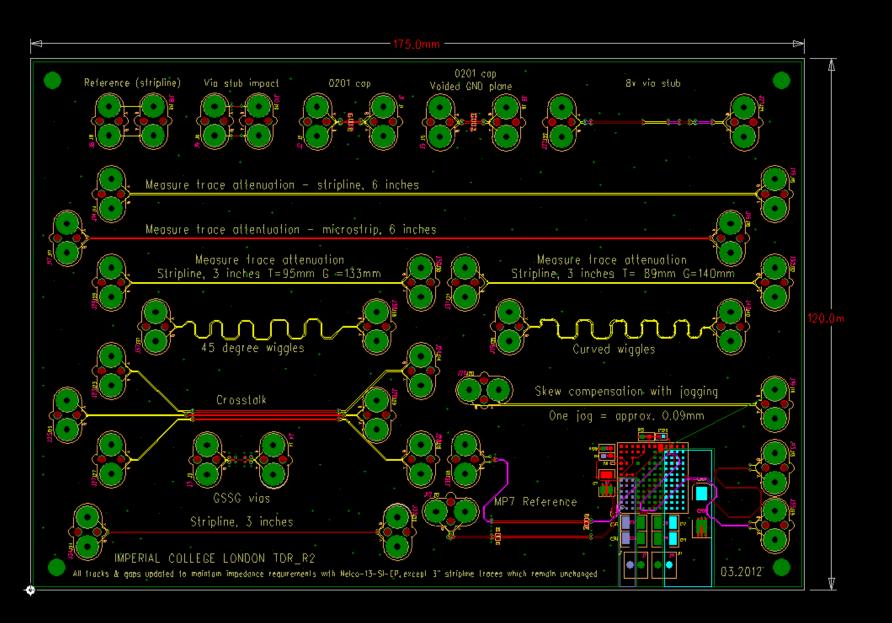
#### **Test Cards**

#### Many different test structures:

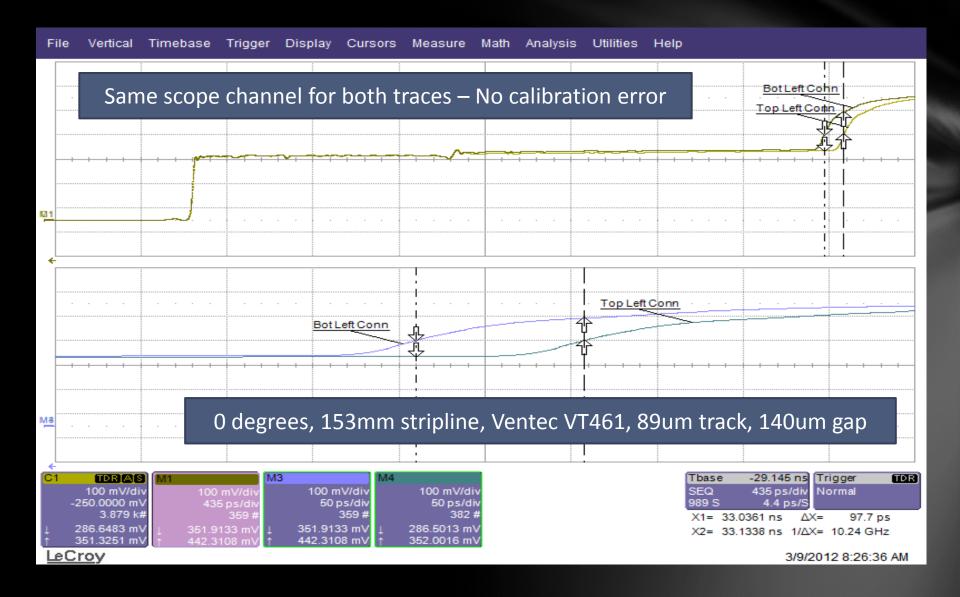
- Bend tracks with 45 degrees or curves
- Track to weave angle
- Capacitor void impact
- Via impact
- Immunity to switching power supply noise
- Ground-Signal-Signal-Ground
- Material impact



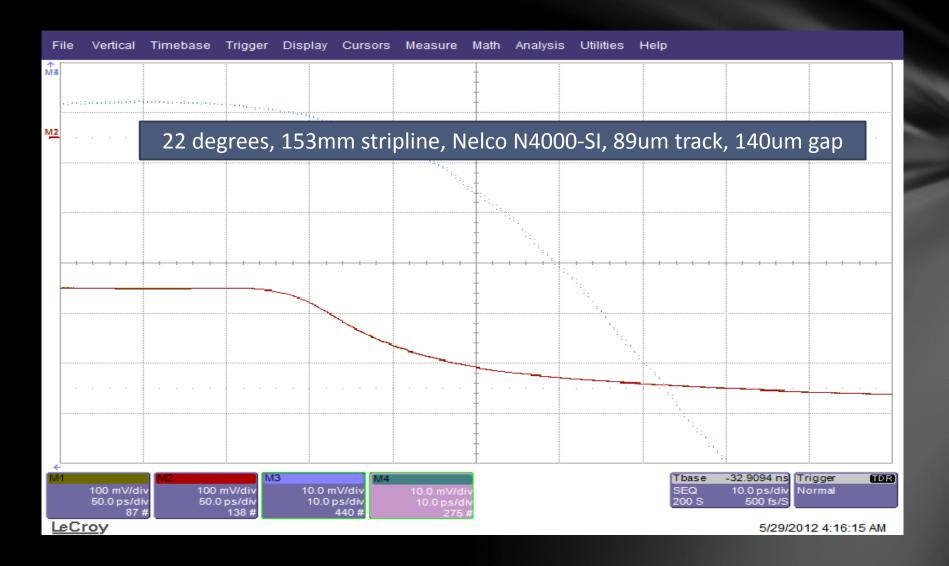
## Test Card



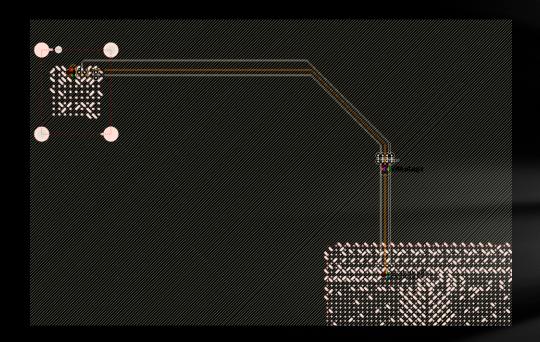
#### Skew: Test Card 0



### Skew: Test Card 2

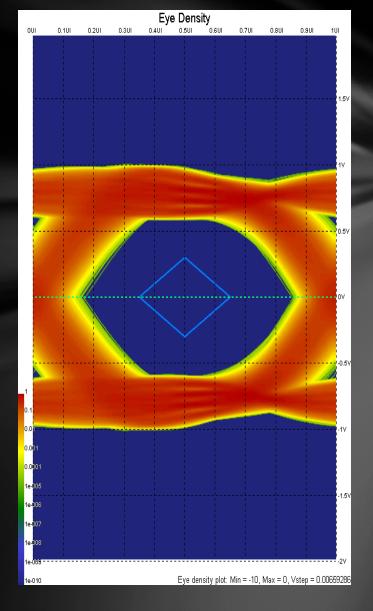


## Simulations



Stressed Eye – Based on SFP+ Spec

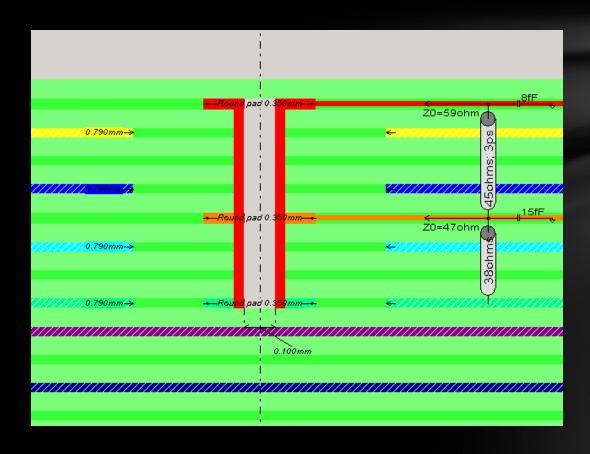
128 bit per UI
1 million UI
8B/10B
PreEmp = 5 (100)
AMI-Dj-min = 5ps
AMI-Dj-max = 15ps
AMI-Sigma = 2.3ps rms



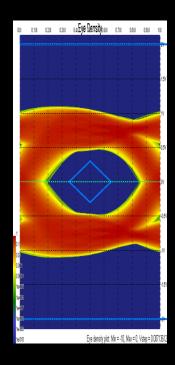
## Via impedance..

Via length, excluding stub < 0.4mm

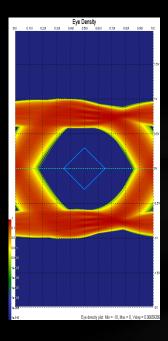
Signal takes < 3ps to traverse via



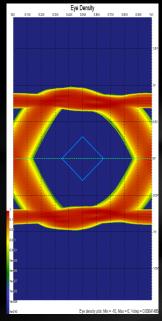
## Stressed Eye & Via Inductance



Diff Imp = 62



0.35mm pad, 0.15mm real drill Diff Imp = 77



0.20mm pad, 0.11mm real drill Diff Imp = 104

128 bit per UI 1 million UI 8B/10B

PreEmp = 5 (100)

Not buildable!

