LOC and VCSEL Drivers

Opto Workshop

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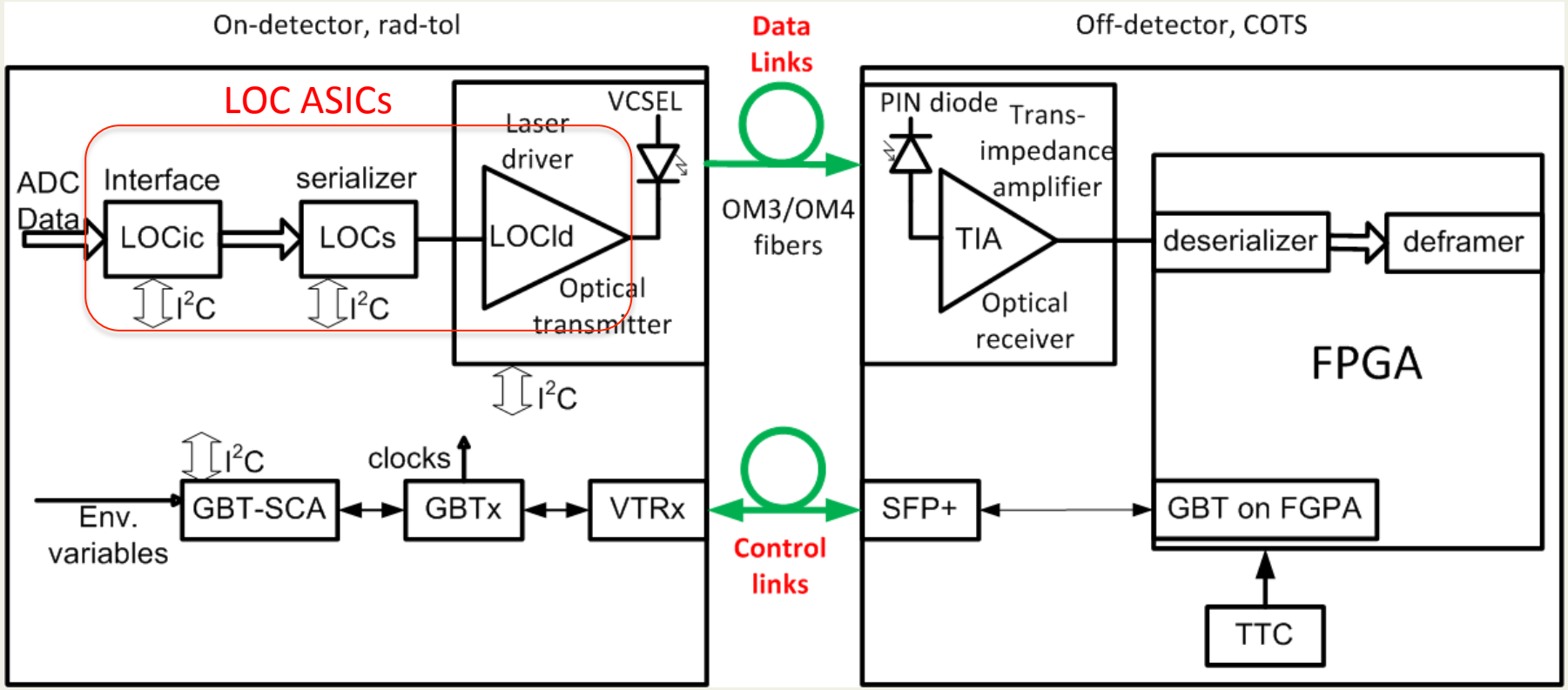
SMU PHYSICS LAB
Datao Gong
Andy Liu
Annie Xiang
Kent Liu
Jingbo Ye

Outline

1. The LOC ASICs.
   - LOCic, the interface to the serializer.
   - LOCs, the serializer.
   - LOCld, VCSEL drivers.
2. Status and plan for the LOCic.
   - FPGA implementation for ATLAS LAr.
   - ASIC implementation for ATLAS LAr.
3. Status and plan for the LOCs.
   - LOCs1, 5 Gbps 16:1 serializer.
   - LOCs2, 8 Gbps, 16:1, 2 lane serializer.
   - LOCs for ATLAS LAr.
4. Status and plan for the LOCld.
   - LOCld1: single channel, 50 ohm load, VCSEL driver.
   - LOCld4: 4 channel, open drain, VCSEL driver.
   - LOCld for ATLAS LAr.

The LOC ASICs



LOCic is an application specific interface chip or design block. It also frames and prepares (scrambling, error checking code, etc) the transmission data.
LOCs is a generic serializer in single channel or multi-channel (sharing the clock unit) versions.
LOCld is a VCSEL driver, again has single channel 50 ohm and open-drain multi-channel versions.

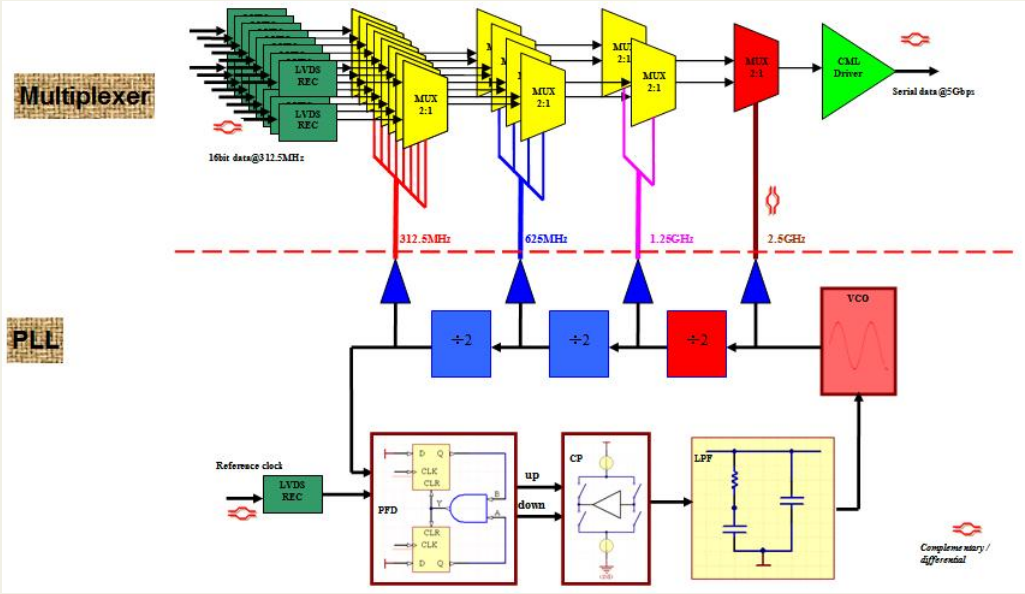
Status and plan for the LOCic

1. Specifically designed for ATLAS LAr phase-1 upgrade.
   - Provide a low overhead frame for the serial output ADC.
   - The frame can quickly re-lock at the receiving end after an SEU induced link synch loss.
   - DC balance data.
   - Add other specific information such as the BCID.
   - error check and possible error correction code.
2. Currently implemented in FPGA.
   - Check the design logic.
   - Provide an FPGA based reference link design (with the embedded SerDes).
   - Provide a tool (with VBERT) for rad-tests.
3. Will be implemented in ASIC.
   - To meet the rad-tol requirement.
   - May exit as a design block that is integrated with the serializer, or exit as packaged chip should generic applications be found.

Status and plan for the LOCs

LOCs1.

- Started by copying the GOL, with great help from Paulo.
- Prototyped in 2009 and reported in 2010.
- A 16:1 5 Gbps serializer based on a ring oscillator PLL.



Amplitude (V)	1.16 ±0.03
Rise time (ps)	52.0 ±0.9
Fall time (ps)	51.9 ± 1.0
Total Jitter @ BER 10^{-12} (ps)	61.6 ± 6.9
Random Jitter (ps)	2.6 ±0.6
Total DJ (ps)	33.4 ±6.7
DJ: Periodic (ps)	3.0 ± 2.3
DJ: ISI (ps)	3.0 ± 2.3
DJ: Duty cycle (ps)	15.2 ± 3.8

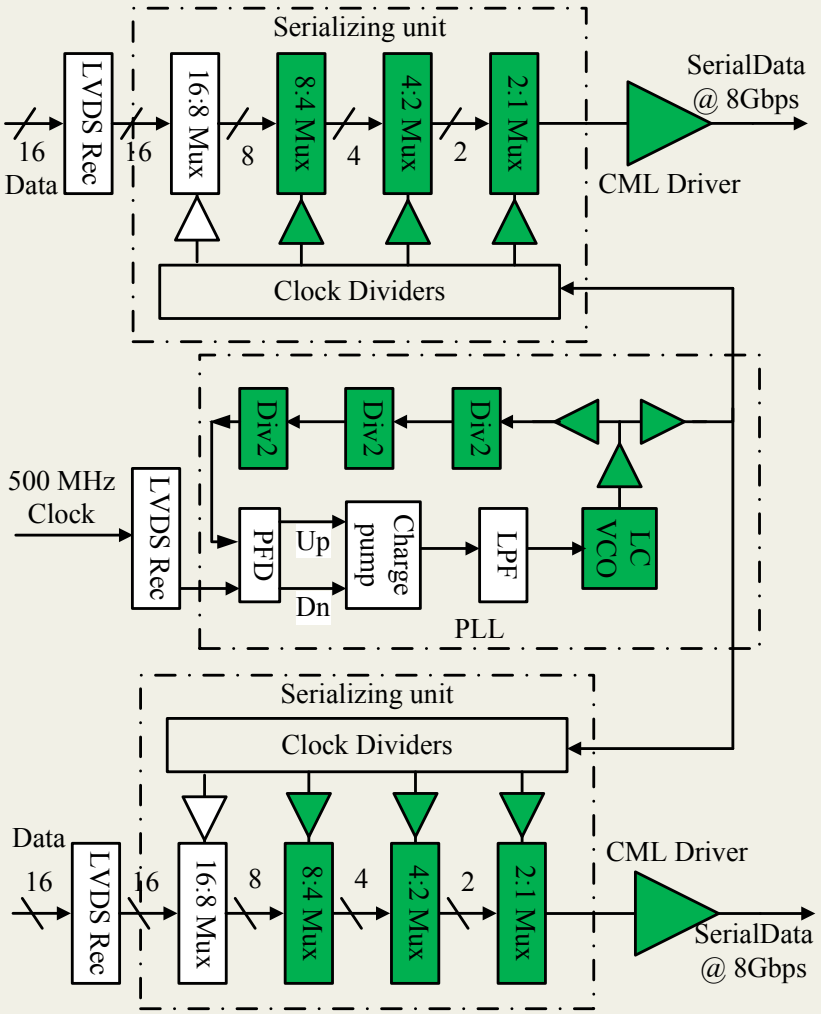
Status and plan for the LOCs

LOCs2.

- 2-lane, 16:1, 8 Gbps, sharing an LC-PLL.
- 1.5 years to design because of high speed; will be submitted June 15.

- Process: the same as LOCs1
- Two channels, each with design speed of 8 Gbps, tunable 6.9 – 8.7 Gbps
- Power dissipation: 1.2 W, or 75 mW/Gbps
- Latency: 8 ns

- Green colored: new designs
- White: adopted and improved from LOCs1



Status and plan for the LOCs

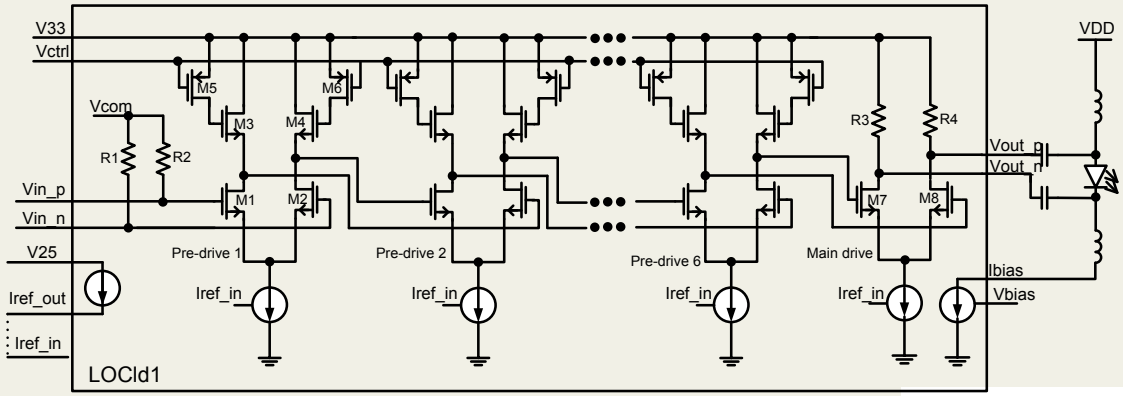
LOCs specifically for ATLAS LAr upgrade.

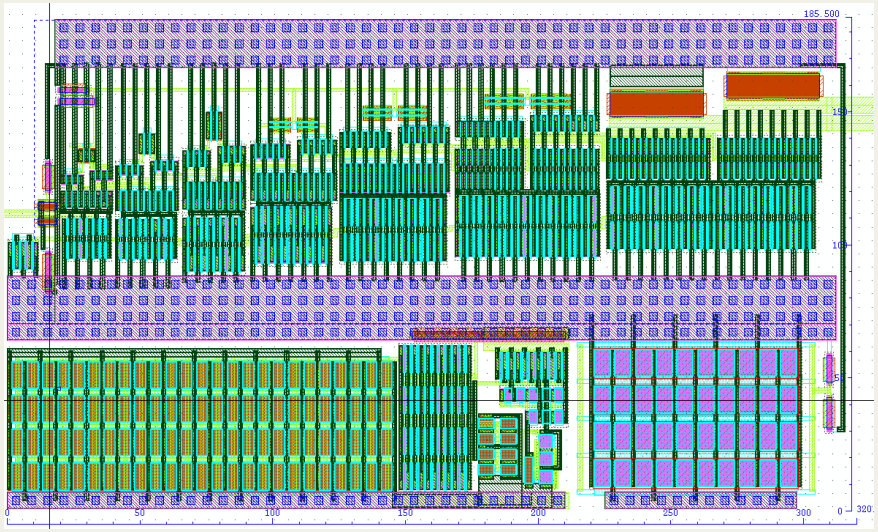
- There will be a specially designed ASIC for ATLAS LAr phase-1 upgrade.
- This ASIC will include LOCic and LOCs into one chip for compactness and low power.
- The serial data rate will be from 4.2 Gbps to 5.6 Gbps.
- This will be a complete chip with control and configuration interfaces.
- We will need to investigate packaging options.

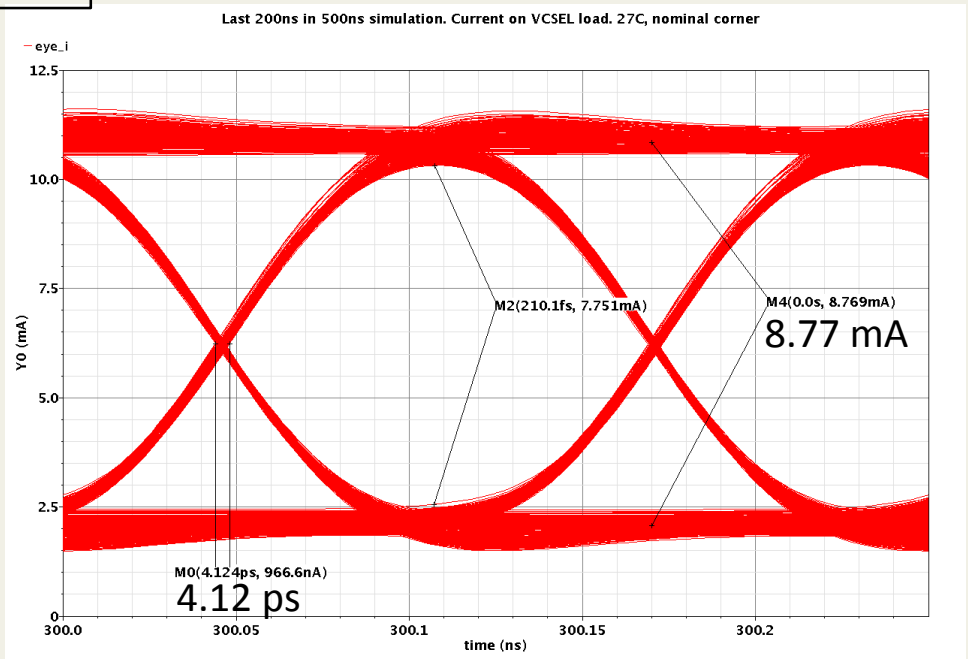
Status and plan for the LOCld

LOCld1.

- Minimum input: 2 mA (100 ohm) differential peak to peak.
- Minimum output: 6 mA, 50 ohm load.



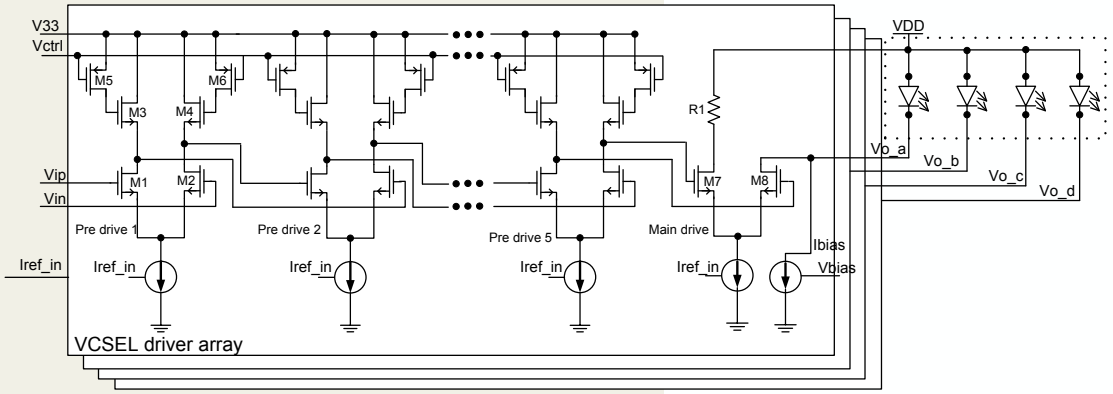


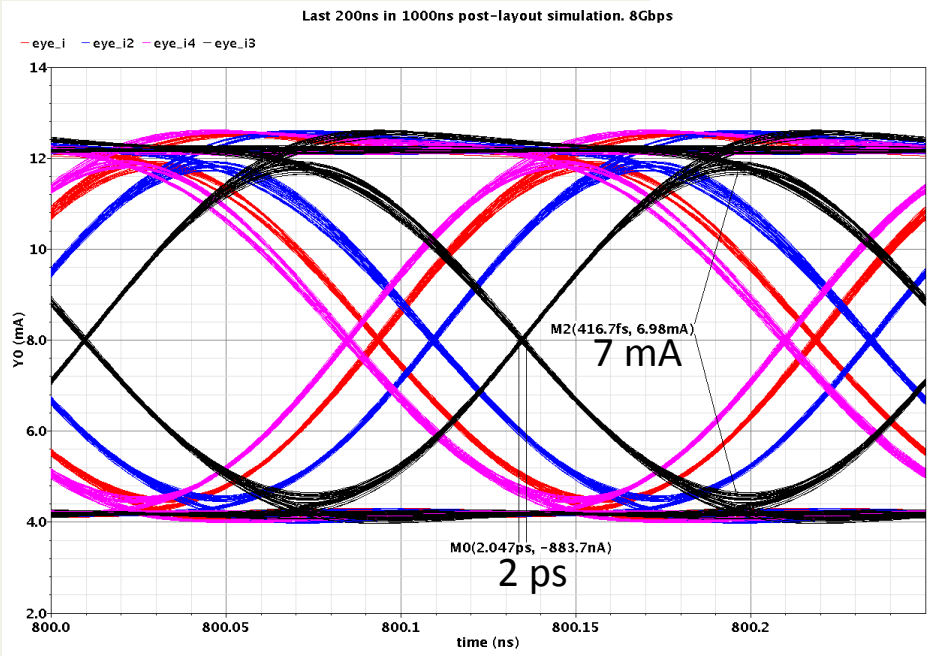


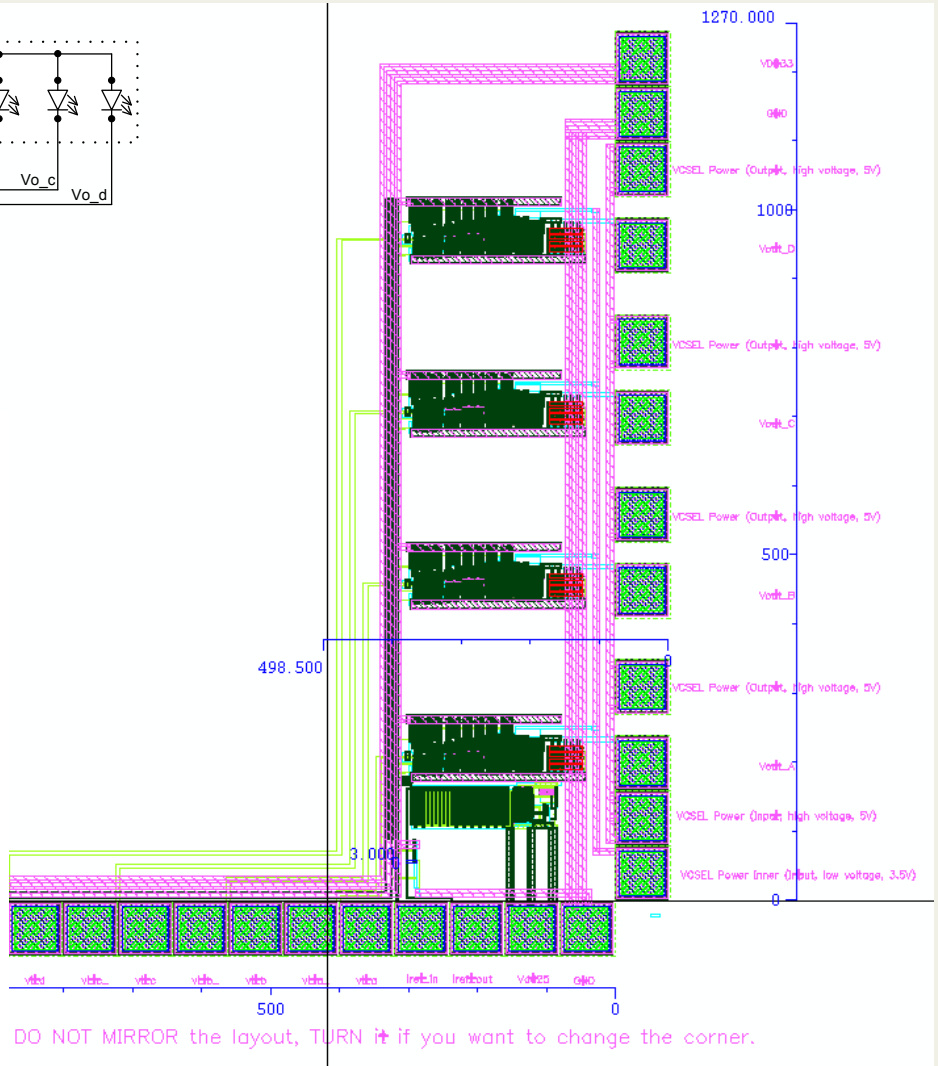
Status and plan for the LOCld

LOCld4.

- 4 channel array prototype.
- Open-drain design.







Status

1. LOCs2, LOCld2 and LOCld4 will be prototyped on June 15.
2. Design documents and specs can be found in EDMS:

   LOCs2 Design Document, https://edms.cern.ch/document/1209497/1.01
   LOCs2 specification, https://edms.cern.ch/document/1209501/1.0
   LOCld Design Document, https://edms.cern.ch/document/1209499/2.00
   LOCld specification, https://edms.cern.ch/document/1209500/1.0