GBT Project Status

Paulo Moreira

CERN

08 June 2012

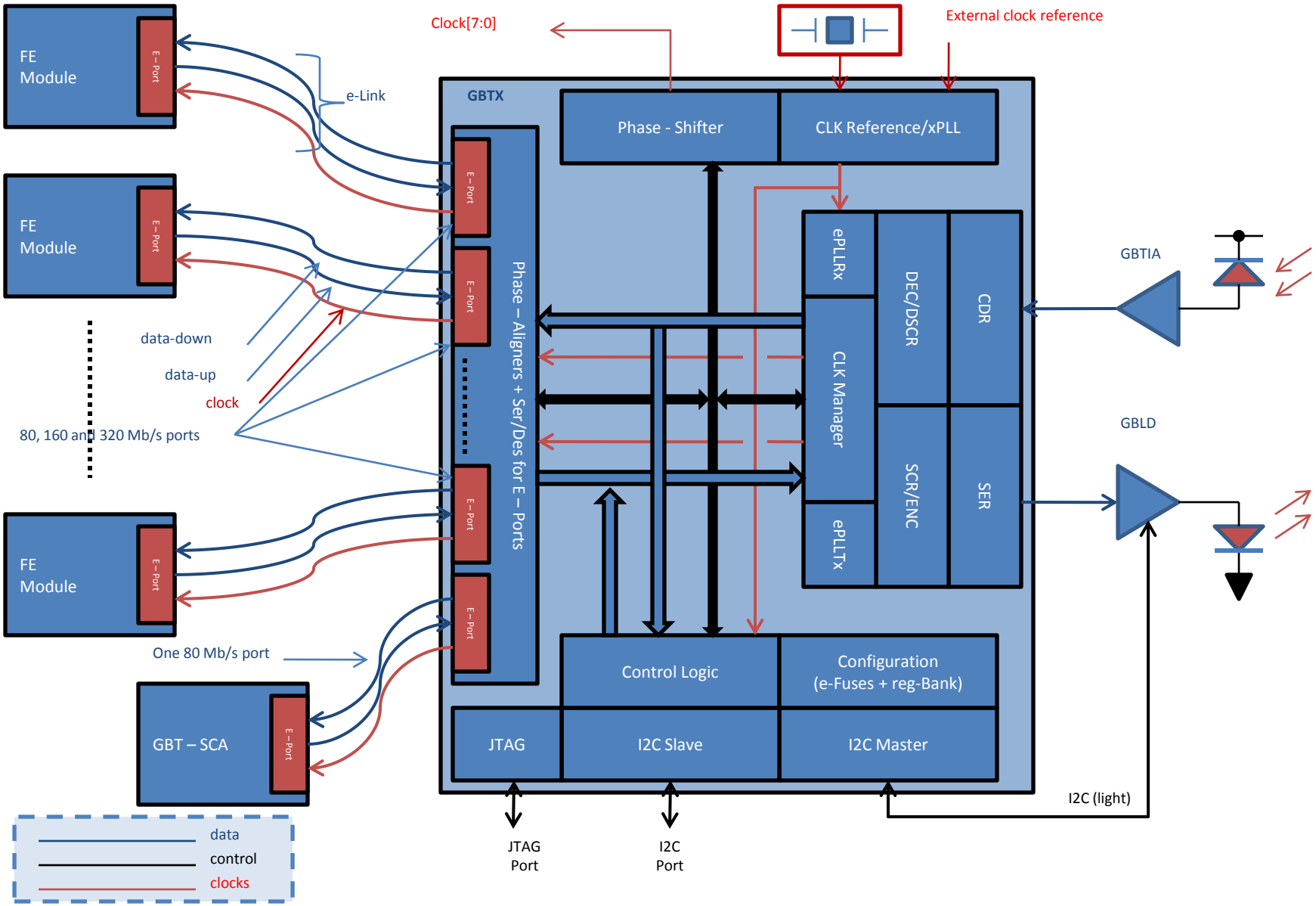
GBT Project

- *Sophie Baron*
- *Sandro Bonacini*
- *Pedro Cardoso*
- *Jorgen Christiansen*
- *Ozgur Cobanoglu*
- *Federico Faccio*
- *Rui Francisco*
- *Tullio Grassi*
- *Ping Gui*
- *Kostas Kloukinas*
- *Alessandro Marchioro*
- Giovanni Mazza
- *Mohsine Menouni*
- *Paulo Moreira*
- *Christian Paillard*
- *Karolina Poltorak*
- *David Porret*
- *Angelo Rivetti*
- *Filip Tavernier*
- *Guoying Wu*
- *Ken Wyllie*

Outline

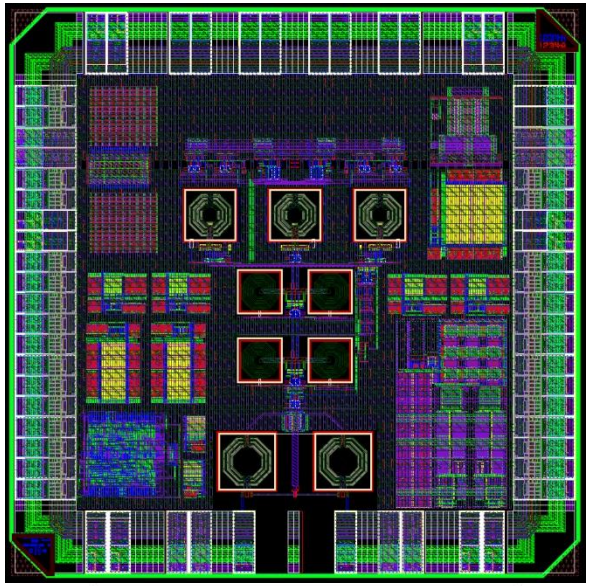
- The GBT system
- GBLD
- GBTIA
- GBTX:
  - “New” features
  - Status
- GBT-SCA
- GBT Project Future

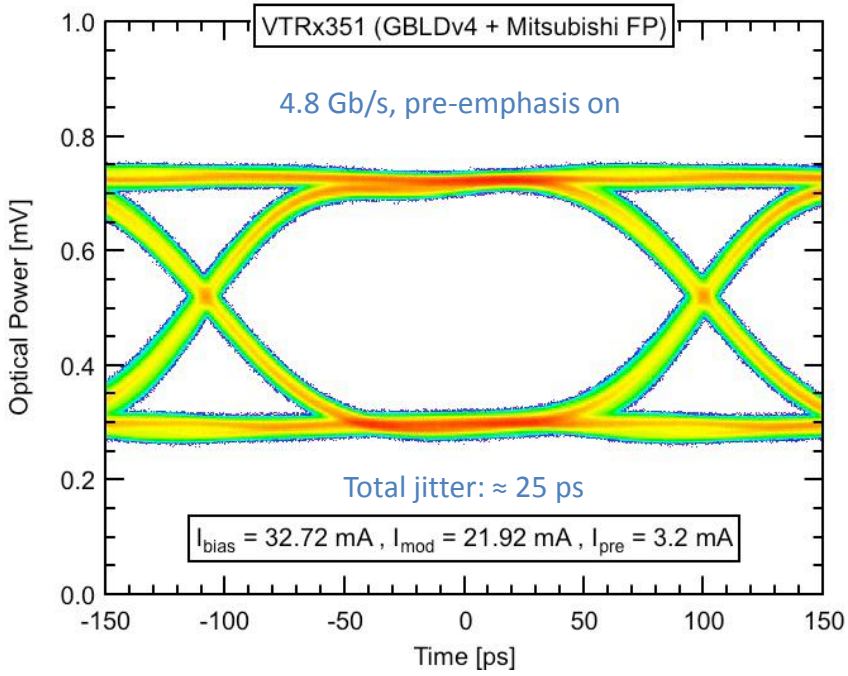
GBT System


FE Module
E – Port
e-Link
Clock[7:0]
External clock reference
GBTX
Phase - Shifter
CLK Reference/xPLL
Phase – Aligners + Ser/Des for E – Ports
ePLLRx
CLK Manager
ePLLTx
DEC/DSCR
SCR/ENC
CDR
SER
GBTIA
GBLD
data-down
data-up
clock
80, 160 and 320 Mb/s ports
One 80 Mb/s port
GBT – SCA
Control Logic
Configuration
(e-Fuses + reg-Bank)
JTAG
I2C Slave
I2C Master
I2C (light)
JTAG
Port
I2C
Port
data
control
clocks

GBLD Status

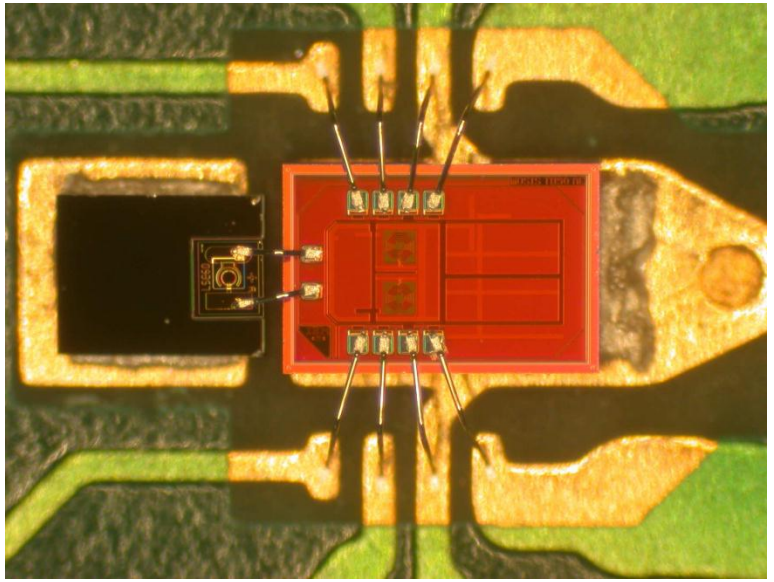
- GBLD V4 performs according to specs (+):
  - Modulator
  - Laser bias
  - Radiation hardness proven!
- Successfully integrated in the versatile link transceiver:
  - VTRx451
  - (F. Vasey presentation today)
- The ASIC is production ready!
- Chips currently available in small quantities: ≈ 120 chips
- Small “production” run
  - August: ≈ 80 chips

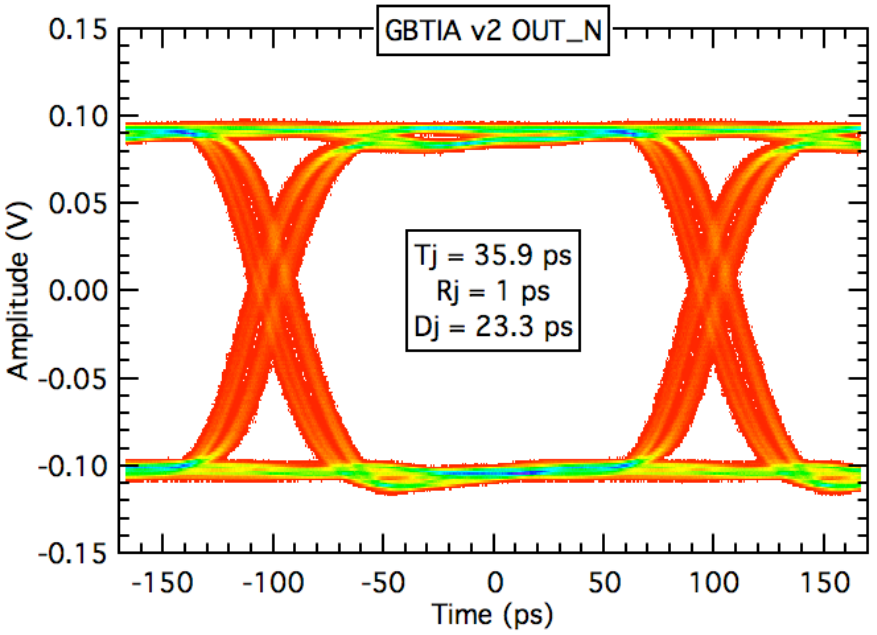




GBTIA Status

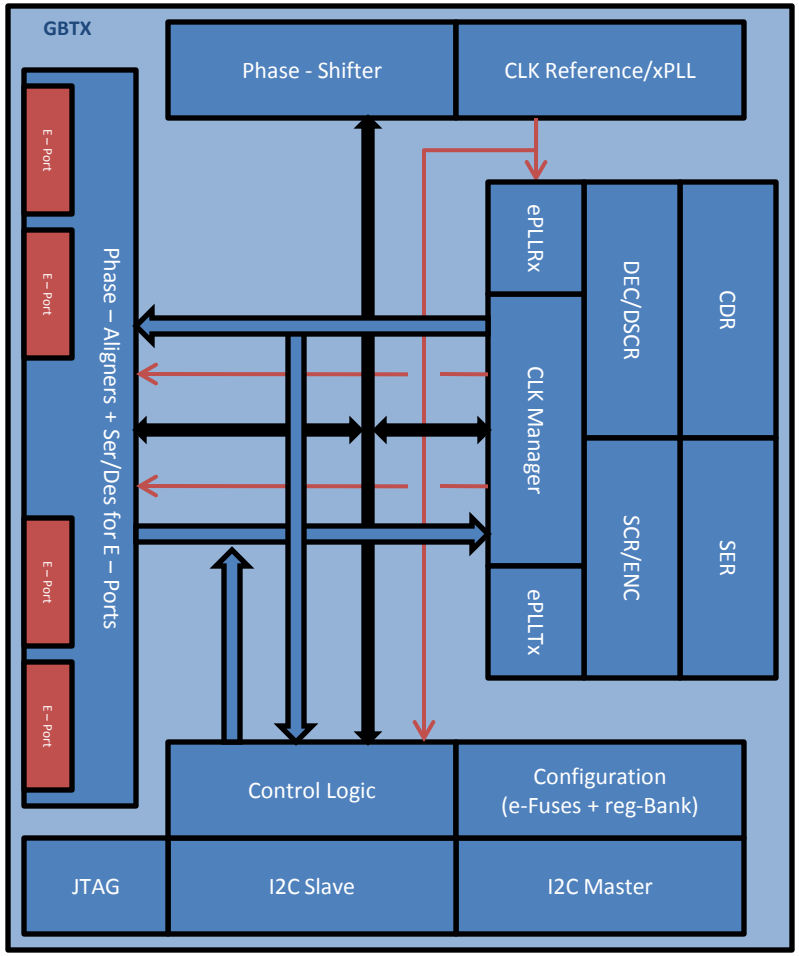
- First version fabricated in 2008:
  - Fully functional
  - Performance according to specifications (+)
  - Radiation hardness proven!
- New version fabricated in 2011:
  - New pad layout
  - Received Signal Strength Indication (RSSI)
    - To facilitate optical fiber/PIN-diode alignment.
  - Higher reversed bias voltage for the PIN-diode
  - Voltage regulator 2.5 V to 2.0 V
  - Tests results reveal performance similar to the first version
- Chips currently available in small quantities: ≈ 240 chips (bare dye)
- Small "production" run:
  - August 2012, ≈ 80 chips





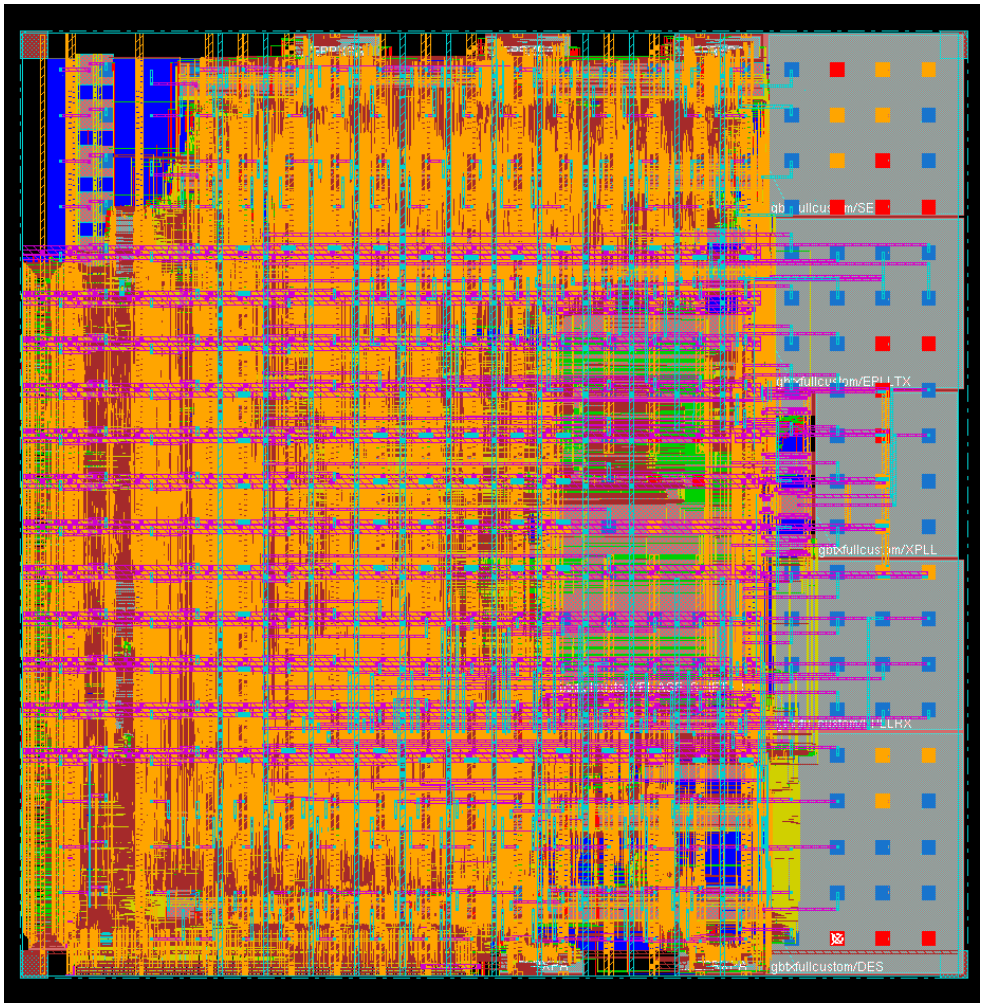
GBTX: New features

- The GBTX now supports three frame types:
  - "GBT" Frame
  - "Wide Bus" Frame
  - "8B/10B" Frame
- "Wide Bus" and "8B/10B"frames are only supported for the uplink
  - The downlink always uses the "GBT" frame.
- "Wide Bus" Mode:
  - Uplink data scrambled
  - No FEC
  - User bandwidth: 4.48 Gb/s
- "8B/10B" Mode
  - Downlink data 8B/10B encoded
  - No FEC
  - User bandwidth: 3.52 Gb/s



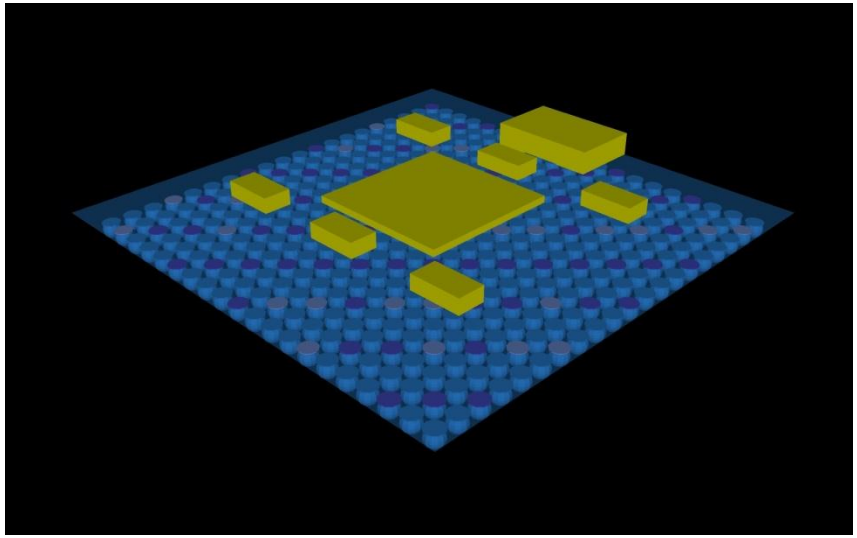
GBTX - Status

- GBTX team currently hard working towards the:
  - 6th of August MOSIS submission
  - Layout work very close to completion
  - Mainly verification work left to be done!
- Preparation of the test-setup currently running in parallel with the ASIC design
- Forecast:
  - Submission:
    - 6th of August 2012
  - Chips back from foundry:
    - November 2012
  - Chips packaged
    - Feb 2013
  - Prototypes available for distribution:
    - May 2013



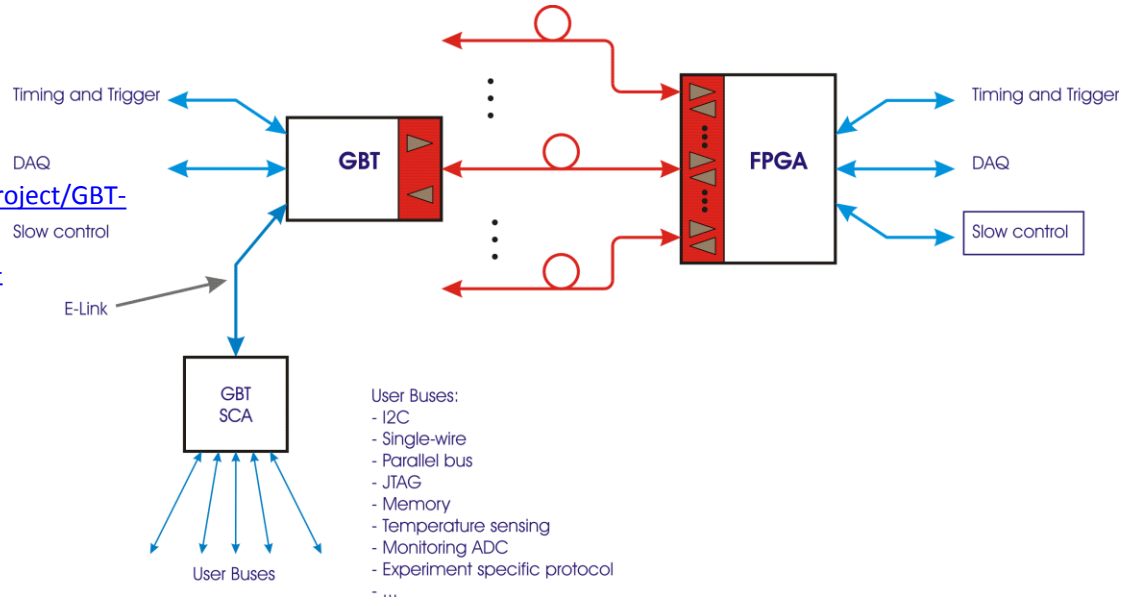
GBTX - Package

- Package:
  - 20 × 20 ball array
  - 0.8 mm pitch
  - Size: 17 mm × 17 mm
- Package:
  - Manufactured by ASE:
  - Integrate the decoupling capacitors
  - Integrate the XTAL
- Package development by ASE has already started



GBT – SCA Status

- Dedicated to slow control functions
  - Interfaces with the GBTX using a dedicated E-link port
    - Standard e-Ports in the 80 Mb/s can be used as well
  - Communicates with the control room using a protocol carried (transparently) by the GBT
- Implements multiple protocol busses and functions:
  - I2C, JTAG, PIA, etc…
- Implements environment monitoring functions:
  - Temperature sensing
  - Multi-channel ADC
  - DAC
- Specifications ready:
  - User Manual: https://espace.cern.ch/GBT-Project/GBT-SCA/Specification/GBT-SCA%20v5.0.docx
  - Technical Brief: https://espace.cern.ch/GBT-Project/GBT-SCA/Specification/GBT-SCA%20technical%20brief%20v0.2.docx
- Under development
  - RTL code
  - DAC
  - ADC
  - Submission date
    - 8th of February 2012
  - Chips packaged:
    - May 2013
  - Prototypes available:
    - September 2013



GBT Project Future

- LpGBT: Low power GBT chip set
  - Reduce the GBT chipset power consumption to ~ ¼ (~500 mW)
  - Two "SERDES" ASICs:
    - Simple SERDES with reduced functionality
      - Low pin count and footprint (targeting tracker developments)
      - Simple parallel port
    - Full GBTX functionality
      - General purpose
      - E-Links
  - High bandwidth capability (option under consideration):
    - Downlink 4.8 Gb/s (as in the GBTX)
    - Uplink two modes: 4.8 and 9.6 Gb/s
      - E-Links double the bandwidth in the 10 Gb/s mode
  - Technology: 65 nm CMOS
    - LpGBT – SerDes
    - LpGBTX
    - LpGBLD will be very likely kept in 130 nm CMOS
- Serious development effort to start summer 2012
  - Target:
    - LpGBT – SerDes prototypes in 2015
    - LpGBTX prototypes in 2016

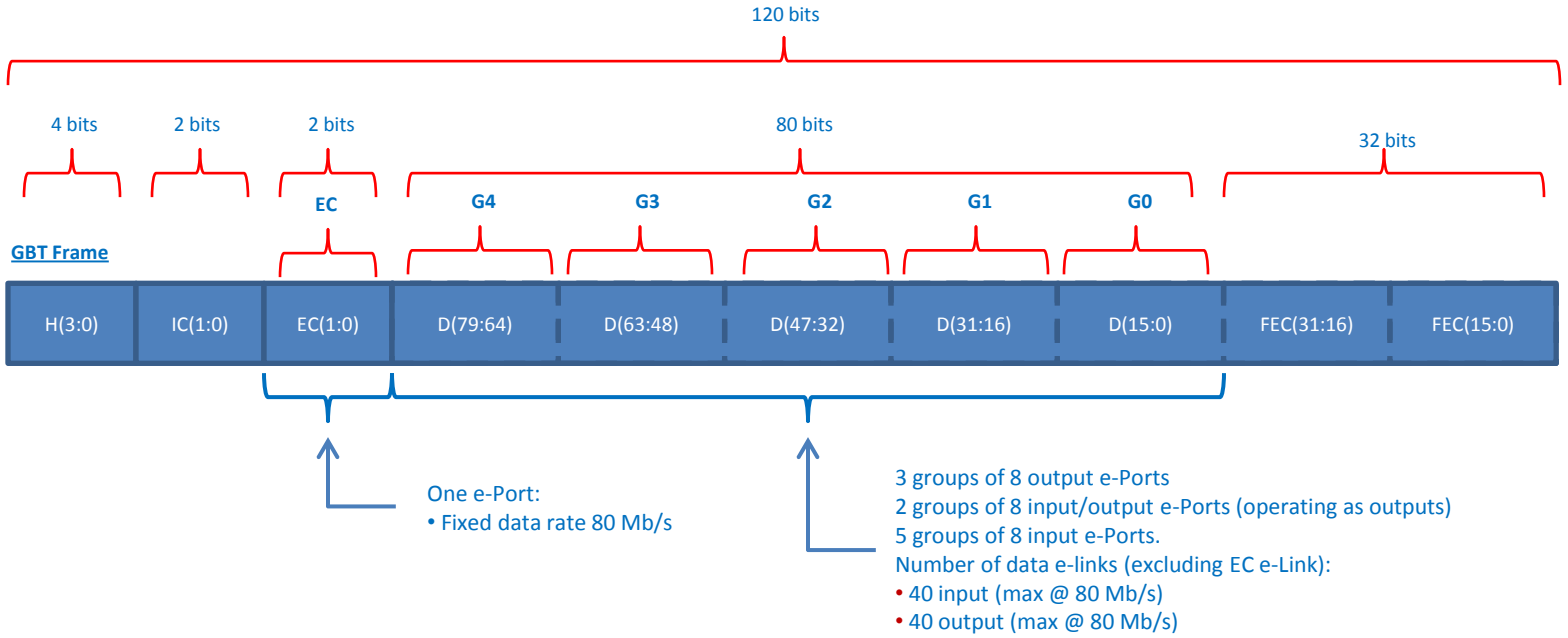
Backup Slides

- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides

- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides
- Backup Slides

GBT Mode

(For Up/Down-Links)



e-Ports to Frame Mapping in the GBT Mode

Uplink (GBT - Frame)

E-Link Data Rate: Up-Link			Group	Frame
80 Mb/s	160 Mb/s	320 Mb/s		
dIn[7:0]			0	FRMUP[47:32]
	dIn[6,4,2,0]			
		dIn[4,0]		
dIn[15:8]			1	FRMUP[63:48]
	dIn[14,12,10,8]			
		dIn[12,8]		
dIn[23:16]			2	FRMUP[79:64]
	dIn[22,20,18,16]			
		dIn[20,16]		
dIn[31:24]			3	FRMUP[95:80]
	dIn[30,28,26,24]			
		dIn[28,24]		
dIn[39:32]			4	FRMUP[111:96]
	dIn[38,36,34,32]			
		dIn[36,32]		

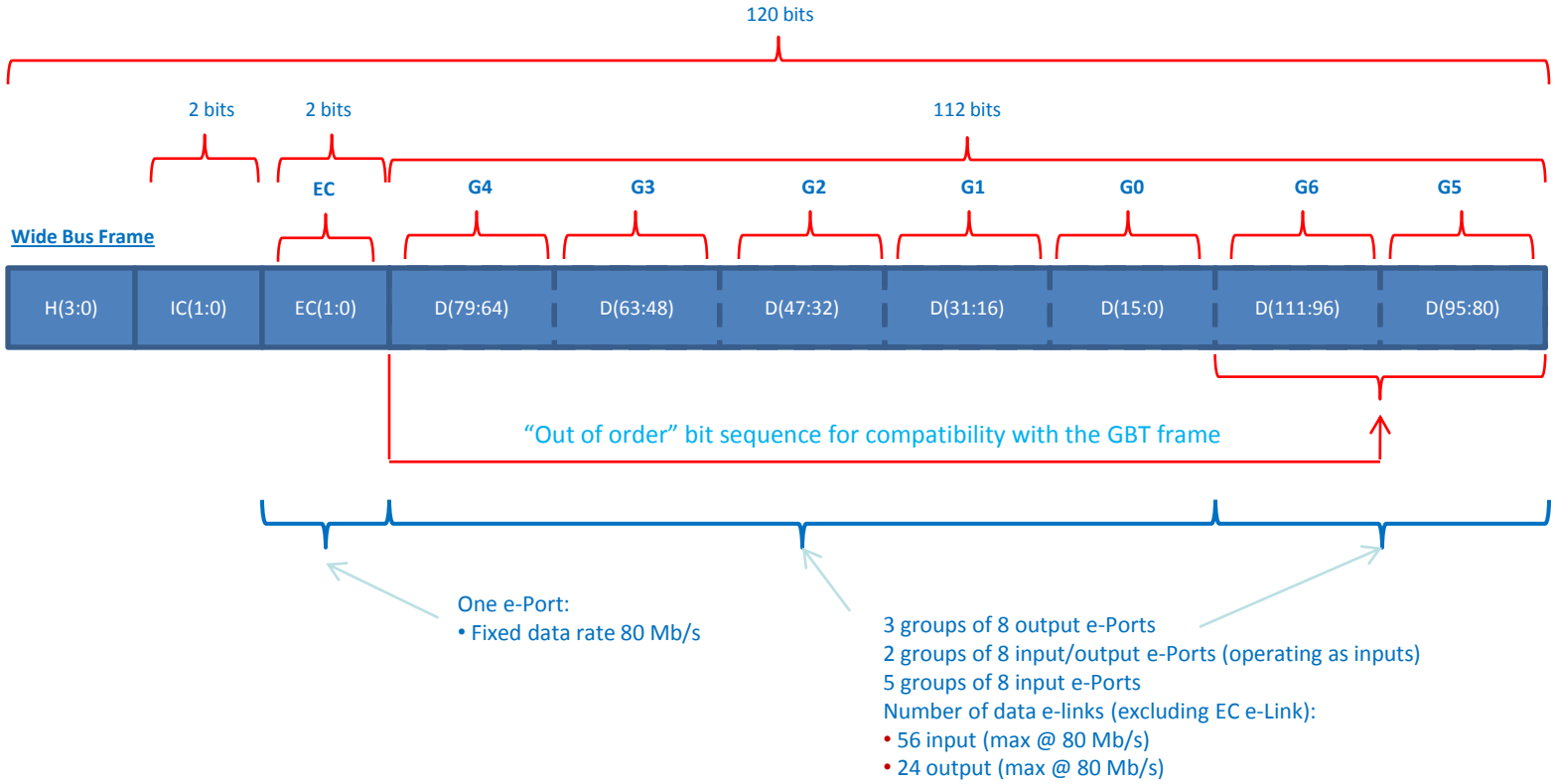
Downlink (GBT - Frame)

Frame	Group	E-Link Data Rate: Down-Link		
		80 Mb/s	160 Mb/s	320 Mb/s
FRMDWN[47:32]	0	dOut[7:0]		
			dOut[6,4,2,0]	
				dOut[4,0]
FRMDWN[63:48]	1	dOut[15:8]		
			dOut[14,12,10,8]	
				dOut[12,8]
FRMDWN[79:64]	2	dOut[23:16]		
			dOut[22,20,18,16]	
				dOut[20,16]
FRMDWN[95:80]	3	dOut[31:24]		
			dOut[30,28,26,24]	
				dOut[28,24]
FRMDWN[111:96]	4	dOut[39:32]		
			dOut[38,36,34,32]	
				dOut[36,32]

E-Link Data Rate	80 Mb/s	160 Mb/s	320 Mb/s
Max # of up-links:	40	20	10
Max # of down-links:	40	20	10

Wide Bus Mode

(Valid only for the Up-Link)



e-Ports to Frame Mapping in the GBT in the Wide Bus Mode

Uplink (Wide Bus Frame)

E-Link Data Rate: Up-Link			Group	Frame
80 Mb/s	160 Mb/s	320 Mb/s		
dIn[7:0]			0	FRMUP[47:32]
	dIn[6,4,2,0]			
		dIn[4,0]		
dIn[15:8]			1	FRMUP[63:48]
	dIn[14,12,10,8]			
		dIn[12,8]		
dIn[23:16]			2	FRMUP[79:64]
	dIn[22,20,18,16]			
		dIn[20,16]		
dIn[31:24]			3	FRMUP[95:80]
	dIn[30,28,26,24]			
		dIn[28,24]		
dIn[39:32]			4	FRMUP[111:96]
	dIn[38,36,34,32]			
		dIn[36,32]		
dOut[7:0]			5	FRMUP[15:0]
	dOut[7,5,3,1]			
		dOut[5,1]		
dOut[15:8]			6	FRMUP[31:16]
	dOut[15,13,11,9]			
		dOut[13,9]		

Downlink (GBT - Frame)

Frame	Group	E-Link Data Rate: Down-Link		
		80 Mb/s	160 Mb/s	320 Mb/s
FRMDWN[47:32]	0	n.a.		
			dOut[6,4,2,0]	
				dOut[4,0]
FRMDWN[63:48]	1	n.a.		
			dOut[14,12,10,8]	
				dOut[12,8]
FRMDWN[79:64]	2	dOut[23:16]		
			dOut[22,20,18,16]	
				dOut[20,16]
FRMDWN[95:80]	3	dOut[31:24]		
			dOut[30,28,26,24]	
				dOut[28,24]
FRMDWN[111:96]	4	dOut[39:32]		
			dOut[38,36,34,32]	
				dOut[36,32]

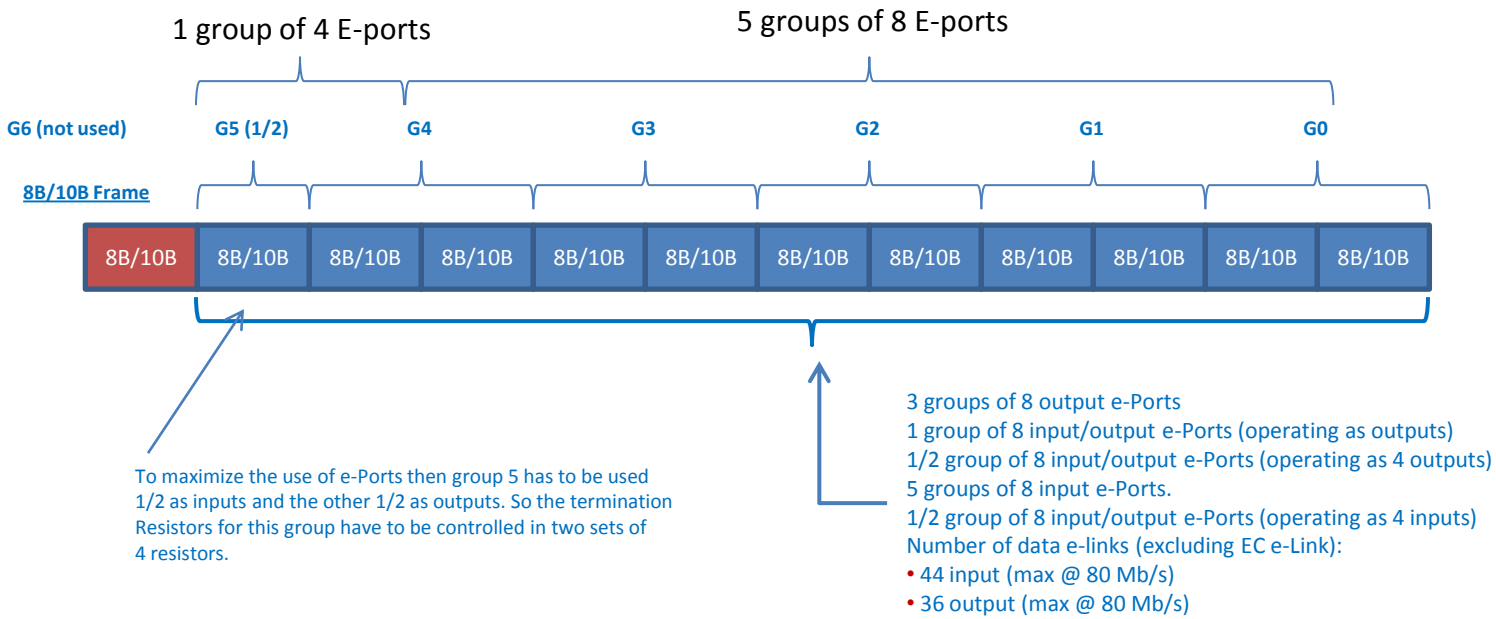
E-Link Data Rate	80 Mb/s	160 Mb/s	320 Mb/s
Max # of up-links:	56	28	14
Max # of down-links:	24	20	10

16, 8 or 4 “Output” E-Links become inputs

Shift order for the E-Link data inputs and outputs is MSB first

8B/10B Mode

(Valid only for the Up-Link)



e-Ports to Frame Mapping in the GBT in the 8B/10B Mode

Uplink (8B/10B frame)

E-Link Data Rate: Up-Link			Group	Frame
80 Mb/s	160 Mb/s	320 Mb/s		
dIn[7:0]			0	FRMUP[19:0]
	dIn[6,4,2,0]			
		dIn[4,0]		
dIn[15:8]			1	FRMUP[39:20]
	dIn[14,12,10,8]			
		dIn[12,8]		
dIn[23:16]			2	FRMUP[59:40]
	dIn[22,20,18,16]			
		dIn[20,16]		
dIn[31:24]			3	FRMUP[79:60]
	dIn[30,28,26,24]			
		dIn[28,24]		
dIn[39:32]			4	FRMUP[99:80]
	dIn[38,36,34,32]			
		dIn[36,32]		
dOut3[3:0]			5	FRMUP[109:100]
	dOut[3,1]			
		dOut[1]		

Downlink (GBT - frame)

Frame	Group	E-Link Data Rate: Down-Link		
		80 Mb/s	160 Mb/s	320 Mb/s
FRMDWN[39:32]	0	n.a		
			dOut[2,0]	
				dOut[0]
FRMDWN[47:40]	0	dOut[7:4]		
			dOut[6,4]	
				dOut[4]
FRMDWN[63:48]	1	dOut[15:8]		
			dOut[14,12,10,8]	
				dOut[12,8]
FRMDWN[79:64]	2	dOut[23:16]		
			dOut[22,20,18,16]	
				dOut[20,16]
FRMDWN[95:80]	3	dOut[31:24]		
			dOut[30,28,26,24]	
				dOut[28,24]
FRMDWN[111:96]	4	dOut[39:32]		
			dOut[38,36,34,32]	
				dOut[36,32]

E-Link Data Rate	80 Mb/s	160 Mb/s	320 Mb/s
Max # of up-links:	44	22	11
Max # of down-links:	36	20	10

4, 2 or 1 “Output” E-Links become inputs