Optical Link Development for Phase-1, ATLAS LAr

Opto Workshop

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SMU PHYSICS LAB
Andy Liu
Datao Gong
Annie Xiang
Kent Liu
Jingbo Ye

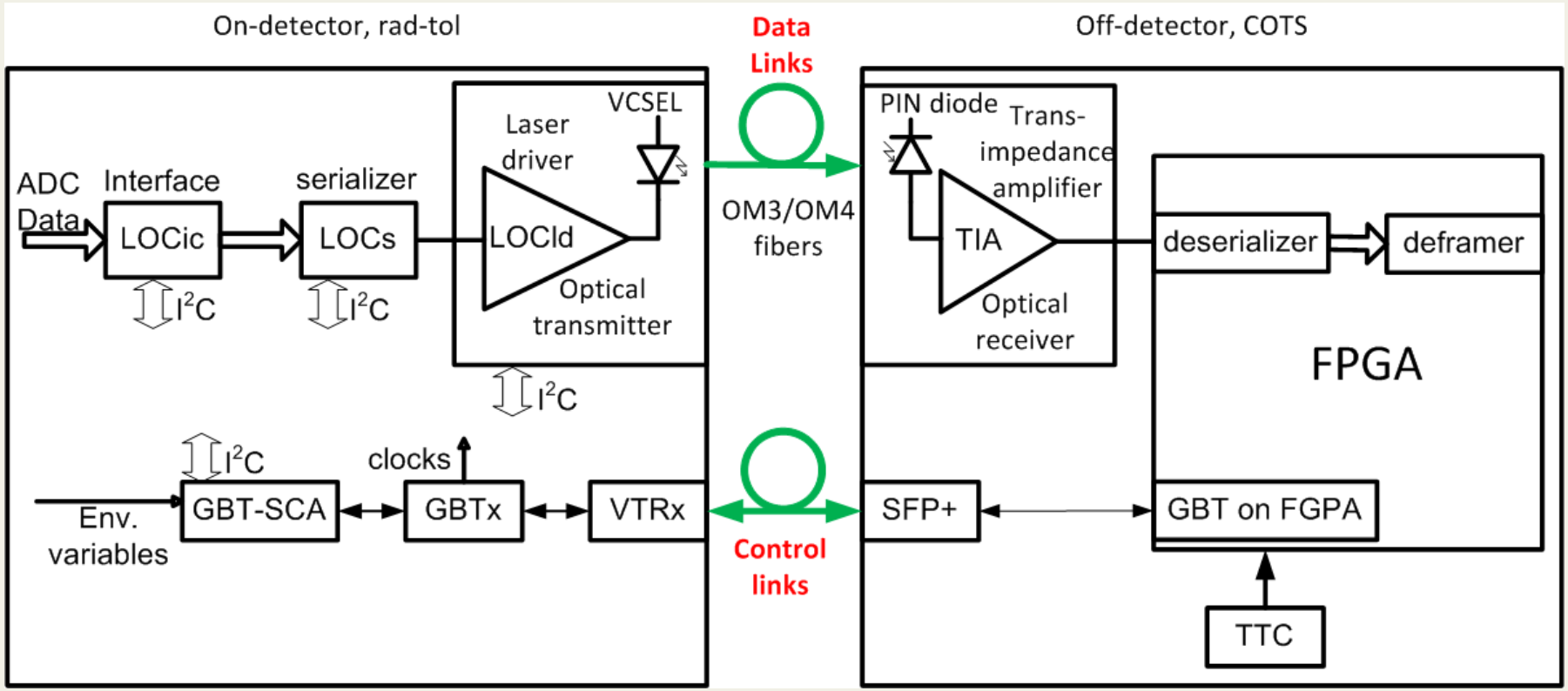
Outline

1. ATLAS LAr phase-1 upgrade and the requirements on optical links.
   - Latency,
   - Data rate and its wide range,
   - Specific transmitting frames,
   - Power dissipation,
   - Rad-tol and related difficulties.
2. The developments to answer the challenges.
   - COTS,
   - ASICs,
   - Custom MTx.
3. Benefits from common projects: GBT based TTC + SCA, custom optical transmitter, fiber, etc, and the back-end.
4. Schedule and plan.

ATLAS LAr phase-1 upgrade and the requirements on optical links

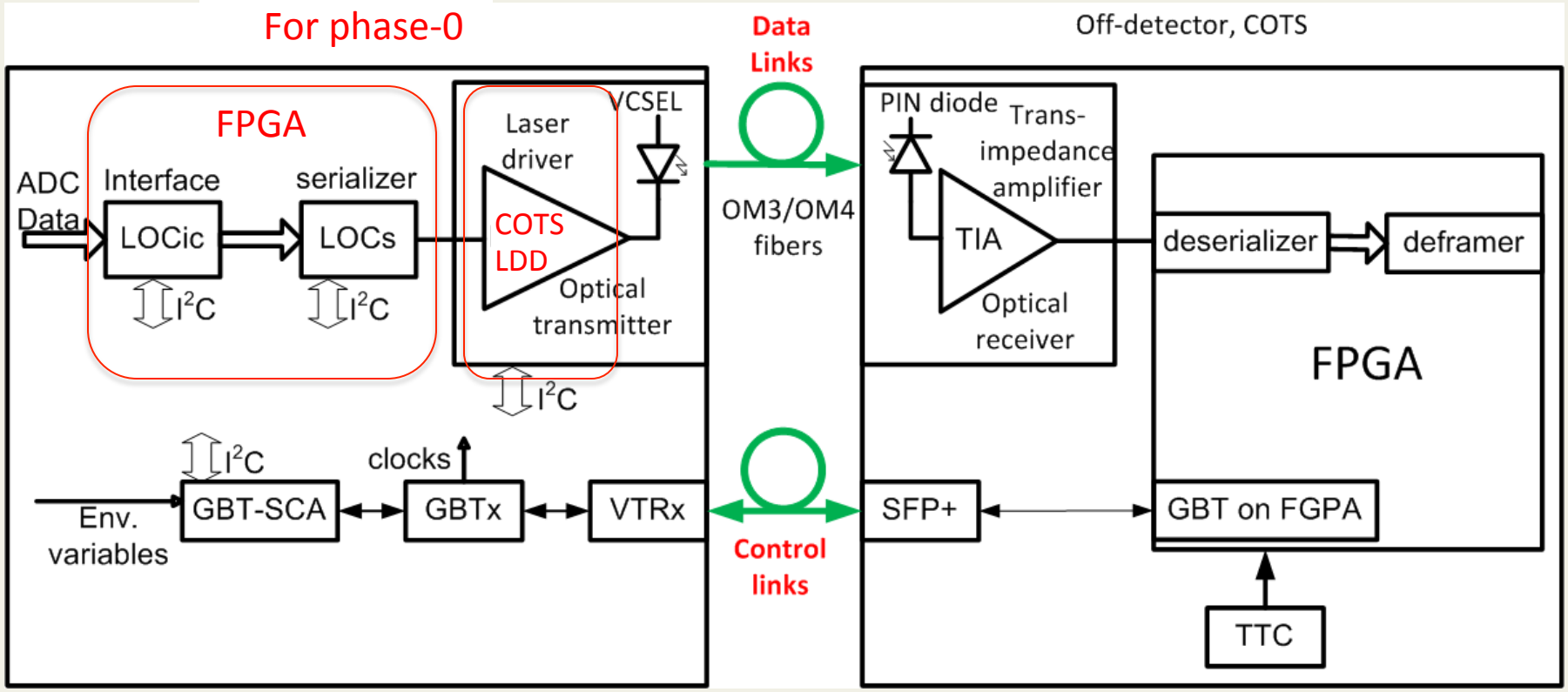
1. ATLAS LAr phase-1 upgrade
   - Goal: to improve level-1 trigger for luminosities expected after LS2 (phase-1) **and** LS3 (phase-2).
   - Idea: to provide level-1 trigger with fine granularity calorimeter information that is usually only available at level-2, so that level-1 trigger can implement some of the level-2 algorithms.
2. Requirements on optical links
   - Latency to be within some legacy buffers on detector front-end for the current level-1 that cannot be upgraded.
   - Data rate is about 200 Gbps per board, or 4.2 – 5.6 Gbps per fiber over 40 fibers, to accommodate data transmission and calibration needs.
   - Specific transmitting frames are investigated to cope with SEU induced link synch loss, and to work with ADC serial outputs.
   - Power dissipation must stay within the capacity of the current cooling system. Need to balance with rad-tol requirement.
   - Rad-tol through phase-2, interesting technical challenges but difficulties in disgusting legal entanglements.

The developments to answer the technical challenges



The ASIC approach, based on LOC and GBT+VTRx

The developments to answer the technical challenges



For phase-0 (or LS1, 2013/14) installation, as a demonstrator for system proof-of-principle, Kintex-7 and COTS LDD will be used in places of LOC ASICs.

The developments to answer the technical challenges

Custom MTx a la VTTx. TOSA based to avoid difficulties in optical coupling, and heat dissipation. We will need fiber connectors smaller than the LC.

R&D work on VCSEL array based optical transmitter will continue and under the support of DOE generic R&D.

For ASIC work please see the ASIC talk.

Benefits from common projects

1. Benefits from common projects:
   - GBT based TTC + SCA. For forward compatibility, and also for interfaces such as I^2C, JTAG, we decide to use GBT for the control and configuration link. The availability of GBT may become an issue for the FPGA based demonstrator link that has a time-line of phase-0
   - custom optical transmitter. MTx = M x VTx plus a change of the optical connector. The critical high speed electrical circuit will be “copy&place”-d.
   - Fiber and passive components. We will only use MM fiber, in 12-way ribbon format.
   - Link back-end, again “copy&place” with parallel optics (miniPOD) version from the Versatile Link project.

Schedule and plan

1. Kintex-7 + COSTs MTx based demonstrator is for LS1.
2. LOC ASIC based data link is for LS2, and driven by the ASIC developments.
3. GBT based control link is aimed for LS1. A TTCrx based fallback solution will be investigated Spring of 2013 if GBT is not available at that time.