SCT SEU measurement

Opto Working Group Mini Workshop

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Motivation

- intense particle flux from beam collisions interacts with the detector → **secondary, highly-energetic hadronic particles**
- these can deposit enough energy in the front-end electronics of the SCT to interfere with its normal operation
- we report on a **measurement** of such **SEU events** within the SCT and **compare with predictions** in beam tests

Overview

SEU:

I mechanism in SCT front-end electronics

II measurement in beam tests

III **measurement in the SCT**

IV **prediction for SCT based on beam test**

I) SEU mechanism

SEU - Where?

- PIN diode - sensitive to small signals, largest active region

SEU - How?

- DORIC4A amplifier AC coupled with threshold close to 0.
- the minimum extra charge required to create a bit error will increase with the increasing value of the mean current in the PIN diode, $\langle I_{PIN} \rangle$

SEU - Who?

- min. energy deposition required in the few MeV range $\gg$ deposition of **m**inimum **i**onising **p**articles (58 keV) (MIP)
- strongly ionising π's from secondary interactions in detector

II) Beam tests

- J.D. Dowell et al. / Nuclear Instruments and Methods in Physics Research A 481 (2002) 575–584

Particle	KE (MeV)	Flux (10^7 cm^{-2}s^{-1})	SEU observed
MIP	< 0.55	4.3	x
Neutrons	14.7	5	✓
π's and protons	300 - 465	depends on KE	✓
π's	405	12	✓

Last row data used for SCT prediction.

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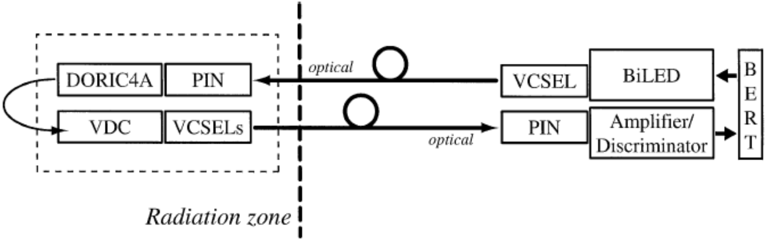
II) Beam test setup

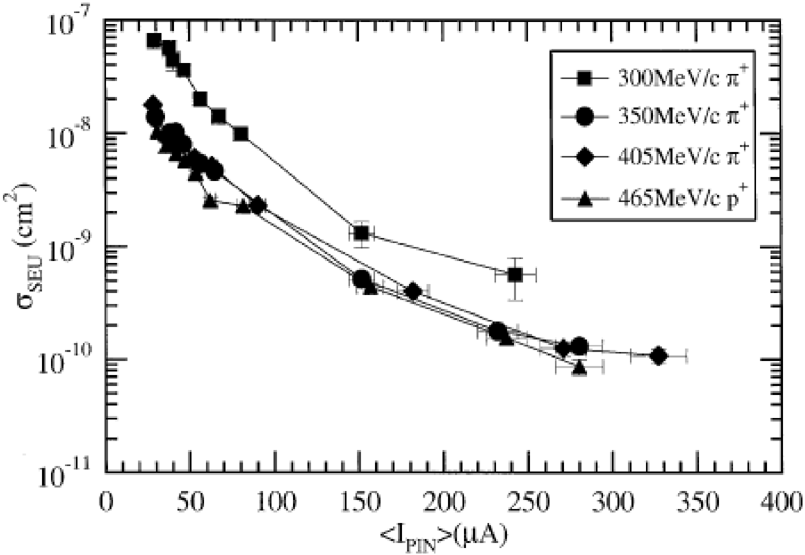


- send 32k pseudo-random number sequence
- receive, decode, encode, send back
- compare received with sent

Convert bit error rate in σ_{SEU}:

$$\sigma_{\mathrm{SEU}} = \frac{N_{\mathrm{ERRORs}}}{\mathrm{flux} \times t} \quad (1)$$

II) Beam test results



III) SEU effect in SCT

One possible **measurable effect**:

- SEU occurs while a L1A (level 1 trigger accept) signal is recieved by a module.
- ABCDT3A chip will miss the L1A signal.
- ABCD3TA will add to the FIFO pipe the hit info + LVL1ID/BCID counters corresponsing to the next L1A only.
- BCID **and** LVL1ID counters for all events stored after the SEU occurence will be out of synch with the rest of the detector until a soft reset command is sent (every few seconds).

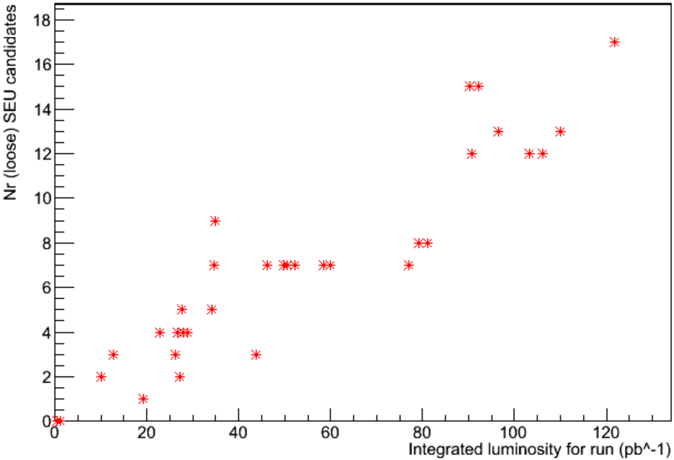
III) SEU effect in SCT

- Look in data in the express_stream (cocktail of various triggers, EF rate ∼10Hz) for error burst for consecutive events.
- typically **a few seconds long**
- require **synchronous LVL1ID and BCID error bursts**
- since SEU is expected to be rare, only **allow one SEU candidate / run.** Discard candidate in that run if the module has more than 1 error burst.

- look in runs in 2011
- $\int \mathcal{L}dt = 1.74\text{fb}^{-1}$

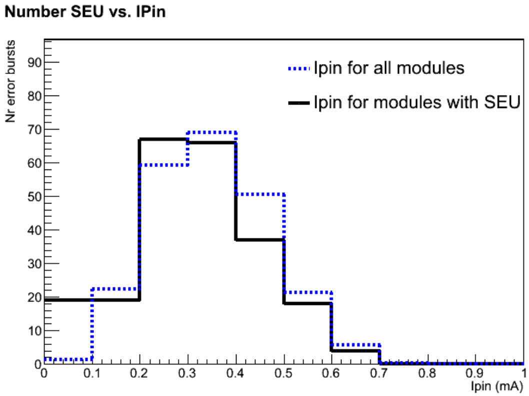
III) #SEU vs. luminosity

Each run analysed is a point.



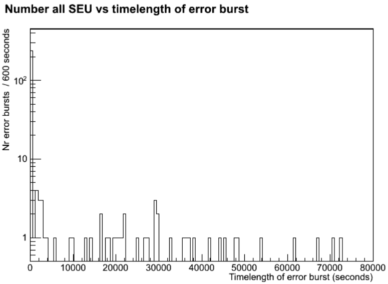
$\int \mathcal{L}dt = 1.74\ \mathrm{fb}^{-1}$; 230 SEU candidates

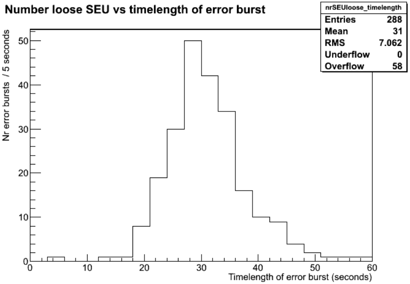
III) $\langle I_{PIN} \rangle$ of affected modules



- $\langle I_{PIN} \rangle$ for all modules: 0.35 mA
- $\langle I_{PIN} \rangle$ for modules with SEUs: 0.31 mA
- Histogram of $\langle I_{PIN} \rangle$ for all modules is normalised to the total number of SEU candidates (230).

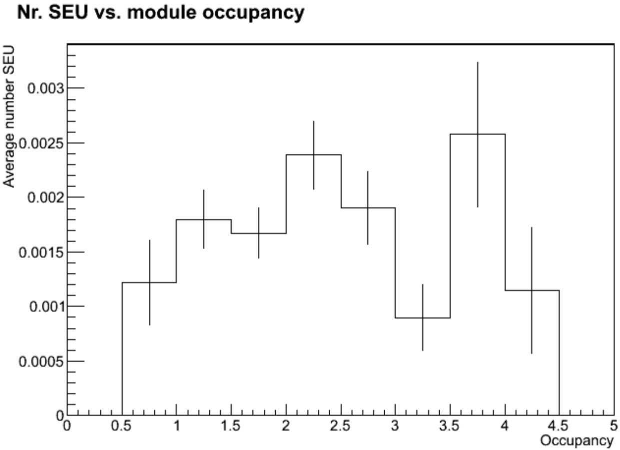
III) Burst timelength





- Large tail, but SEU bursts concentrated at $T \sim 30$s.
- Regular resets do not fix the lack of synchronization, the 30s is the time it takes for the DAQ to reset the module.
- Place a cut at 60s. Assume longer error bursts have some other underlying issue rather than SEU.

III) Nr SEU vs occupancy



Profile plot of average number of SEU for modules with a certain cluster occupancy / event.

IV) Beam test σ_{SEU} vs. #SCT error bursts

- Probability of a bit flip is 0 if:
  - the bit transmitted is 1 or
  - there is no particle flux
- Let $2p$ be - probability of a flip $0 \rightarrow 1$ if there is particle flux in the time bin in which the bit is received.
- $2p$ will depend on $\langle I_{PIN} \rangle$ and particle flux.

Extract $2p$ from the beam test:

- N_{errors} measured in time t
- half the time one was sending 1's, which were not affected.
- Probability of $0 \rightarrow 1$ flip when flux is present:

$$2p = 2 \times \sigma_{\mathrm{SEU}} \times \mathrm{fluence} \tag{2}$$

IV) Beam test σ_{SEU} vs. #SCT error bursts

- L1A signal has the format ...00110...
- SEU can occur in any 0's in the presence of particle flux.
- 50 ns BC means only every second bit affected.

	Pre-L1A		During L1A			$Pr_{miss\ L1A}$
Collisions	x	0	x	0	x	-
Data	0	0	1	1	0	$2 \times (2p)$

$$Pr_{\mathrm{miss\ L1A}} = kp, \text{ with } k = 4 \tag{3}$$

However, *k* is still not well determined.

- beam tests: flux received asynchronously with clock; the flux that induces SEU is really 6ns / 25 ns * nominal flux
- SCT: the overlap between the 6ns window and the particle flux not well known.

IV) How to create a spurious L1A

Spurious L1A? ABCD3TA is listening (to **..**000**..**):

- if **one bit** flips here, it will not look like L1A and will be ignored
- in principle SEUs can incur **multiple bit** flips but at the large values of $\langle I_{PIN} \rangle$ used, this should be a small effect.

Control command is **..**00**101**:

- if preceding bit flips, it will look like L1A
- control commands not very frequent, ignore this effect

IV) SCT prediction from beam test

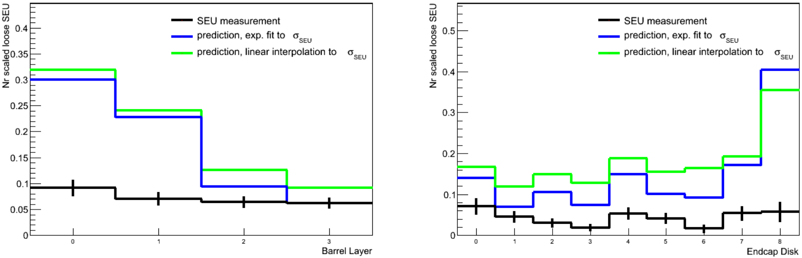
The predicted number of missed L1A signals for any given module in any given run:

$$\begin{aligned} \text{predicted \#missed L1A} &= Pr_{\text{miss L1A}} \times \text{\#L1A (run)} && (4)\\ &= k \times \frac{\text{Ev. Cluster Occupancy (module, run)}}{A_{\text{module}}} && (5)\\ & \quad \times \sigma_{\text{SEU}}\left(\langle I_{PIN}\rangle\right) && (6)\\ & \quad \times \text{\#L1A (run)} && (7) \end{aligned}$$

- set $k = 1$ rather than $k = 4$ for now
- #missed L1A = # LVL1ID and BCID error bursts
- compare predictions vs. actually measured:
  - **average** over all modules in a barrel layer / endcap disk
  - **sum** over all analysed runs

IV) SEU measurement vs prediction

Nr SEU / module for all analysed runs.



- order of magnitude agreement.
- obvious discrepancies under investigation.

Conclusions

- **measured SEU rate** in the SCT front-end opto-electronics
- **compared measurement with predictions** from beam tests
- **agreement within order of magnitude**

To-Do:

- improve statistics, analyse full 2011 data set / 2012 data set
- algorithm too selective and misses some SEUs?
- understand features like #SEU vs. module occupancy

Back-up slides

BackUp

SEU mechanism

SEU - Where?

Parts of the SCT optical links system sensitive to small signals:

- PIN diode (active region: diameter 350 μm, thickness 15 μm)
- amplifier and receiver ASIC: DORIC4A chip (much smaller active region in comparison)

SEU - Why?

- DORIC4A amplifier AC coupled with threshold close to 0.
- the minimum extra charge required to create a bit error will increase with the increasing value of the mean current in the PIN diode, $\langle I_{PIN} \rangle$
- min. energy deposition required in the few MeV range $\gg$ deposition of **m**inimum **i**onising **p**articles (58 keV) (MIP)

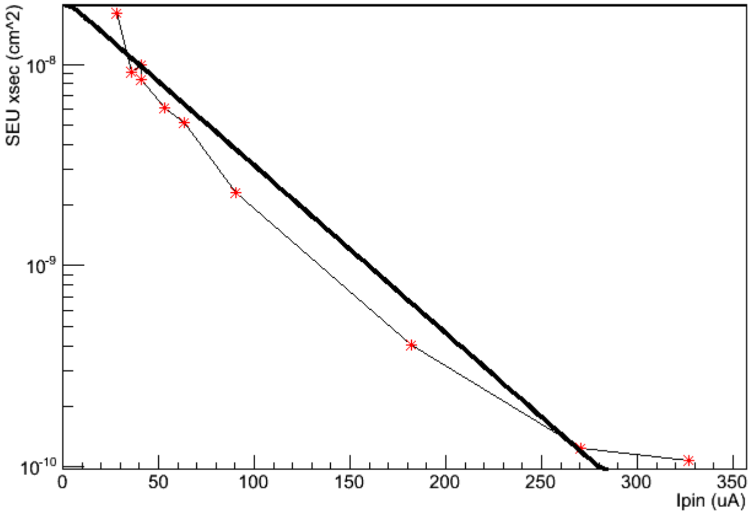
SEU mechanism

SEU - Who?

- not MIPs
- strongly ionising π's from secondary interactions within the detector
- need between 1 - 8 MeV to create bit error, corresponds to linear energy transfer in range 29 - 230 MeV gm^{-1} cm^2.

SEU - With what effect?

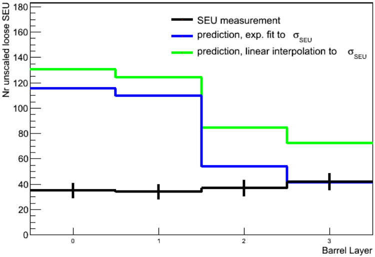
- different for normal SCT operation and beam tests.

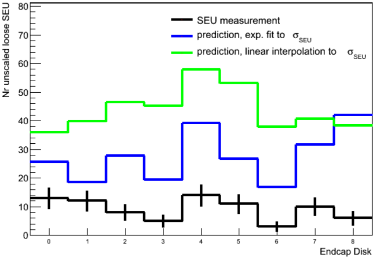


Exponential fit versus "linear" interpolation for σ_{SEU}, π 405 MeV/c.

IV) SEU measurement vs prediction

Not normalised to number of modules in layer/disk.





- shape agrees well for endcaps.
- deficit in barrel layers 0,1.