Proposal of a sparsification circuit for mixed-mode MAPS detectors

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SLIM5 project (INFN collaboration: BO, PI, PV, TO, TN, TS)

Aim

Improve the state-of-the-art of slim tracking system construction for high-energy physics applications

Applications

Low material budget silicon tracking systems (detector/ mechanics/cooling) relevant for the future experiments (SuperB, ILC) to reduce multiple scattering

MAPS (Monolithic Active Pixels Sensors)

- good candidate technology for the innermost layers of the vertex detectors,

- sensitive zone 10-20 µm thick with integrated front-end electronics,

- some latest papers and presentations:

L. Ratti, et al., Nucl. Instr. and Meth. A-568 (2006) 159

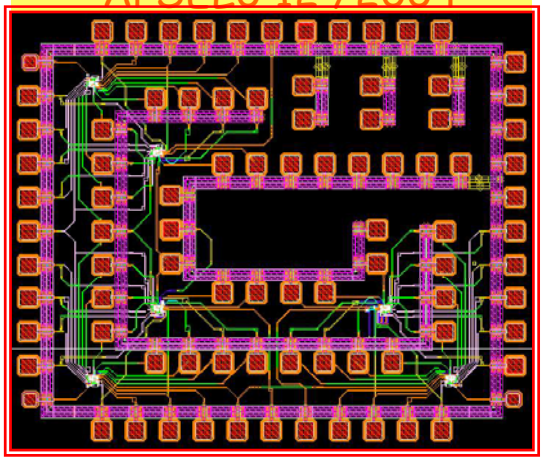
G. Rizzo et al., Nucl. Instrum. Methods, A-565 (2006), 195

F. Forti et al., 2006 IEEE NSS, San Diego, Oct. 30-Nov. 2, IEEE 2006 N34-7

THE PAST: ASICs designed, fabricated and tested

Full-Custom ASICs: APSEL0, APSEL1, APSEL2M/T

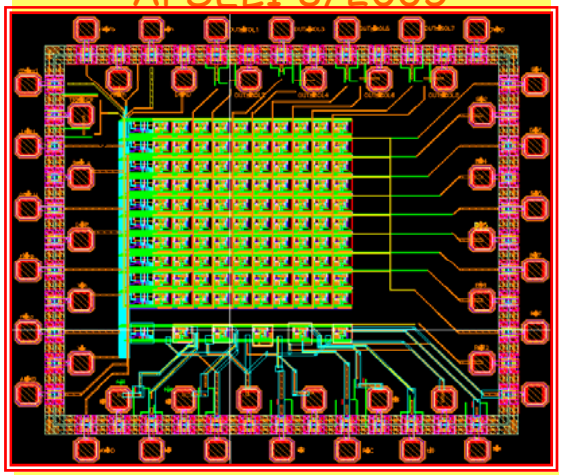
APSEL0 12 /2004



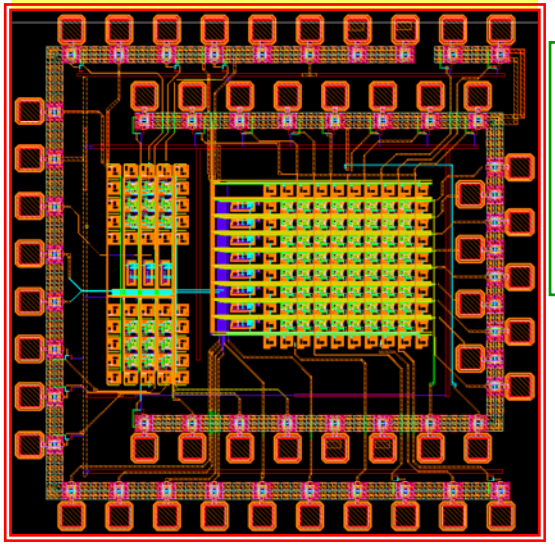
The ASICs differ basically in

- pixel layout,
- matrix dimensions,
- sensitivity

APSEL1 8/2005



APSEL2M 8/2006

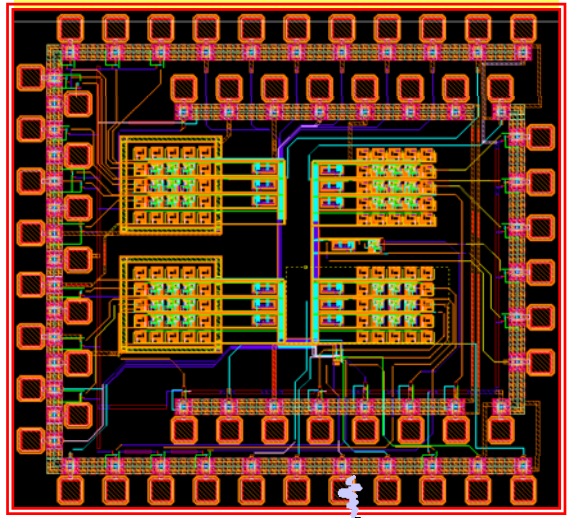


Designs fabricated with:

0.13µm ST-Microel.

CMOS technology

APSEL2T 8/2006

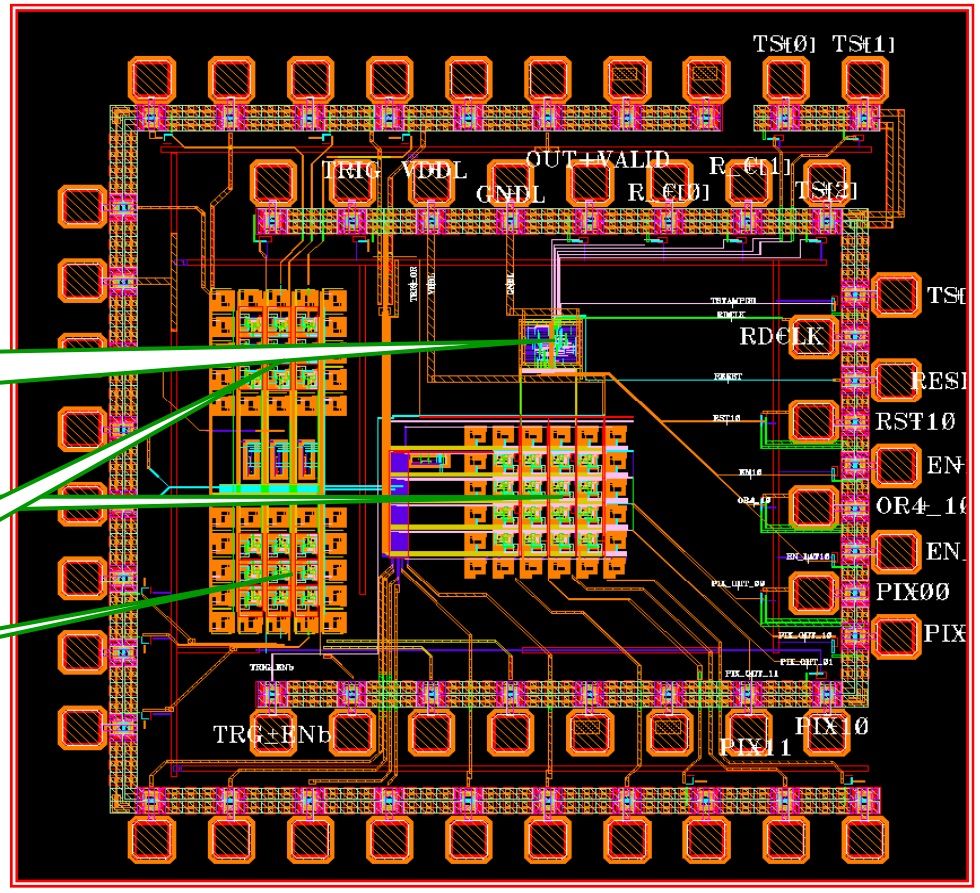


THE PAST: ASICs designed and fabricated

First mixed-mode ASIC: APSEL2D

APSEL2D includes a standard-cell based readout logic

APSEL2D 11/2006



300 std-cell readout circuit with sparsification capabilities

16-MAPS matrix

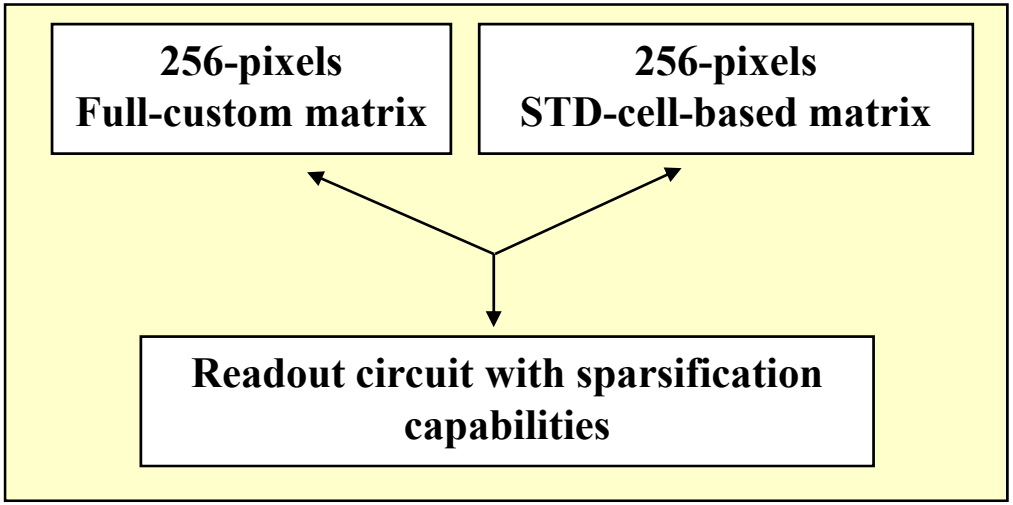
2 Test circuits

THE FUTURE: ASICs designed and under submission

First "large-matrix" mixed-mode ASIC: APSEL3D

Main Features

- **2 matrixes of 256 pixels** each
  - **1** made of MAPS,
  - **1** based on digital std-cells,
  - to be used one at a time,
- **Slow-Control** for configuration,
- on-line data sparsification,
- **52 Pads**
  - 15 digital outputs,
  - 16 digital inputs,
  - 7 analog ref. I/Os,
  - 12 analog + digital VDD/GND,
- **2 clocks** (over 50 MHz),
- **Stand_By** if over-hit-rate



7200 std-cells for the digital architecture

+

256 full-custom MAPS

THE FUTURE: ASICs designed and under submission

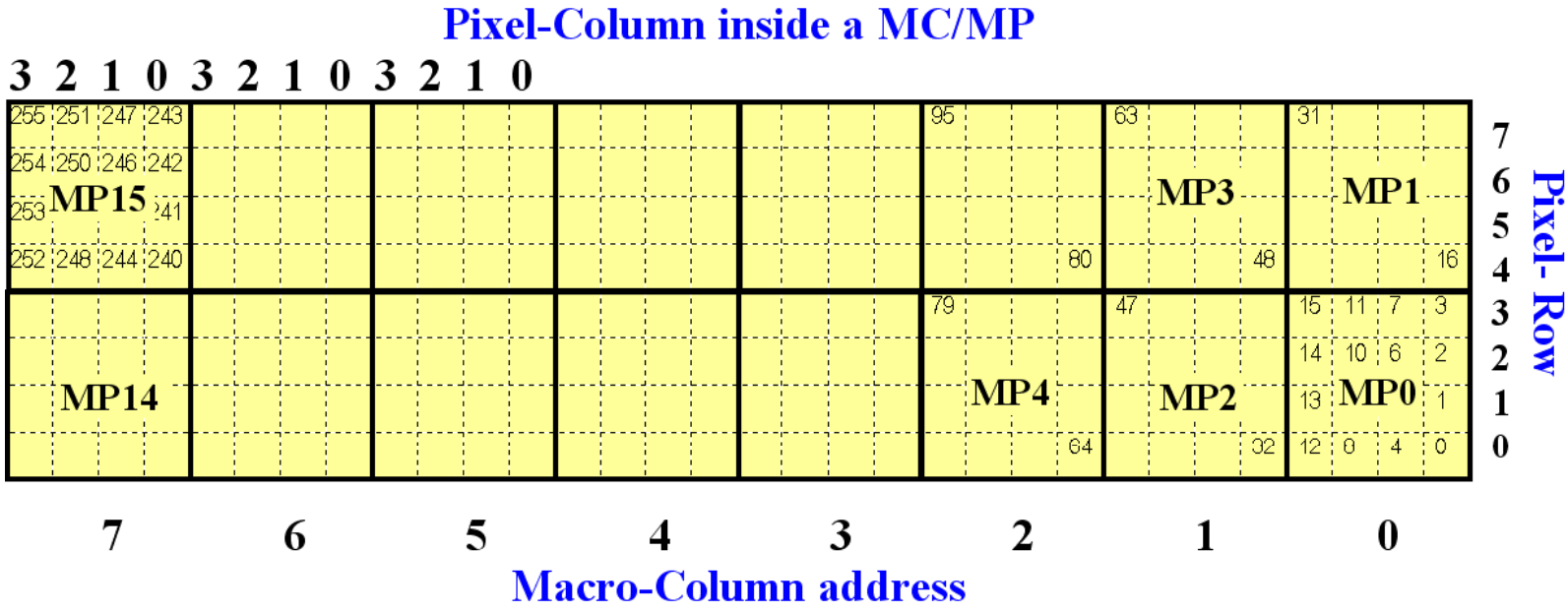
The Matrix

The 256-pixel matrix is arranged in:

- **32** columns × **8** rows,
- **8** MacroColumns (MC) × **2** MacroRows (MR),
- **16** MacroPixels composed of **4 × 4** pixels

The pixels, the MCs, the MRs and the MPs are numbered to define the **13-bit** formatted output data

The hits are on-line associated with a **4-bit Time-Stamp**

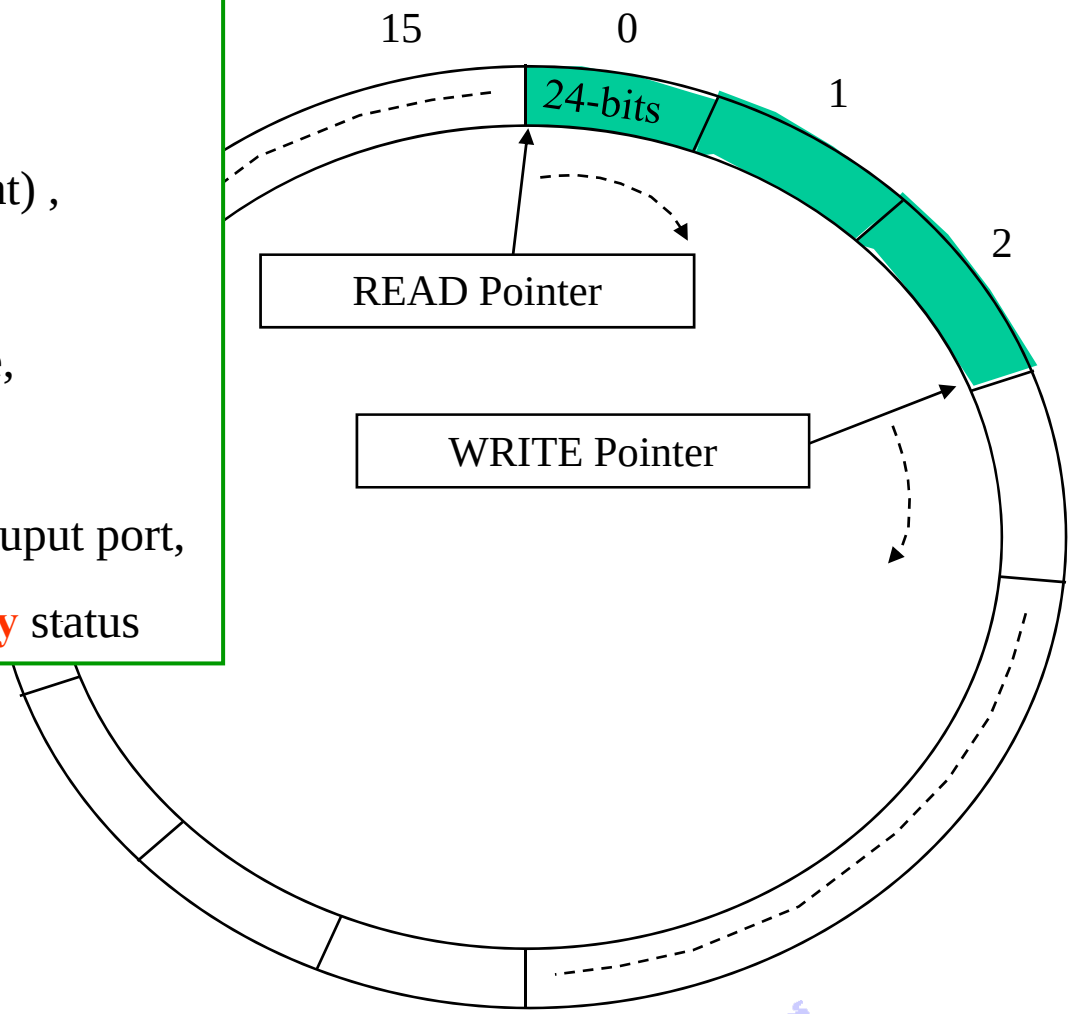


THE FUTURE: ASICs designed and under submission

The queued output dataflow

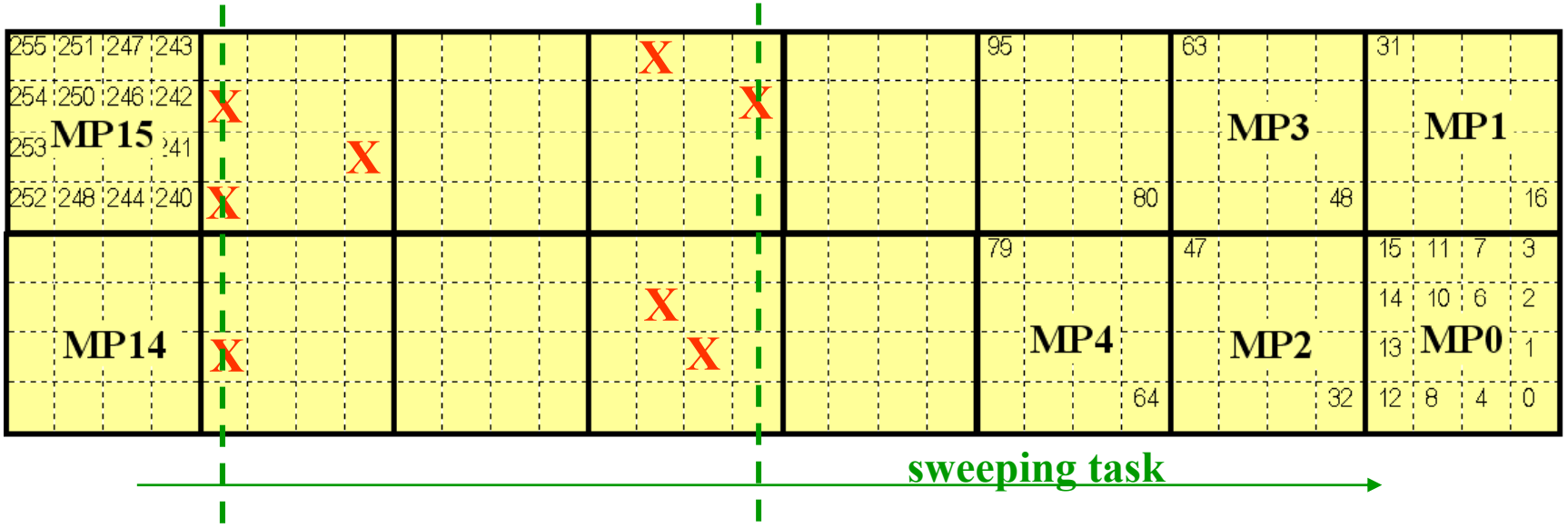
The output BARREL:

- is circular and **16-word deep**,
- has **24-bit words** (now redundant) ,
- **never shifts** data (low power),
- uses pointers to identify the state,
- **reads 1 to 8 words** at a time,
- **writes 1 word at a time** to the ouput port,
- **empties** its words if in **Stand_By** status



THE FUTURE: ASICs designed and under submission

The Matrix Readout



At each clock cycle, a full column (1-to-8 hits) is readout in parallel….

… then each hit is associated with its Time-Stamp and the information …

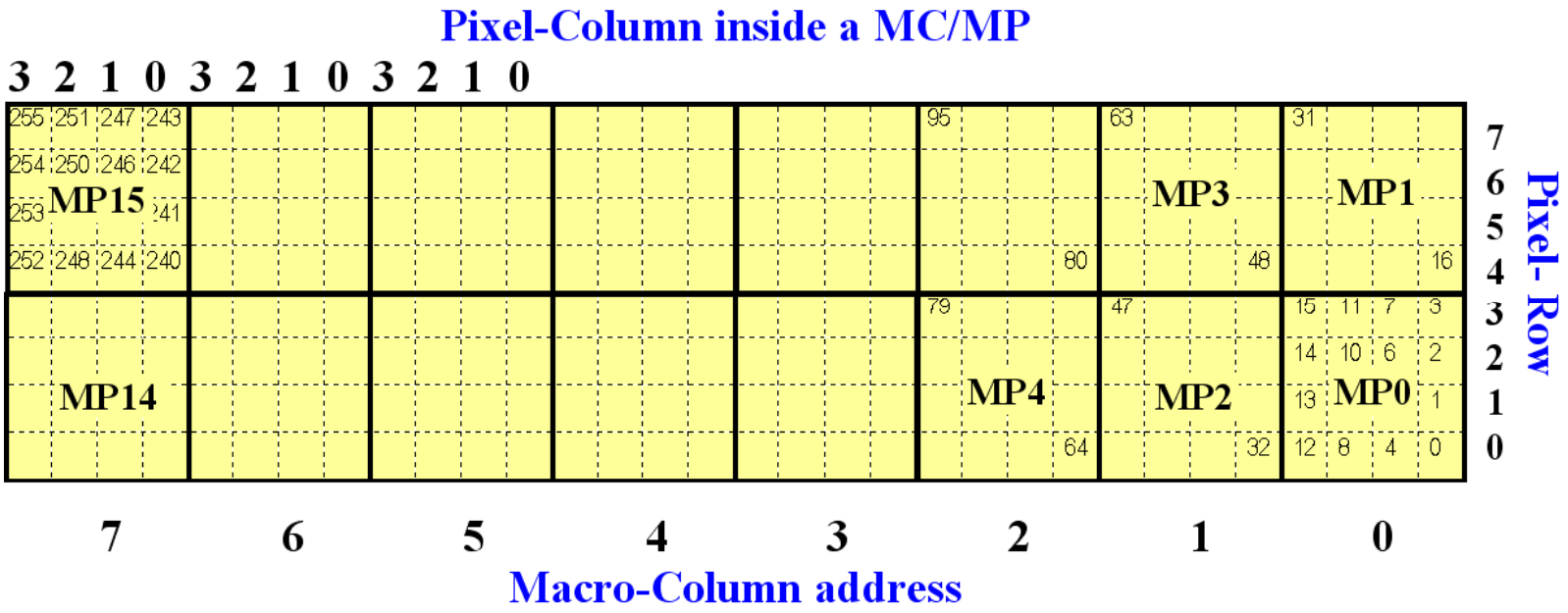
… is sent to a FIFO-like BARREL output to queue the dataflow

Each MC readout requires 4 cycles + 1 to reset the MPs. Empty MCs are skipped

Example above requires 10 (2 MC × 5) cycles to readout 8 hits. Then the 8 hit words are packed into the BARREL and sent to ASIC's output in 8 clock cycles

THE FUTURE: ASICs designed and under submission

The Matrix Readout



FORMATTED OUTPUT (1+3+2+3+4 = 13 bits)

<Data Valid><Pixel Row><Pixel Column within MP><MC Address><Time Stamp>

THE FUTURE: ASICs designed and under submission

The APSEL3D ASIC

Analog Pads

256-MAPS matrix

7200 std-cell area

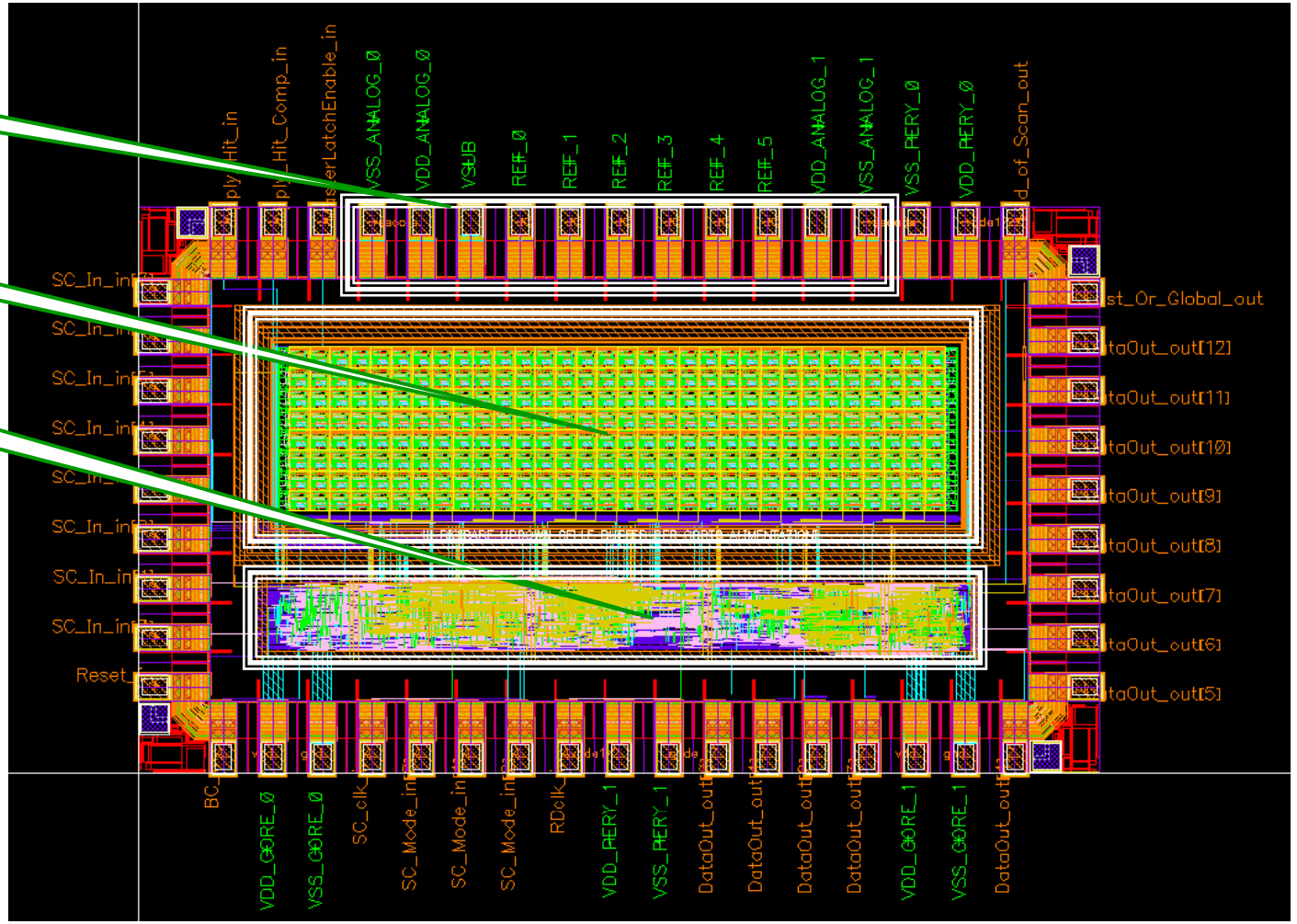
Area

2343.56 µm

×

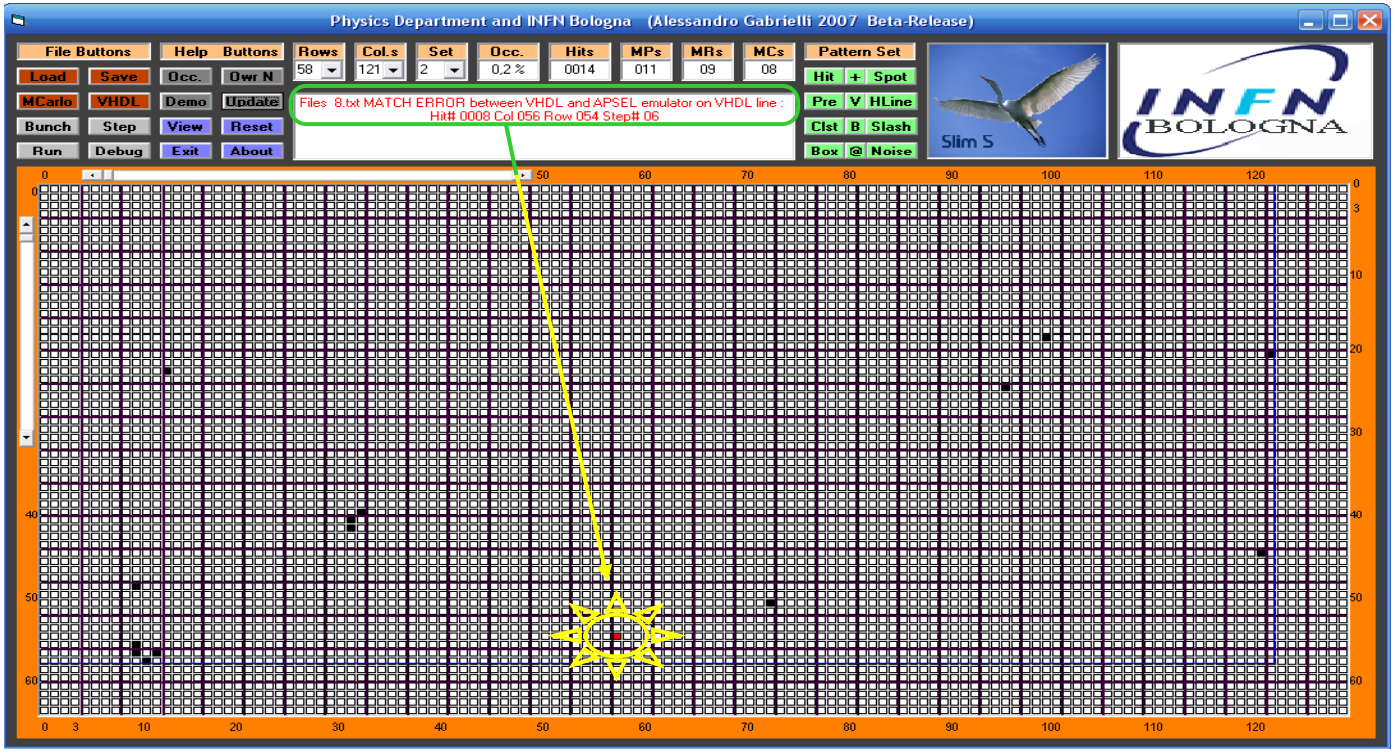
1379.24 µm

Pitch = 120.54 µm



THE FUTURE: ASICs designed and under submission

The simulator-debugger: under development



The simulator-debugger:

- interfaces with Monte Carlo input patterns,
- provides APSEL3D's formatted output data,
- copes with matrixes up to 128 ×64 pixels

CONCLUSIONS

The work is aimed at

- fabricating a first “large-size” prototype,
- fabricating a high-density thin MAPS detector, **new versions up to 10k MAPS**,
- sparsifying on-line the hits,
- matching the requirements of future HEP experiments.

In particular, the readout architecture extends the flexibility of the MAPS devices to be also used in first level triggers on tracks in vertex of future detectors.

It is a novel ASIC with an integrated sparsification circuit on