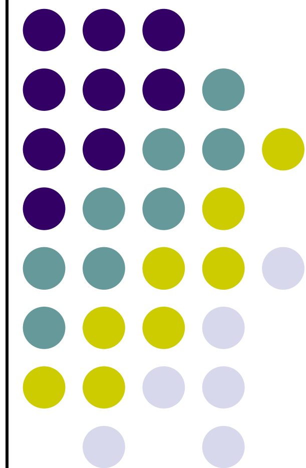
Test procedures for ALICE Silicon Pixel Detector ladders



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University & INFN Catania

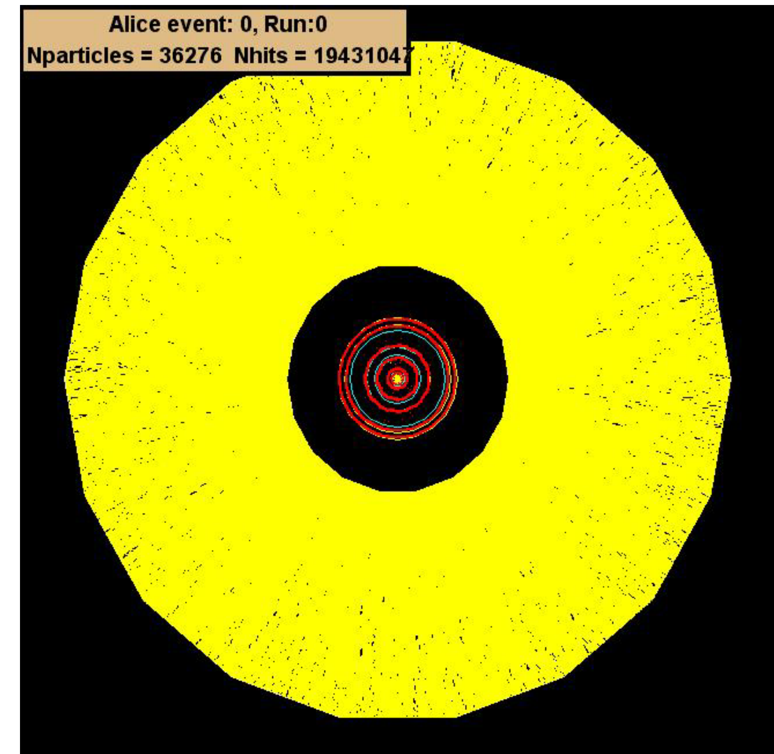
8th International Conference on Large Scale Applications and Radiation Hardness of Semiconductor Detectors

Florence, 27-29 June 2007

Large Hadron Collider

Some numbers related to ALICE and LHC

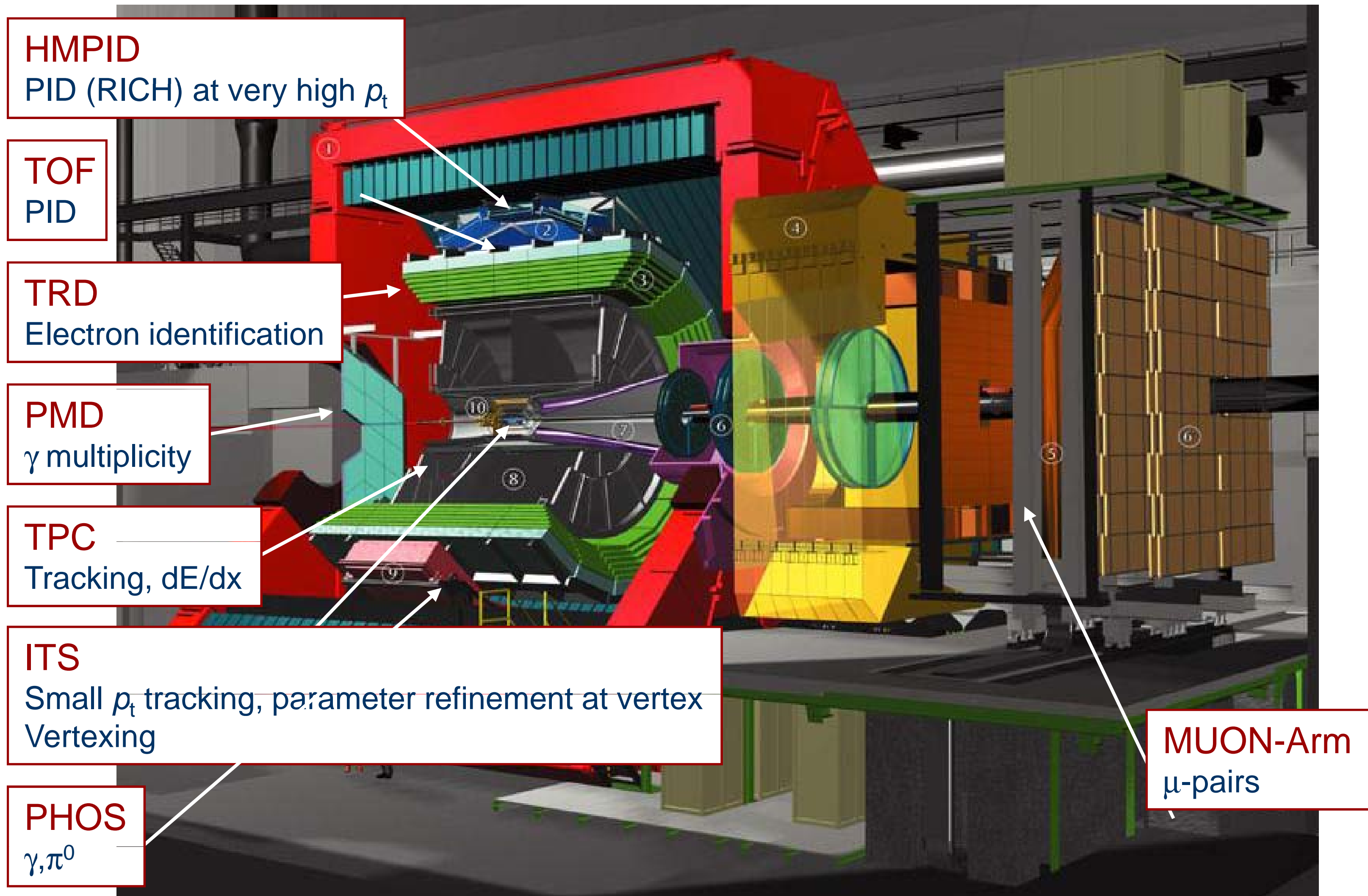
- 5.5 A TeV Pb-Pb
- Expected multiplicity $(dN_{ch}/dy)_{y=0}$:
  - Major uncertainties not completely resolved
  - Still no safe way to extrapolate
  - Simple scaling form RHIC → ~2500
  - Safe guess → ~1500 - 6000
  - Worst case → ~8000
    - Baseline in the project
- Luminosity for Pb-Pb:
  - $\mathcal{L}_{max} = 1\times10^{27}$ cm^{-2}s^{-1}



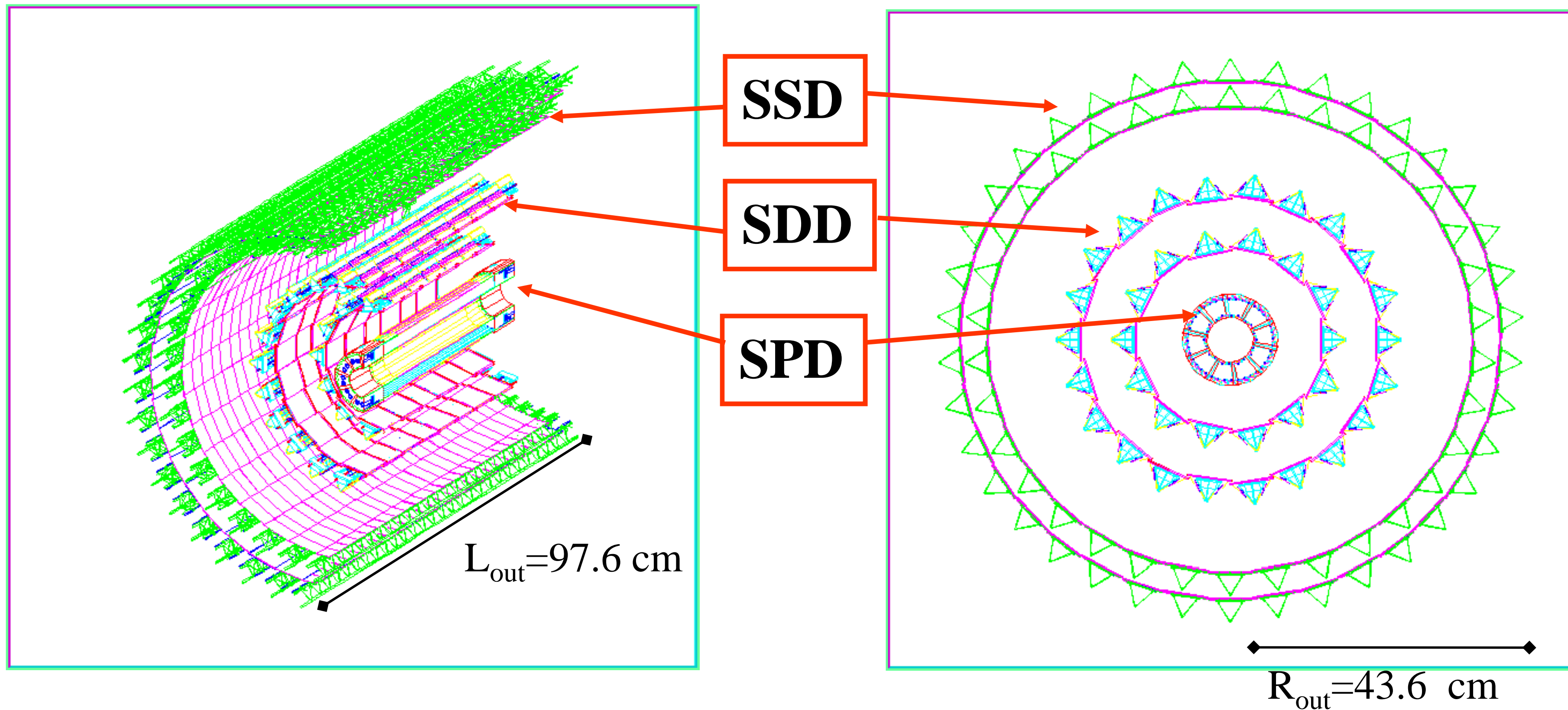
...and the worst case for

ALICE

The ALICE detector



Inner Tracking System (ITS)



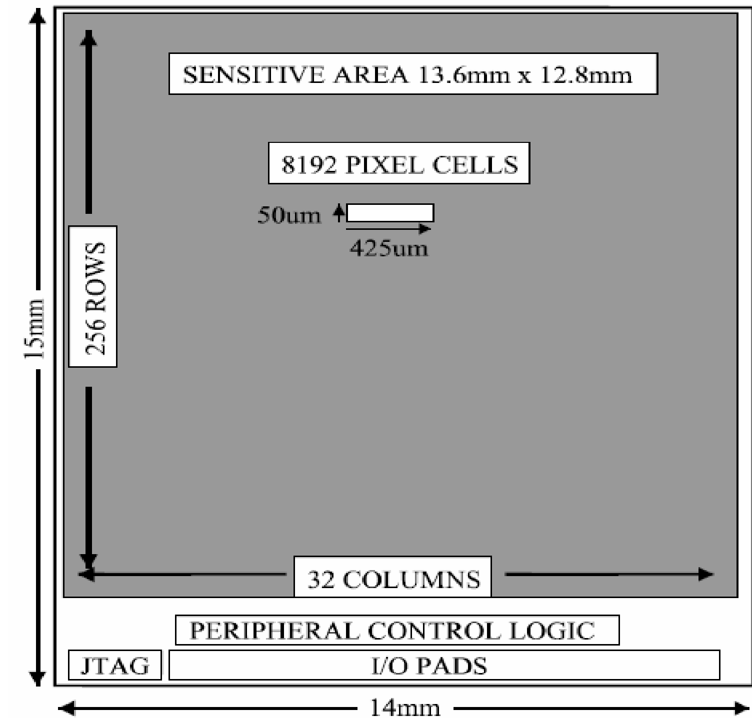
- 6 Layer, 3 technologies (occupancy ~2% at max multiplicity)
  - Silicon Pixels (0.2 m^2, 9.8 Mchannels. Single chip size = 50x425 μm)
  - Silicon Drift (1.3 m^2, 133 kchannels)
  - Double-sided Strip (4.9 m^2, 2.6 Mchannels)

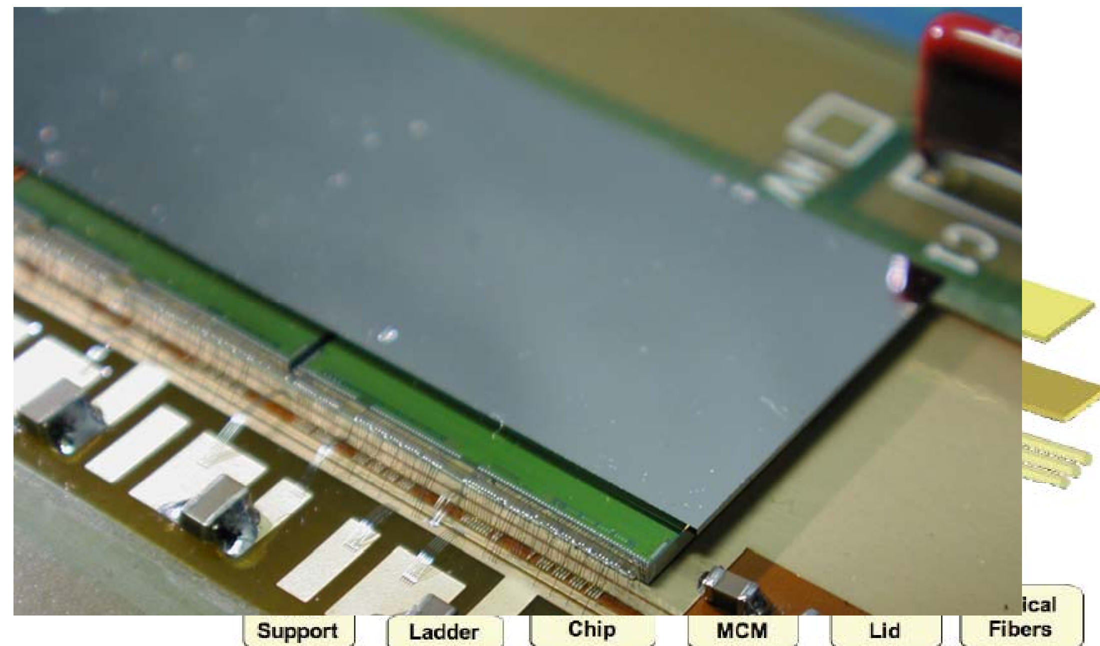
ITS performances

	Layer 1, 2 Pixel (SPD)	Layer 3, 4 Drift (SDD)	Layer 5, 6 Strip (SSD)
$\Delta(r\phi)$ (μm)	12	38	20
Δz (μm)	100	28	830
Two track resolution $r\phi$ (μm)	100	200	300
Two track resolution z (μm)	850	600	2400
Cell size (μm^2)	50 × 425	150 × 300	95 × 40000
X/X_o (1%)	2.0	2.2	1.76

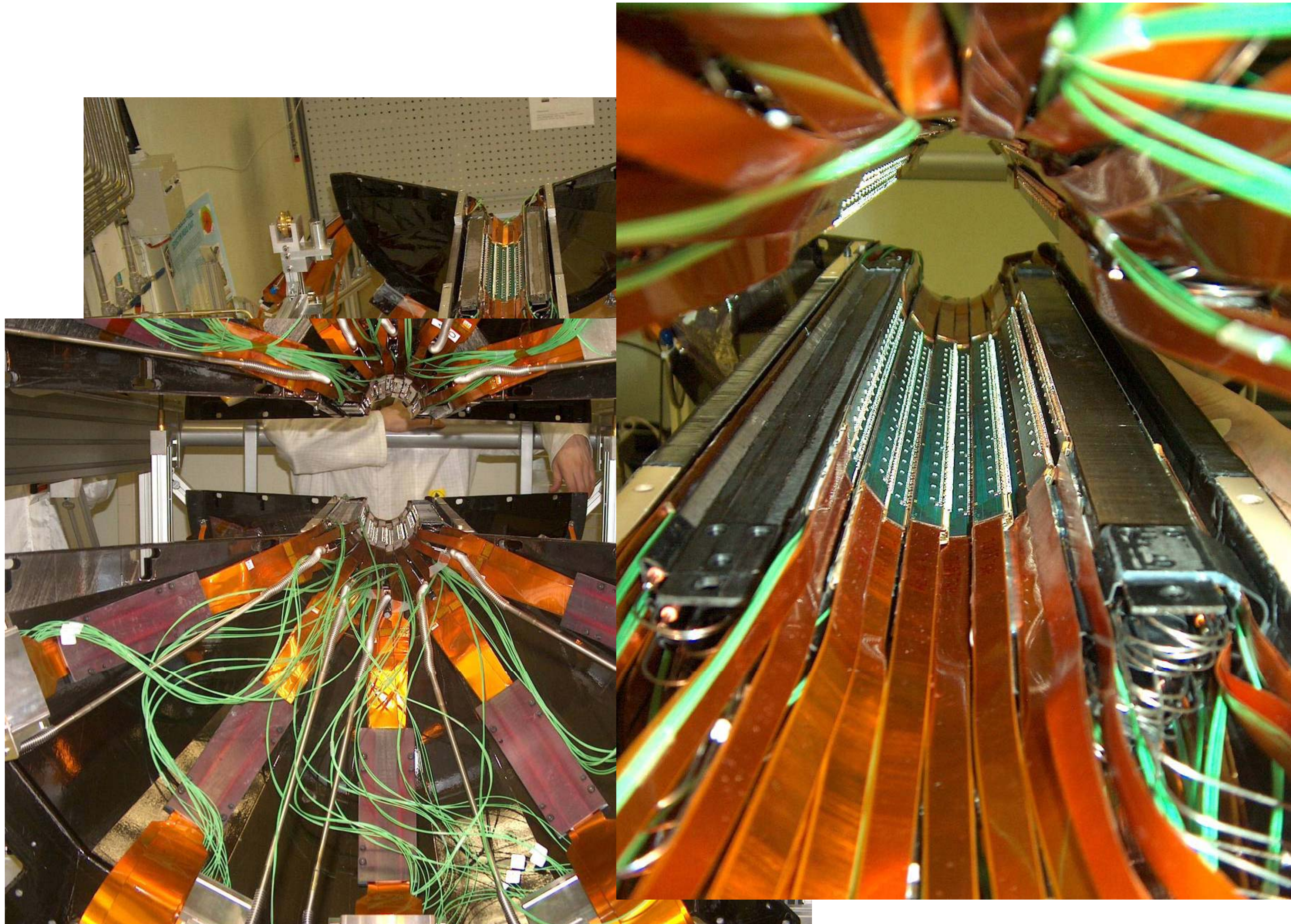
Silicon Pixel Detectors

- ASIC Chip (150 μm thick):
  - 8192 pixels (256 columns * 32 rows)
  - sensitive area: 13.6 mm x 12.8 mm
- Silicon sensor (200 μm thick)
  - size: 70.7 mm x 16.8 mm
- Elementary assembly: the “Ladder”
  - = 1 Si sensor bump-bonded to 5 chip cells



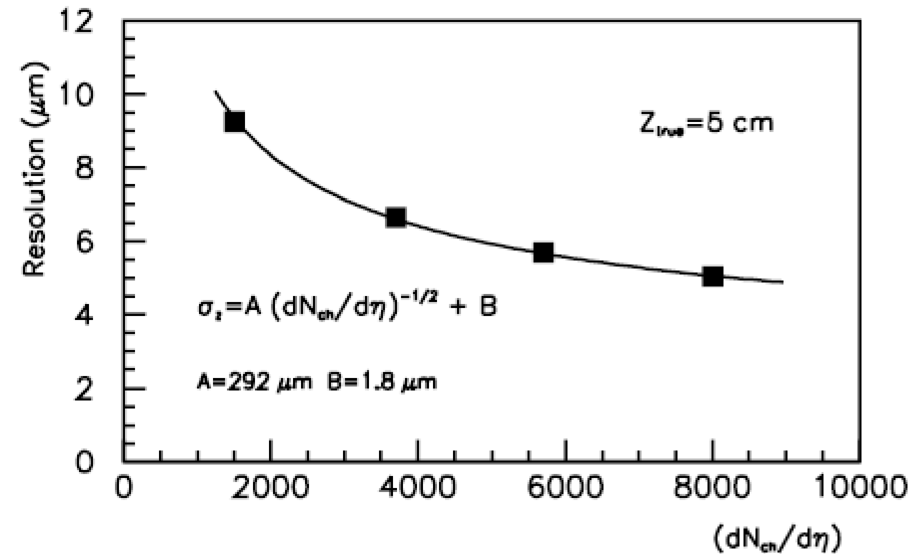


Silicon Pixel Detectors



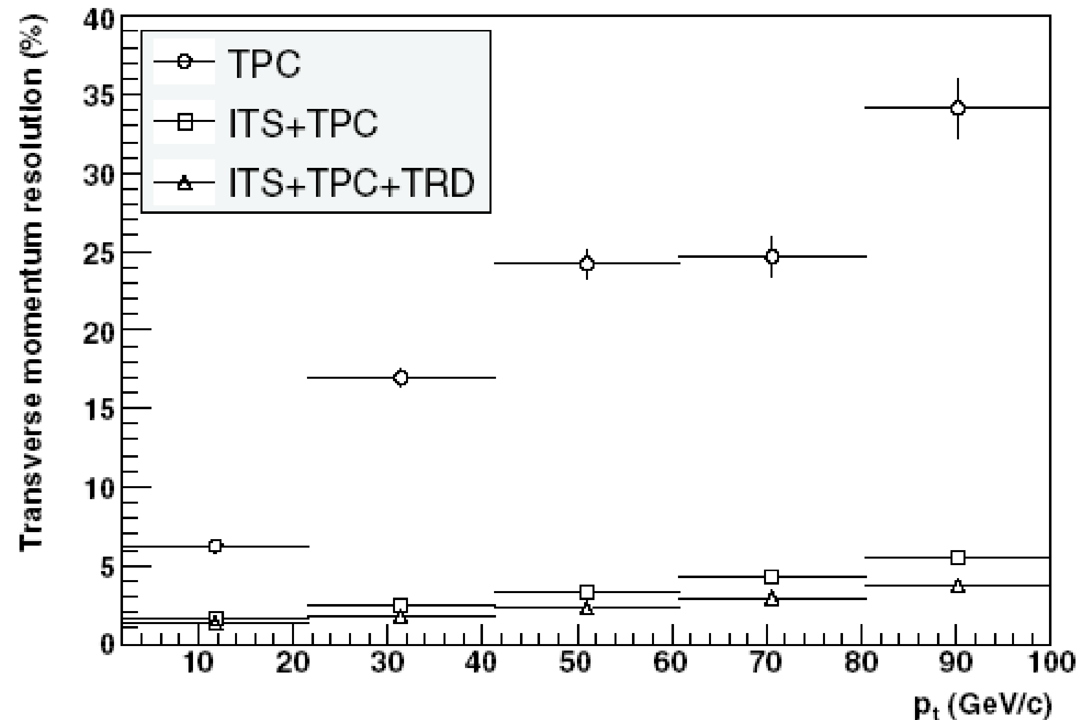
ITS purposes

- Track propagation to the closest distance from the interaction point
  - Best resolution for all track parameters
- Tracking of low transverse momentum particles



Main SPD contributions:

- Primary vertex estimation before tracking (and used as a constraint for primary particles tracking)
- Event multiplicity evaluation
- Secondary vertices detection
  - D, B
  - strangeness



SPD test: work sequence

- Step 1: wa
  - chips are
  - each chip
  - chips whi
- Step 2: lad
  - ladders a
    and also
  - when at l
    (bad chip
  - when too many chips are not good, the ladder is rejected

SPD test: evaluation criteria

- Chips:
  - Class I – "good"
    - used to build ladders
  - Class II – "not too bad"
    - used for tests
  - Class III – "bad"
    - rejected

- Ladders:
  - Class I: "good"
    - used to mount half-staves
    - *When: all class I chips*
  - Class II: "not too bad"
    - reworked to be re-tested
    - used for test
    - *When: at least one class 2 chip*
  - Class III: "bad"
    - if just 1 bad chip → rework
    - If too many bad chips → reject
    - *When: at least one class 3 chip*

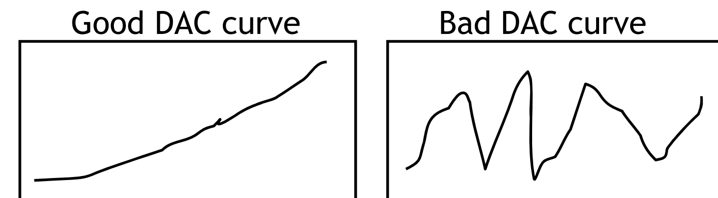
Chip test sequence (I)

- Test of currents in the chip:
  - too high values can damage the chip (or the testing apparatus) or cause the chip not to work properly
  - *Test protocol: threshold values for maximum allowed currents*
    - *If I_analog > max or I_digital > max → CLASS 3*

- Test of JTAG:
  - JTAG is fundamental for the dialog between the chip and the computer which must control it and read data from it
    - *if JTAG test fails → CLASS 3*

Chip test sequence (II)

- Test of digital-to-analog converters (DAC)
  - DAC are fundamentals both for setting working parameters of chips and to read signals from them
  - *Requirement: the conversion DAC curve must be smooth*
    - *if at least one DAC curve is not smooth → CLASS 3*

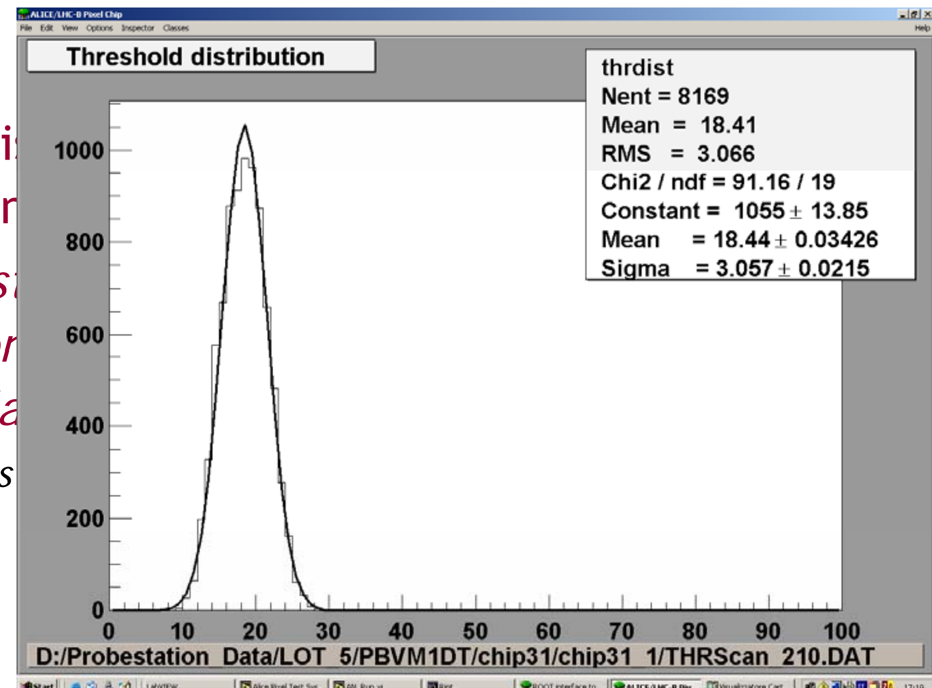


- Minimum threshold search:
  - *Requirement: a value must be found for which NO pixels fire due to electronic noise only*
    - *if at least one pixel cannot be switched off (by lowering the threshold or masking that pixel), and then no minimum threshold is found → CLASS 3*

Chip test sequence (III)

- Pixel matrix test
  - for 100 times, a MIP-like signal is sent to each pixel, when the whole chip is set to the minimum threshold value found before
  - *Requirement: all pixels must respond to this signal almost always (~100 times).*
    - *if more than 1% (=82) pixel are underefficient or overefficient → CLASS 2*

- Threshold scan:
  - a signal is sent to the chip, which i
  (60mV) to zero: at each step, the r
  - *Requirement: responding pixel dis must have a mean value not larger waferprobing step, 60 mV in the la*
    - *if the mean of threshold distribution is*



Chip test sequence (IV)

- Fast-OR minimum threshold
  - Fast-OR signal is generated by the chip when at least one chip responds.
  - It can be used as a trigger during data acquisition.
  - *Requirement: a threshold value must be found for which the pixel **does not** return a FO signal in absence of signal (i.e. due to noise)*
    - *if no FO minimum threshold is found → CLASS 3*

Average required time for a complete chip test:

10 min.

Detector test sequence

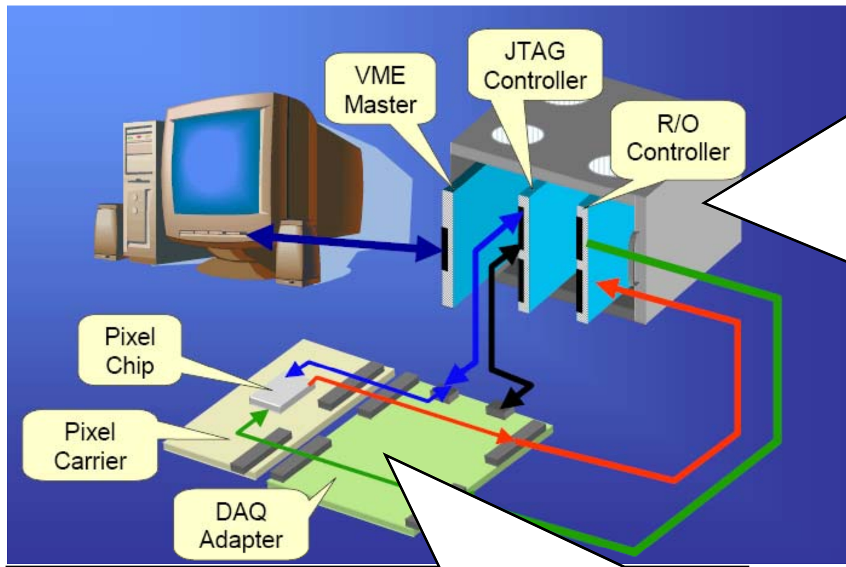
- Leakage current
  - Requirement: not larger than a threshold value (1 mA) when applyng standard bias
    - *if leakage current is too large → CLASS 2*

- Detector response:
  - the detector is exposed to a 37 MBq ^{90}Sr source
  - *Requirement: 1% maximum pixel defects (dead or noisy)*
    - *if there are > 1% dead/noisy pixels or entire dead/noisy columns → CLASS 2*
    - *if there is are too many dead/noisy pixels or dead/noisy zones in the matrix → CLASS 3*

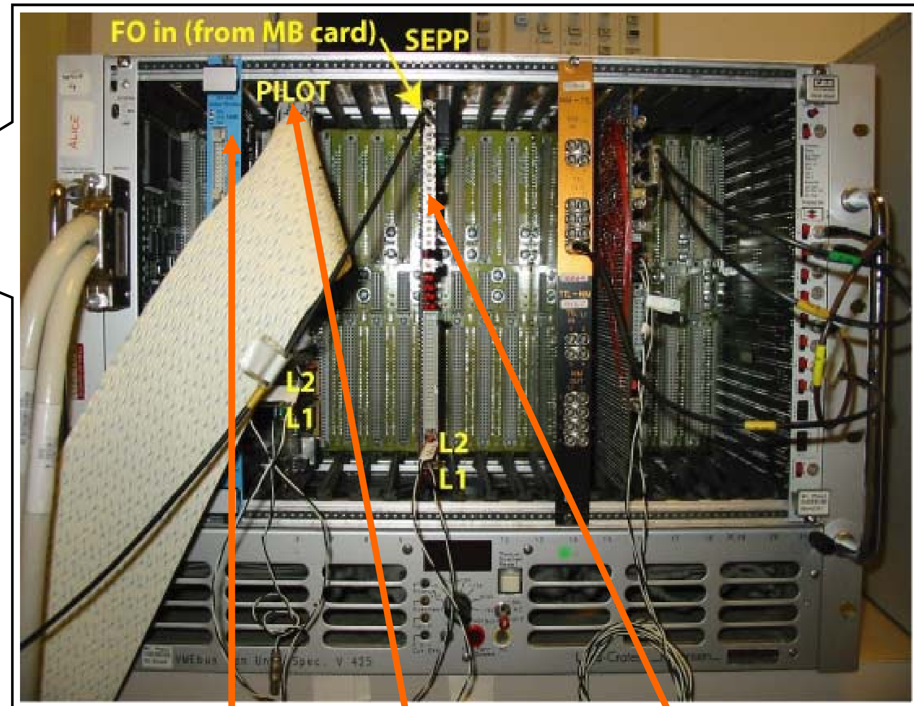
- Visual inspection of the detector surface:
  - required to detect surface defects, holes, deep scratches which could cause the detector not to work properly
    - if defects are absent/negligible → CLASS 1
    - If defects are serious (deep holes or scratches) → CLASS 3 not reworkable

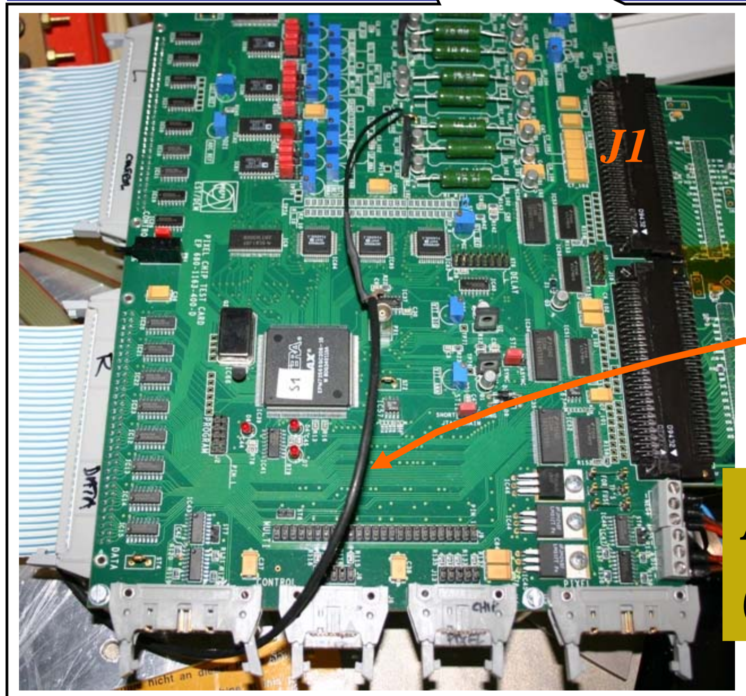
Average time requirement for a complete ladder test: 3.5 hours

Test apparatus



VME Crate





JTAG controller

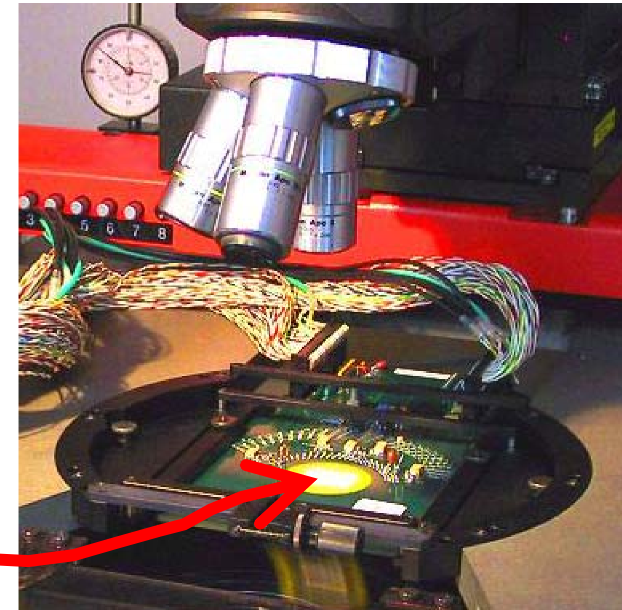
Pilot card

Card to manage Fast-OR trigger

MB card (chip control)

Cable to get Fast-OR signal

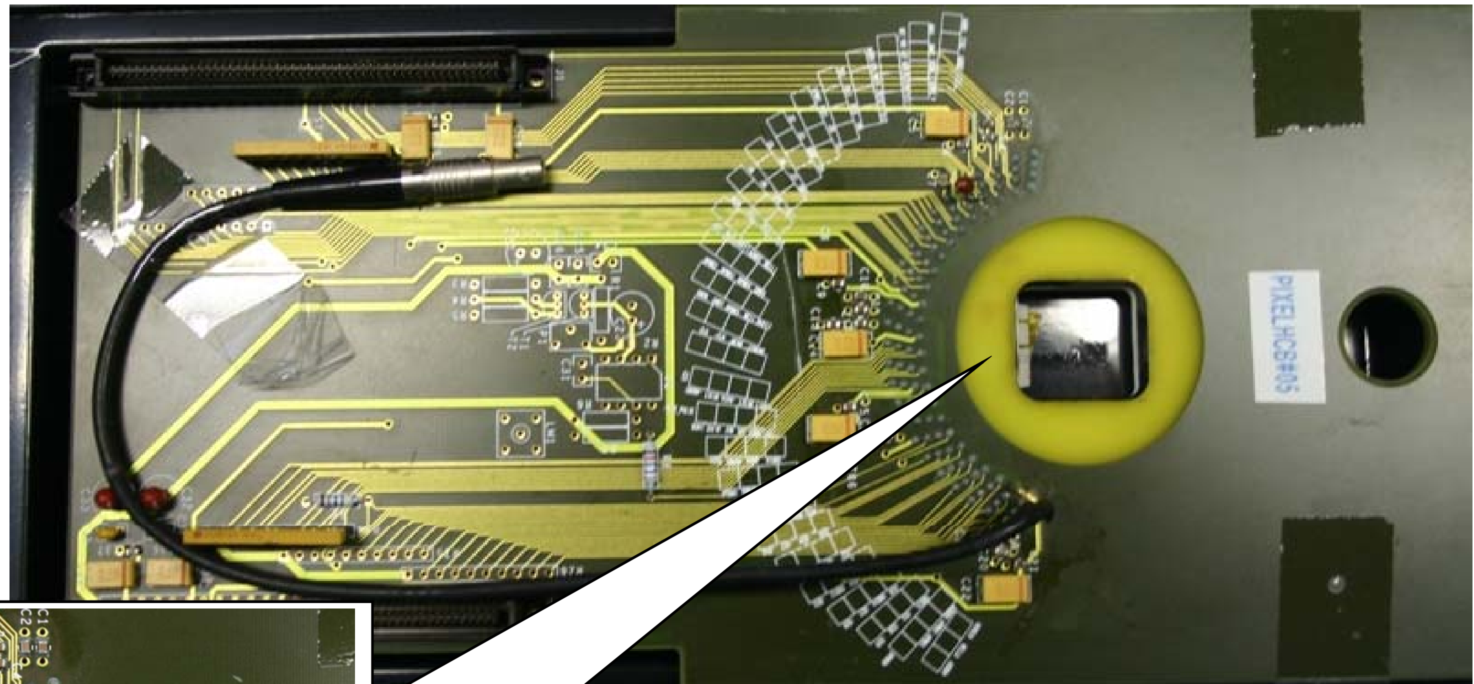
Probe station

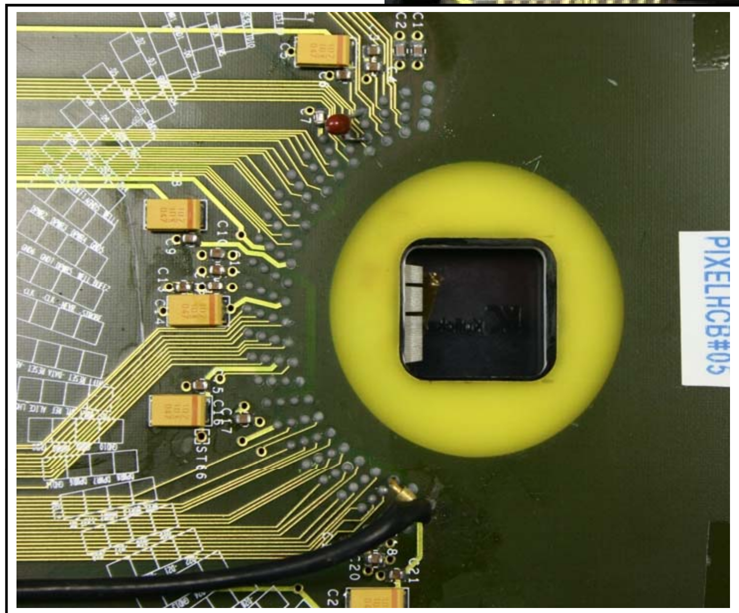


- Suppor for tested device
  - “chuck”
- Probe card with needles which create the contact with the tested chip

trace left by previous contact (re-testing)

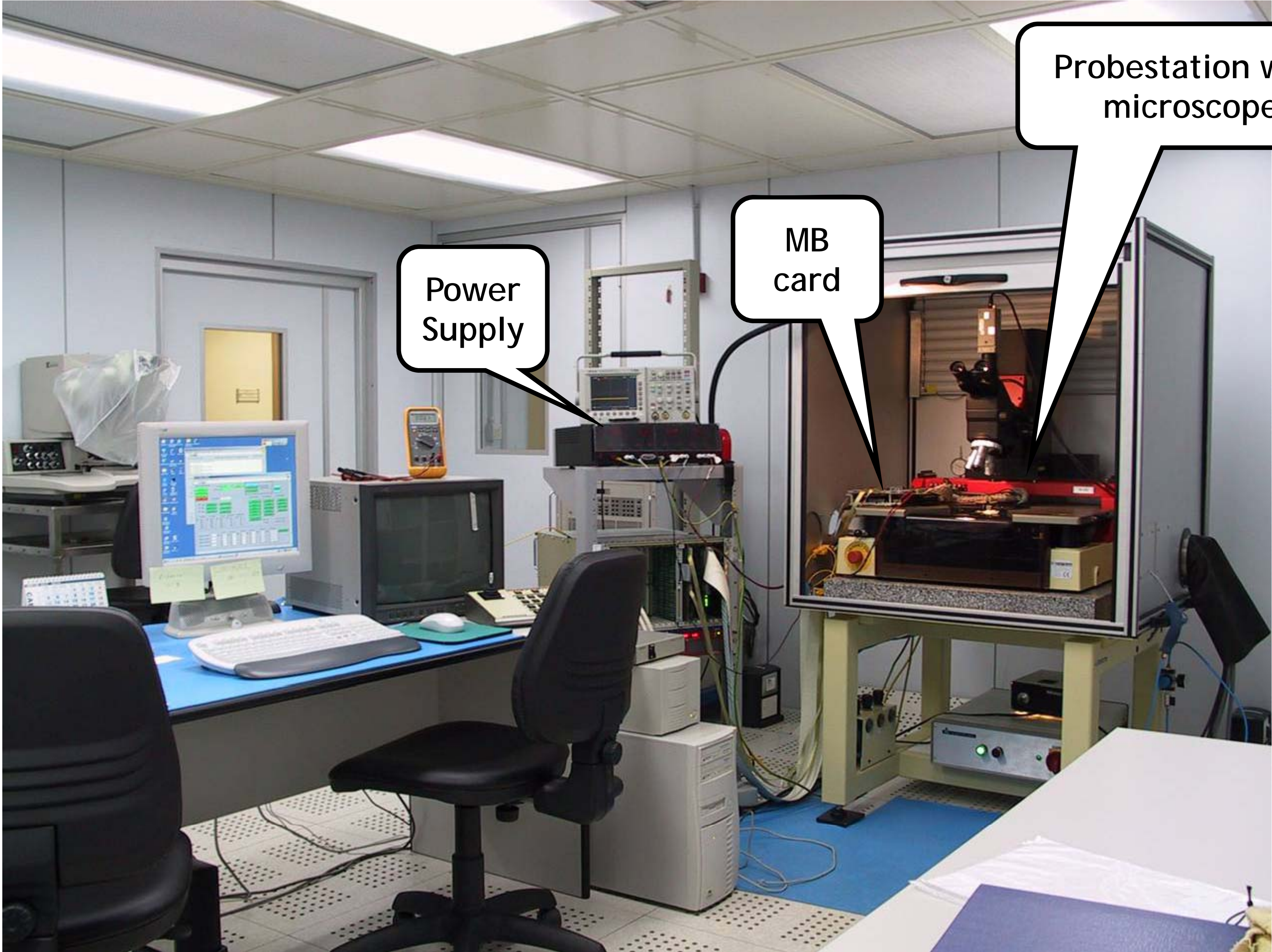
Probe card





1. ***103 microneedles, divided in 3 groups***
2. ***same needle spacing as chip pads one***
3. ***common ground (LEMO cable)***

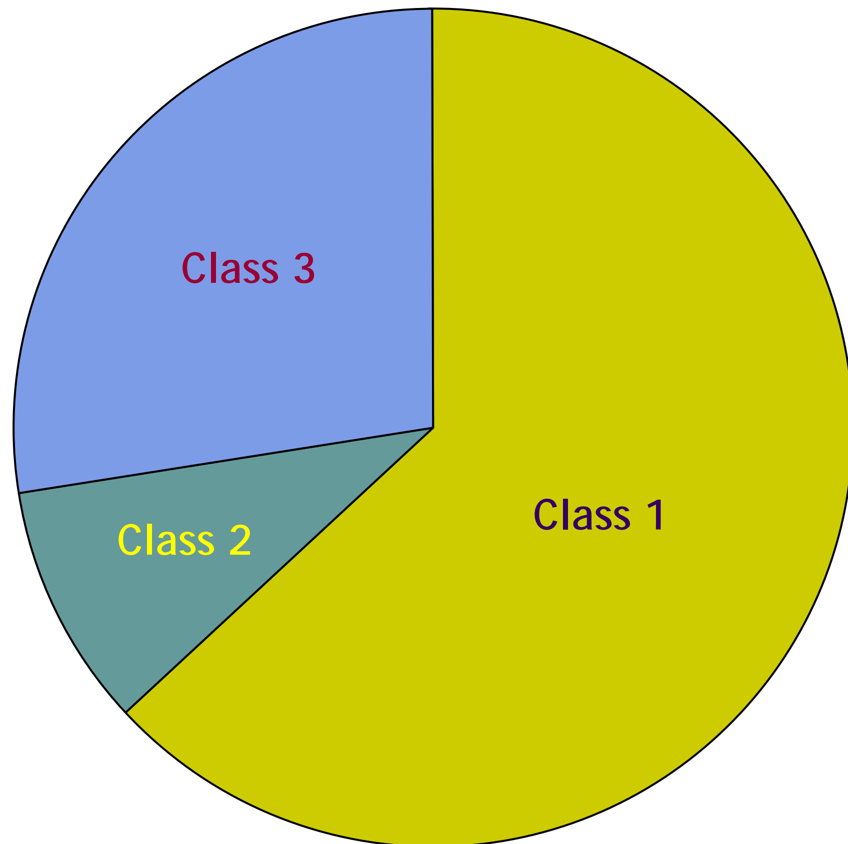
Clean room in Catania



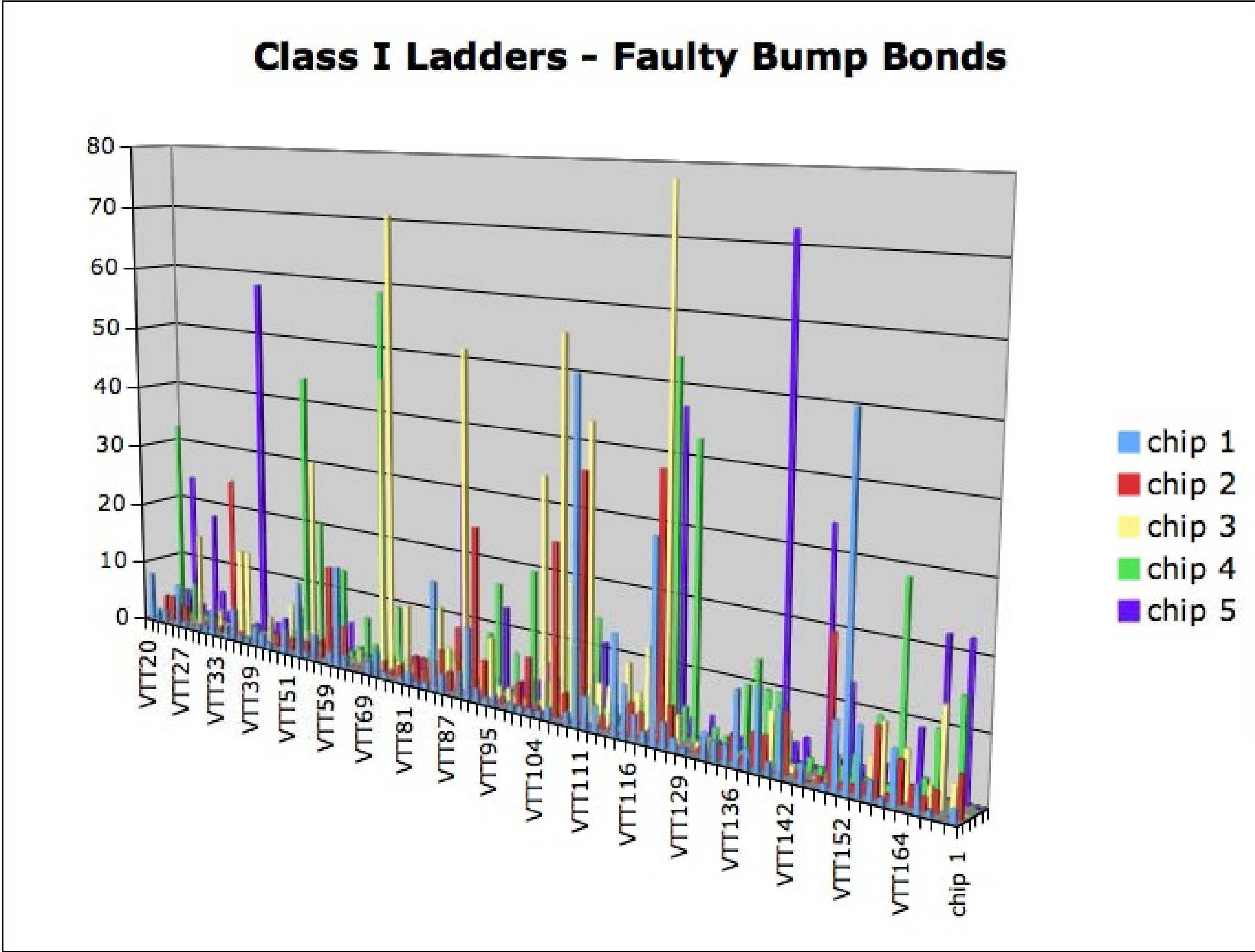
Test software: LabView application

Ladder tests in Catania: summary from November 2005 up to now

- 240 ladders tested:
  - 151 (= 62.9%) class 1
  - 23 (= 9.6%) class 2
  - 66 (= 27.5%) class 3



Statistics

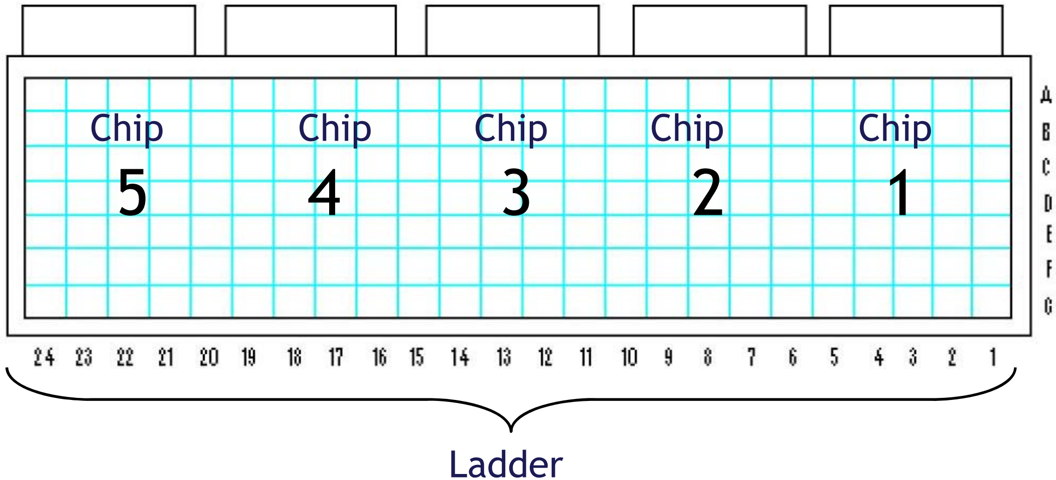


Statistics

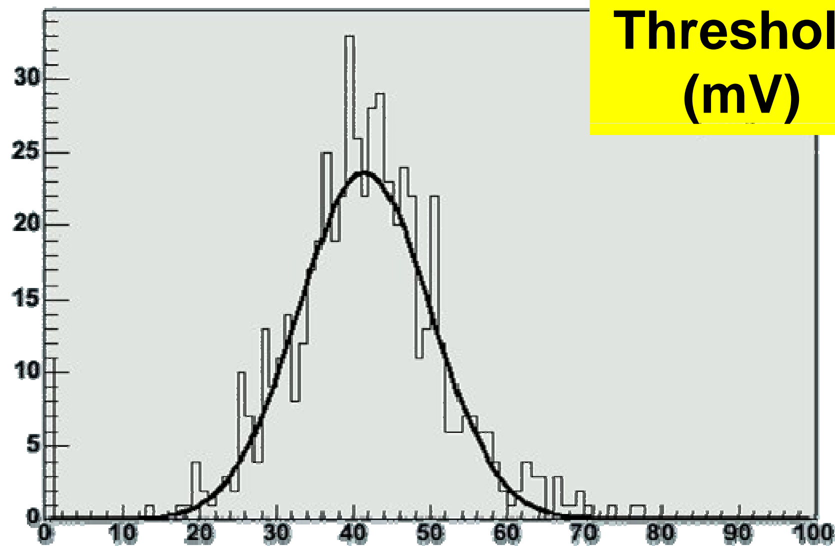
Average number of defects per chip position:

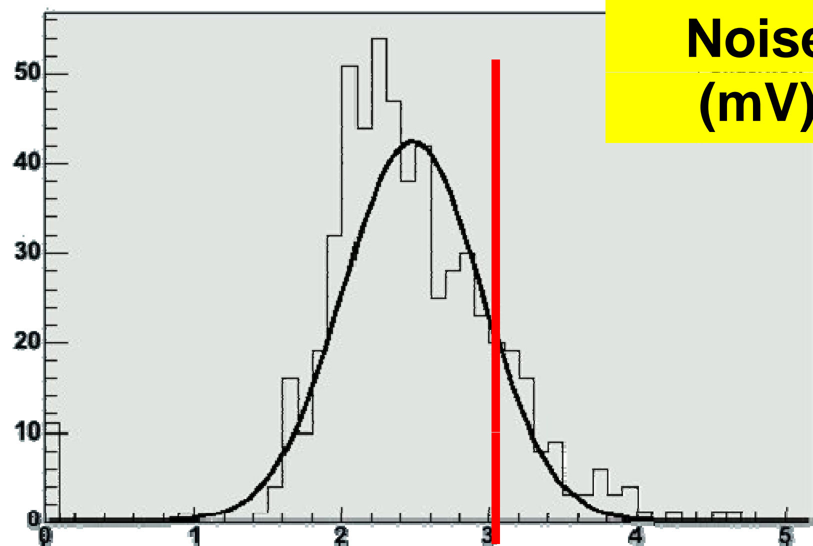
Class I ladders

Chip	1	2	3	4	5
Defects	5	4	8	7	6



Average min. threshold & noise





- Avg. Threshold:
  - *41.1 ± 0.5 mV ~ 2400 e-*
- Avg. Noise:
  - *2.45 ± 0.03 mV ~140 e-*
- Good *S/N* ratio
- Efficiency ~1 at experimental phase

Chips with avg. noise > 2.8 mV
→ 100 readout chips
- *82 from production lots #7 and #8*
- *avg. Noise = 3.15 ± 0.03 mV*

→ systematic effect due to production process

(source: Carmelo Digiglio – INFN Bari)

Dead pixels

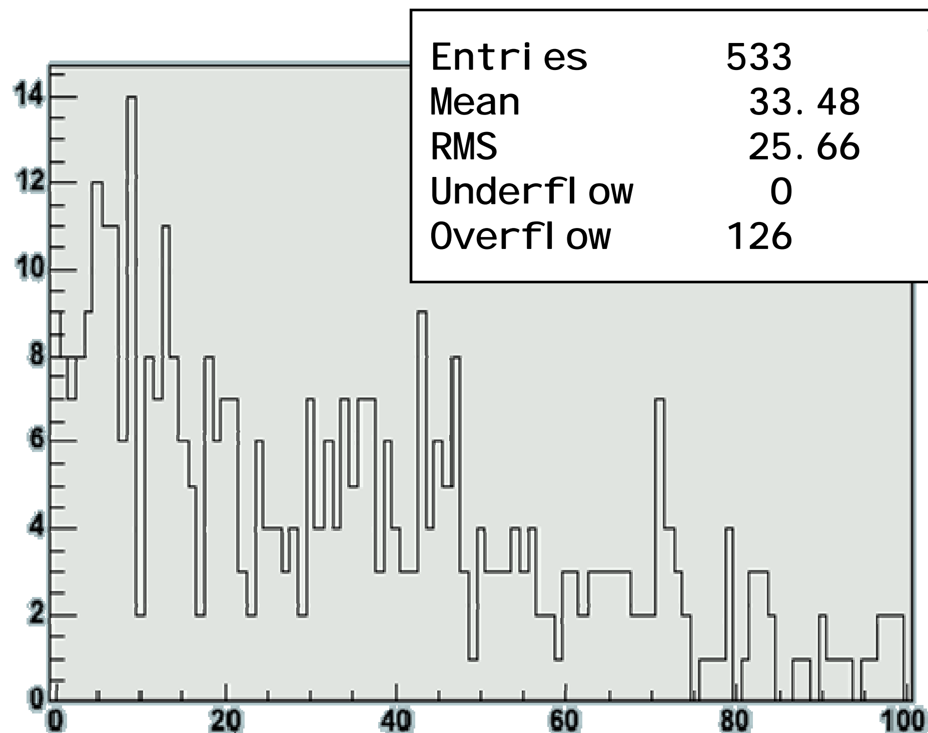
A pixel is “dead” when it does not respond to impulses given by pulse or source

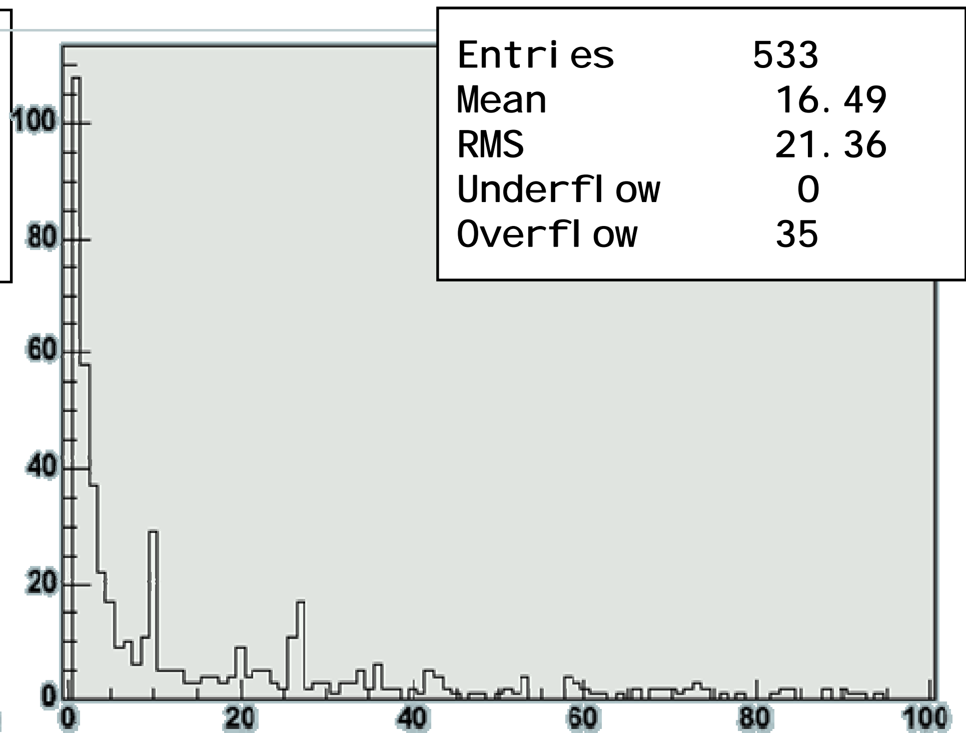
Dead pixels in source test
(chip + sensor)

defect in pixel response OR faulty bump-bonds

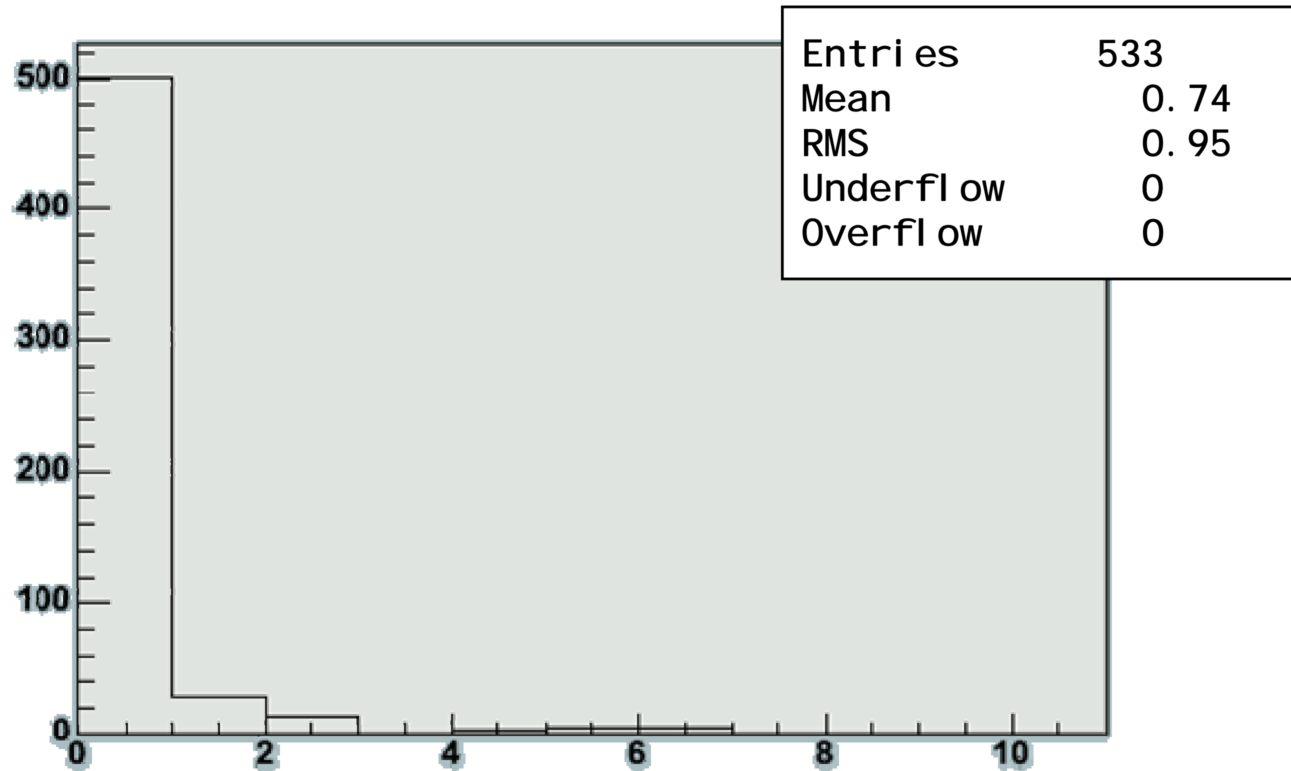
Dead pixels in pulse test
(chip alone)

defects in pixel response





Noisy pixels



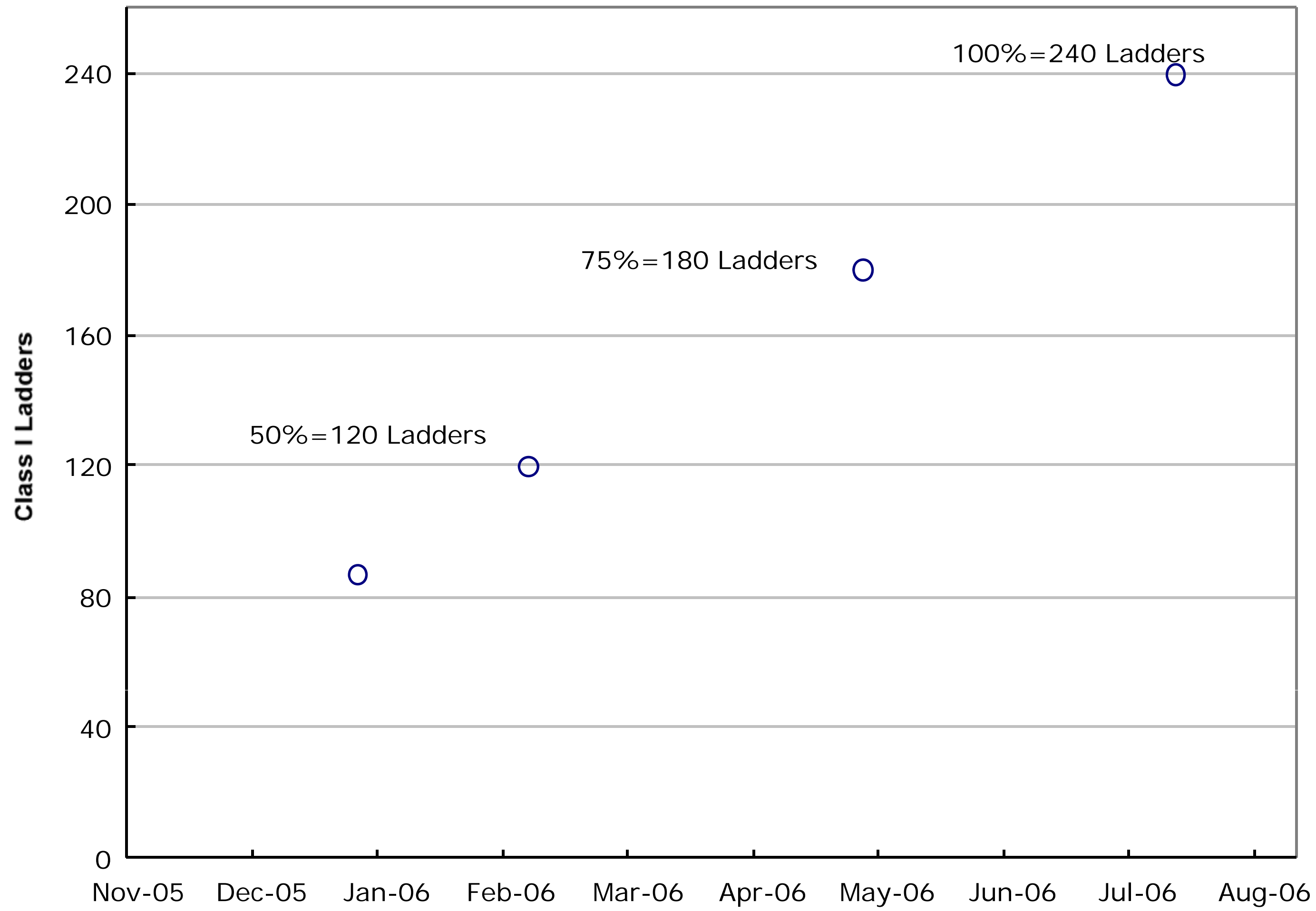
10^6 trigger signals sent during test phase

noisy pixels → #hits > 10^4 (1% of #triggers)

94% sample → 1 noisy pixel = 0.1‰ of total

Max number of noisy pixels in a single chip = 7 (0.08% of the total)

Ladder production



Summary

- SPD is a fundamental module for several purposes in ALICE event reconstruction.
- Building SPD requires an accurate testing procedure of each of its single components (ladders/chips), and for several aspects:
  - performances
  - defects
  - working parameters
  - PC – to – device communication
- Catania's group has given a large contribution to this testing activity, since 2004 up to the end of production required for SPD commissioning (first half of 2007).

- Future plans:
  - tests for spare modules
  - looking forward to start using them with LHC beam! ☺

- Thanks to Carmelo Digildo for contributions to the statistics plots

Thank you!