Development and test of an analog front-end electronic board for the NEMO neutrino telescope.

For the **Nemo** Collaboration

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Project Nemo Km^3: The study for a deep underwater neutrino telescope

Technological research for:

- Cherenkov light detector
- 1 Km^3 volume
- 3500 m beneath sea level

The aim of the detector:

- Look for astrophysical point-like sources of Ultra High Energy neutrinos (up to 10^{19} eV)
- Comprehension of accelerating laws
- Dark matter investigation

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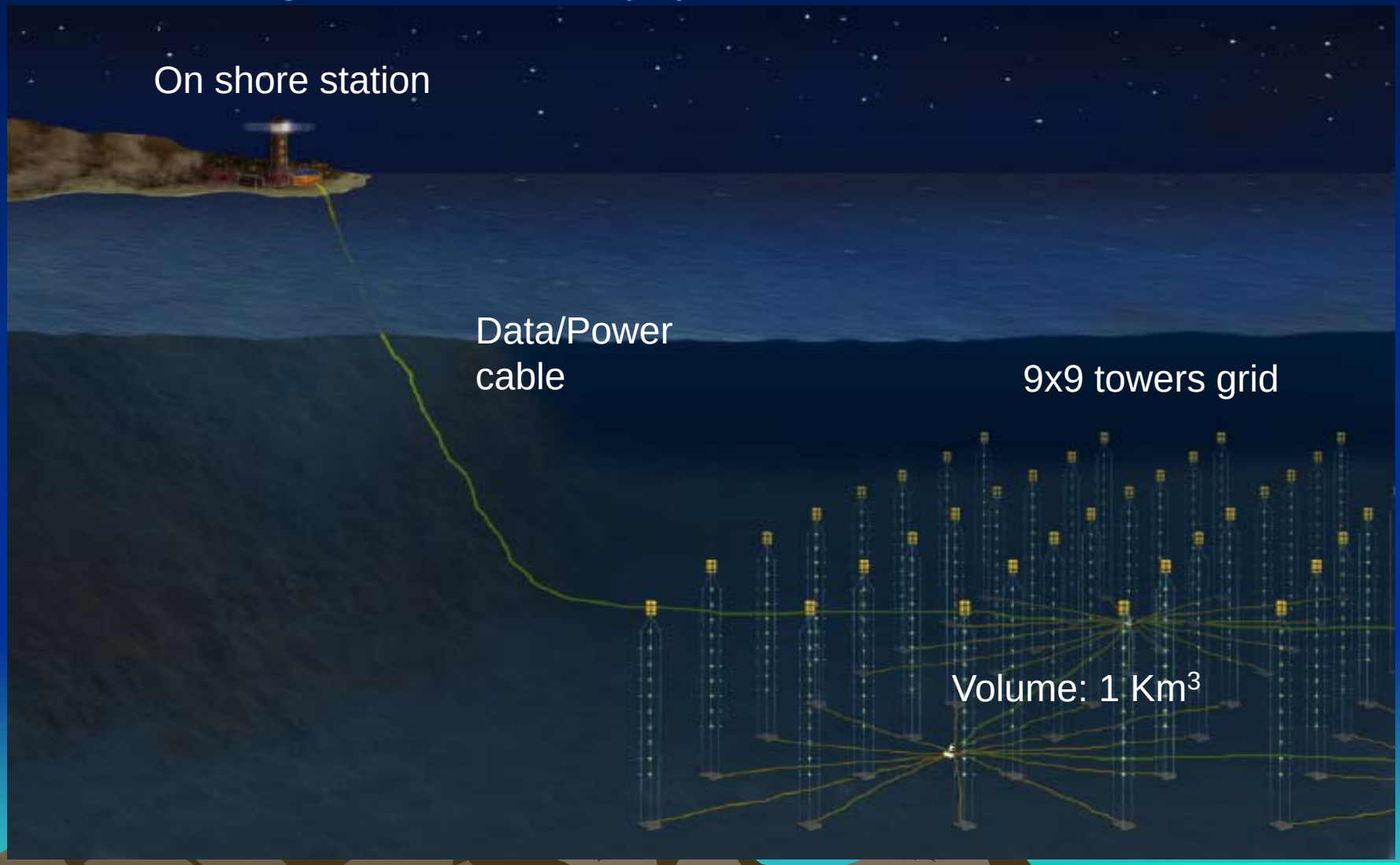
The proposed telescope:

A Cherenkov light detector to be deployed beneath the Ionian Sea.



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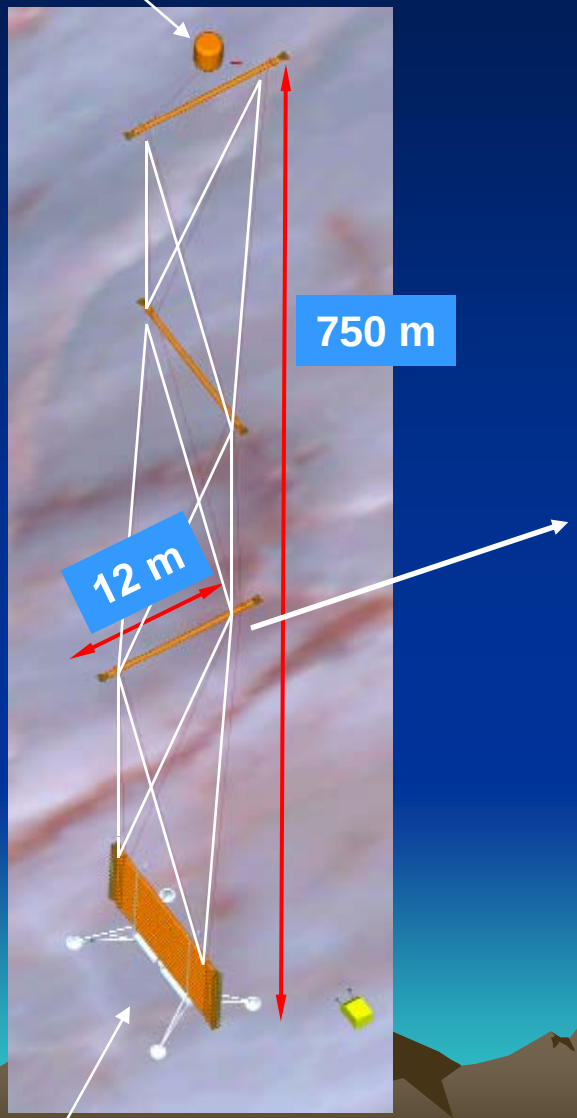
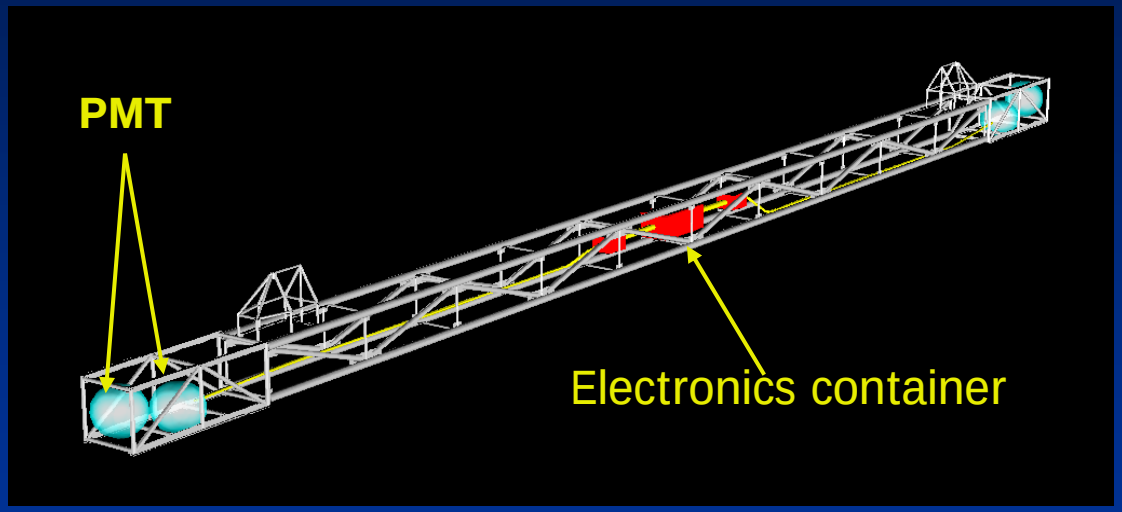
The tower structure





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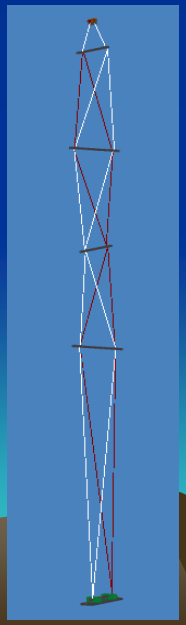
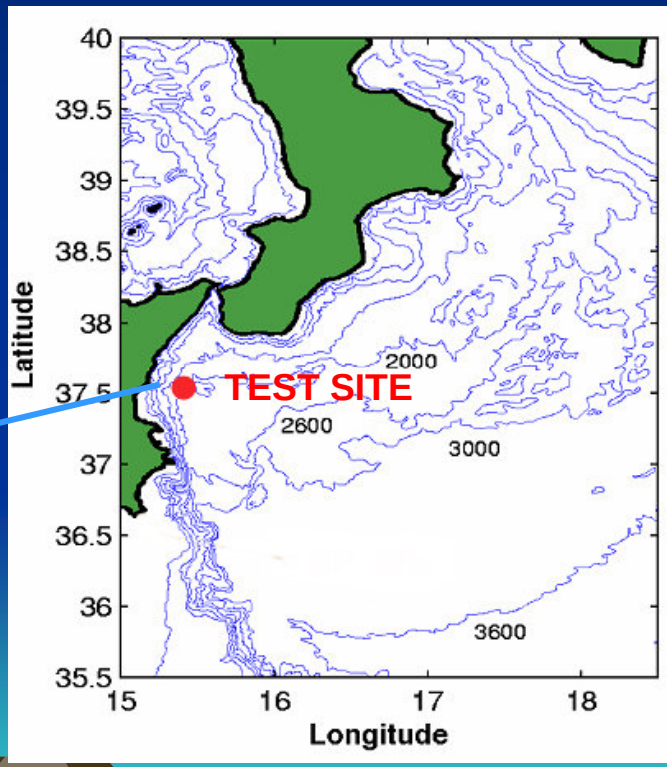
Test site: Nemo Phase -1

- A Single tower made up of **4** floors
- **4** PMTs per floor
- Deployed on December 2006
- Test site location: Catania, Sicily (2500 m depth)





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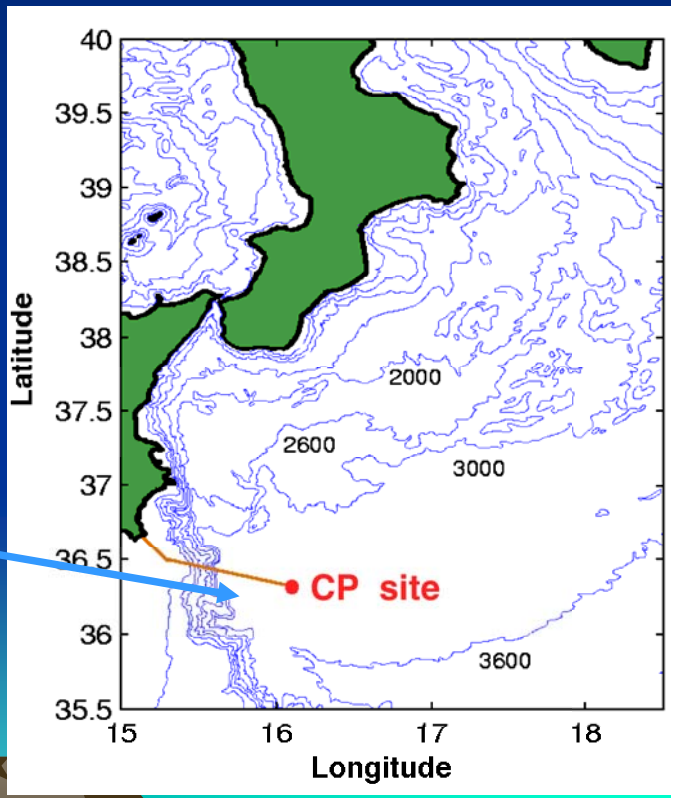
Nemo Phase - 2

- A Single tower made up of **16** floors (2 of which for new R&D projects).
- **4** PMTs per floor.
- Deployment scheduled end **2008** / beginning **2009.**
- Location: Capo Passero, Sicily. (3500 m depth)



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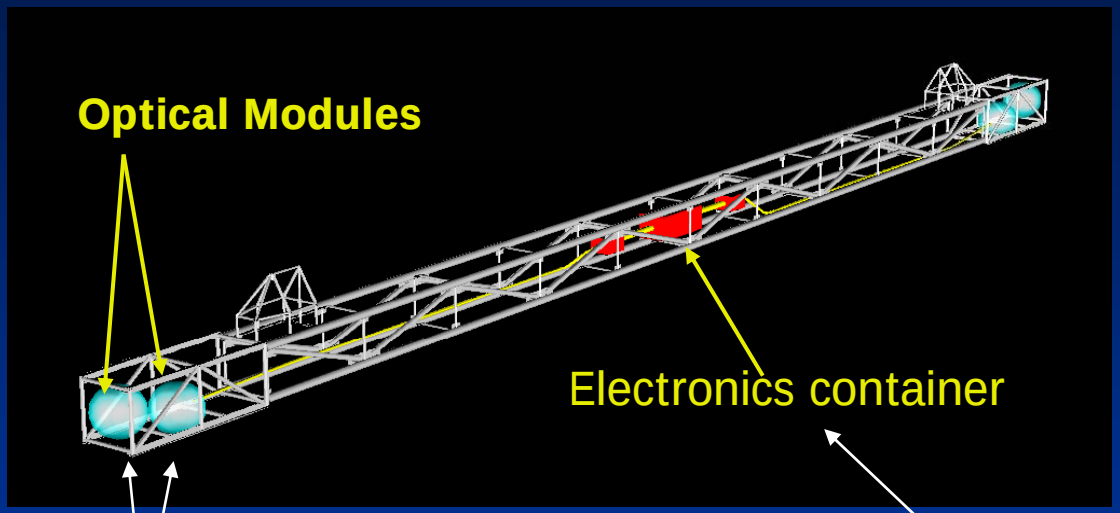
Present floor electronics

(Nemo Phase – 1)



(each)

+

PMT

Digital Front-End read-out electronics

Floor Control Module: 1° level concentrator

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The proposed new front end electronics for Nemo phase2 (R&D floor)

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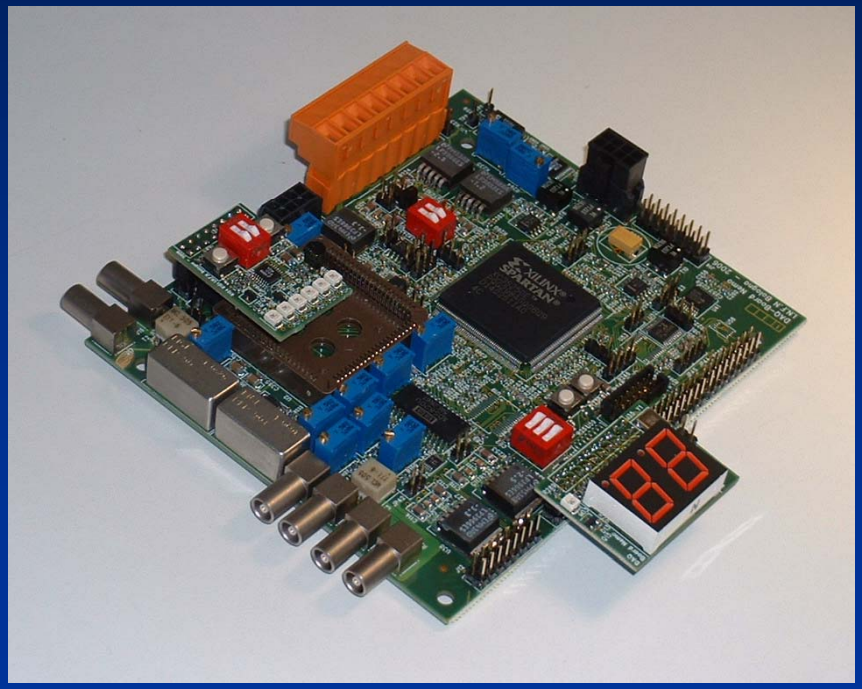

PMT and related high voltage supply electronics (same as present ones)

Data acquisition board with a socket for the **analog** sampling chip LIRA

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The aim of this board

- To give a digital control logic to the chip LIRA:
  (analog sampling ASIC developed by the INFN section of Catania).
  - High linear dynamic extension.
  - Low Power Consuption.
- To implement the data transmission protocol over the present data acquisition system.
- To realize a mechanically compliant board.
- To test the whole mixed-singal front end board solution.

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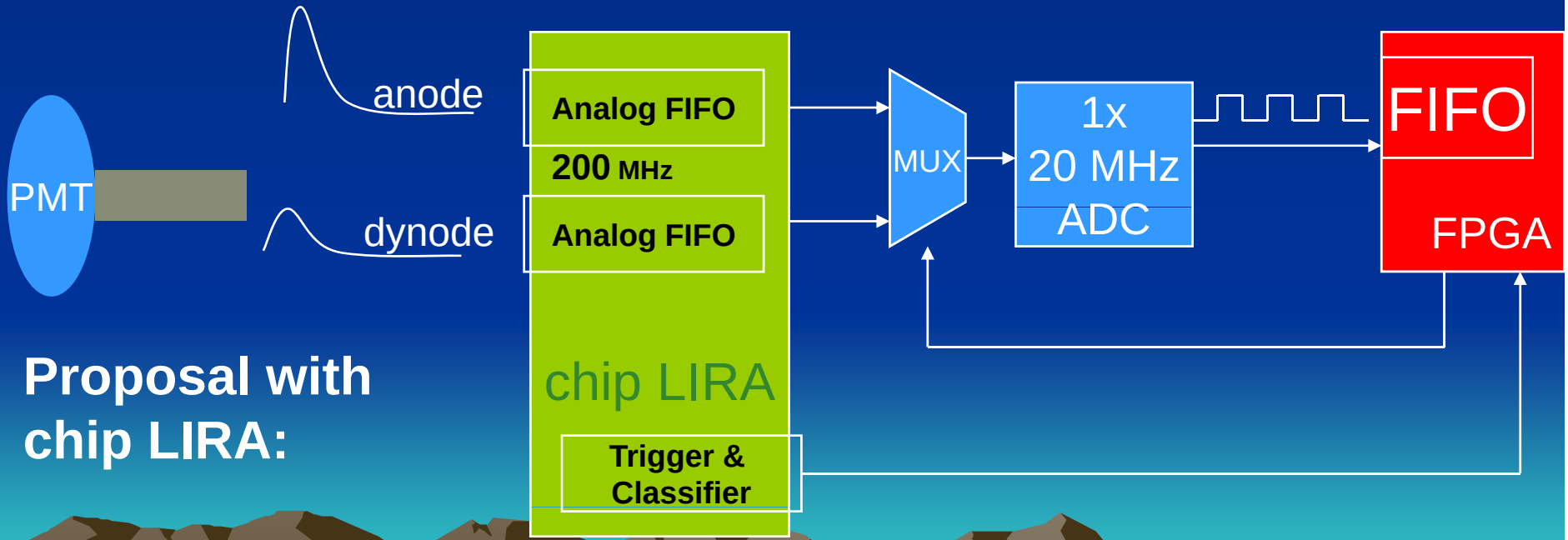
Digital and analog acquisition techniques

Nemo Phase1:



Proposal with chip LIRA:

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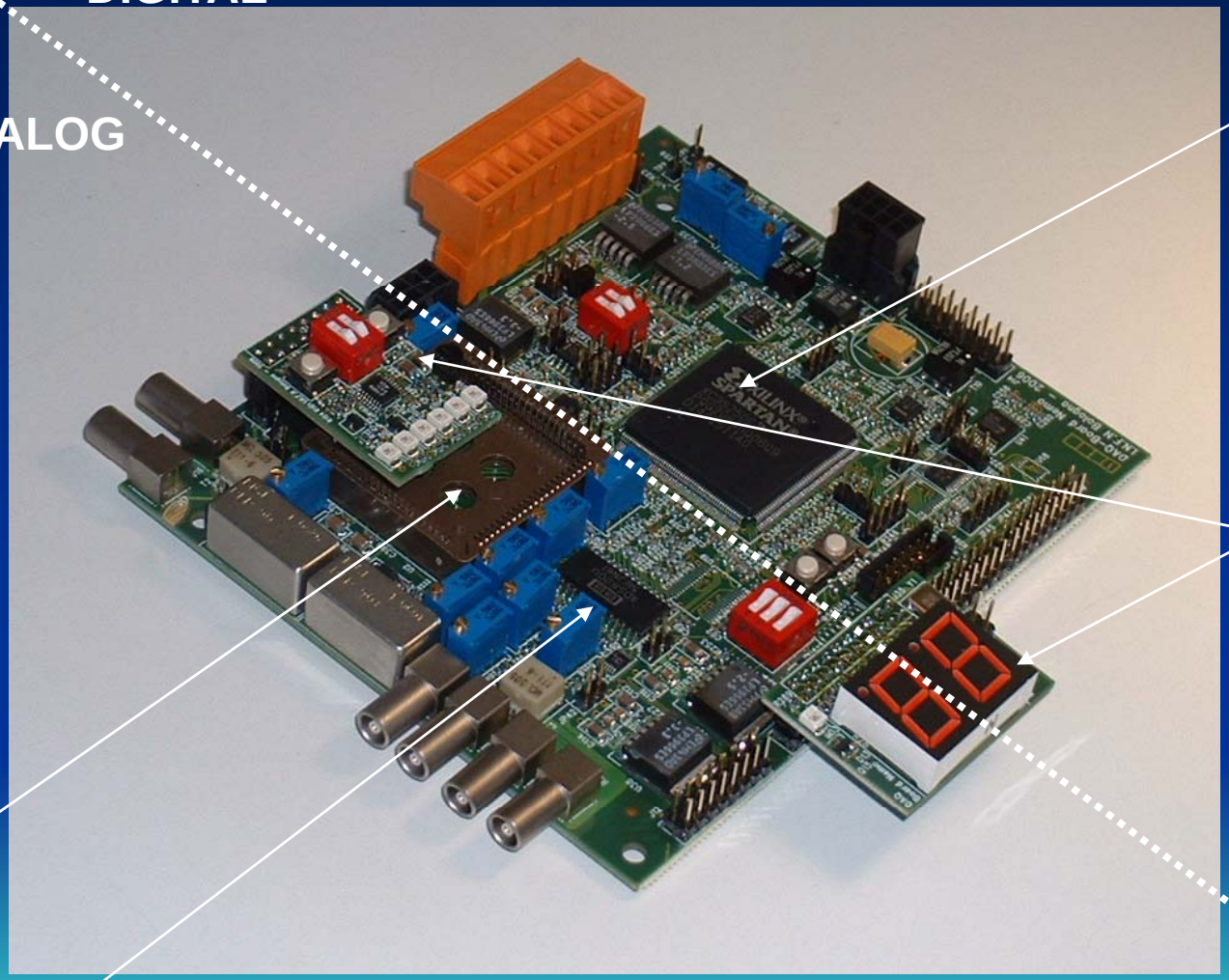
Board presentation



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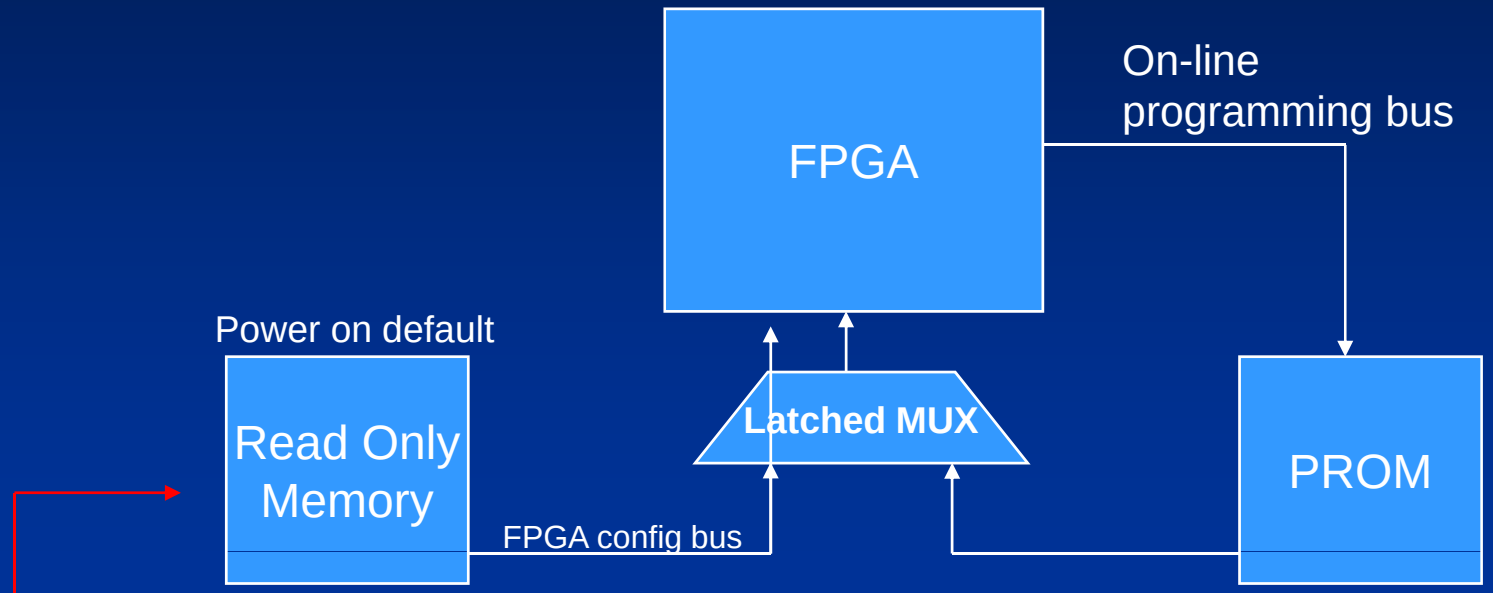
SAFE DUAL-BOOT

Architecture for a safe remote reconfiguration of the digital logic



on-line firmware flexibility:

- Minimizing extra logic components.
- Granting a safe post-upgrade reboot.

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Preliminary tests

- Power On test – OK (~700mW)
- Programming logic devices (FPGA & PROM JTAG programming) – OK
- System bootstrap (FPGA config. from PROM) – OK
- Logic test: demo firmware loaded and executed - OK
- On board PLL test (5Mhz x 4) – OK
- Debug modules test - OK
- Safe Dual Boot test - OK

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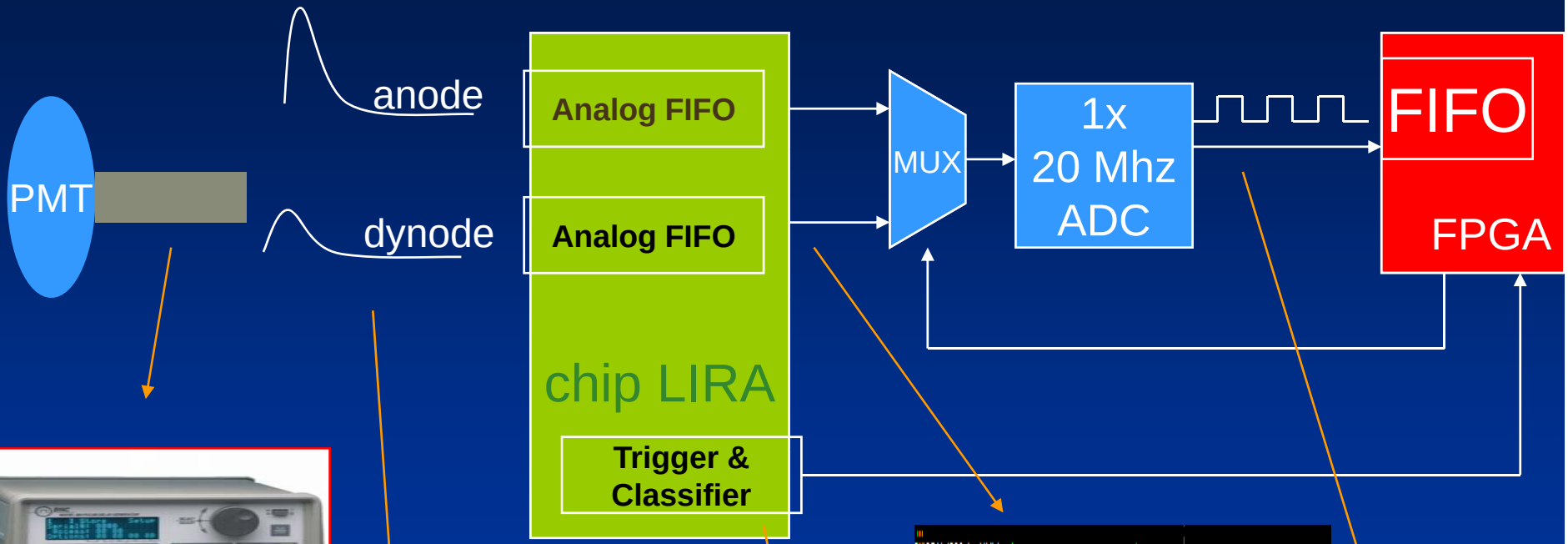
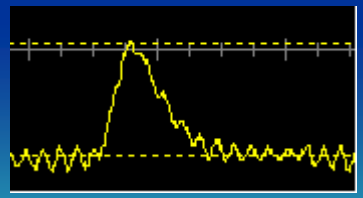
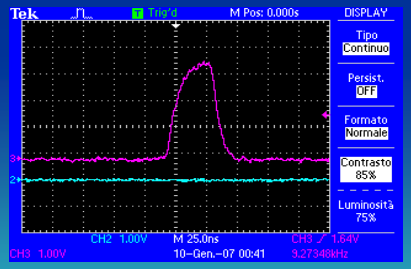
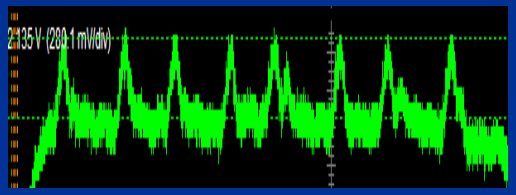
Acquisition test



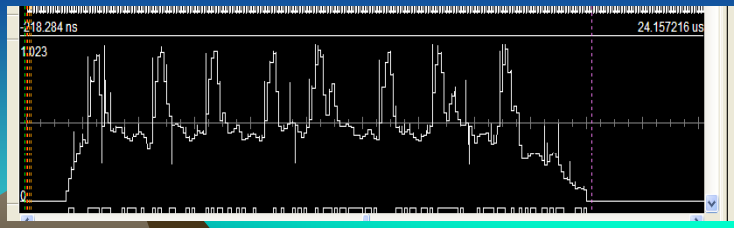
Waveform generator







Output (oscilloscope)



Output (digital)

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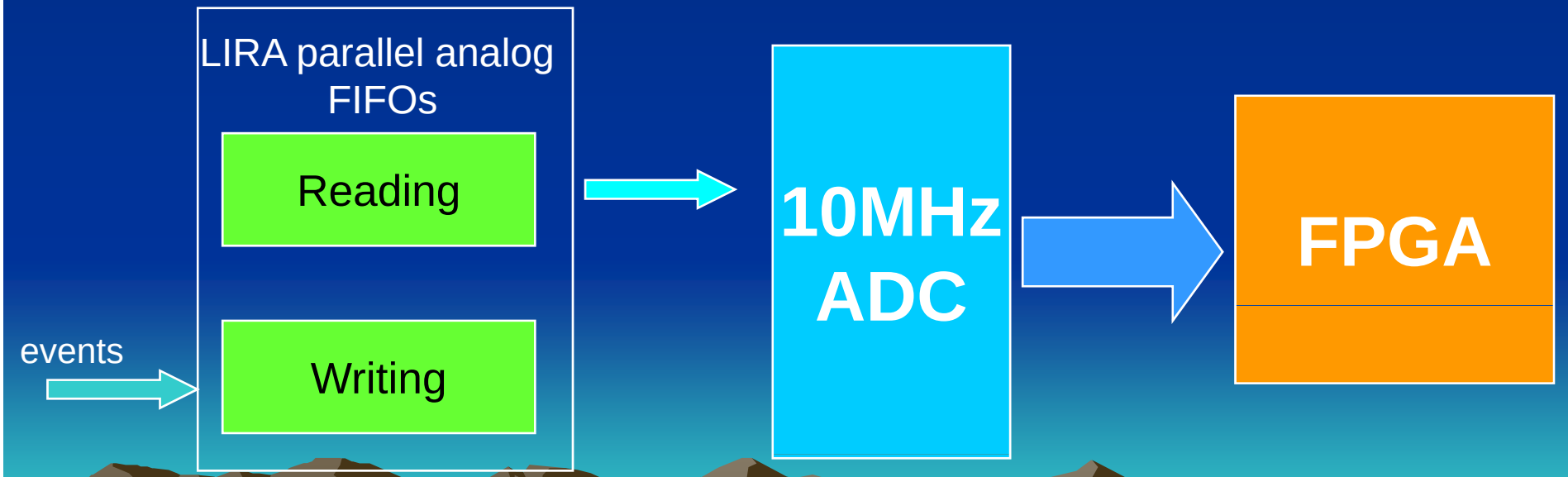
Testing LIRA driving firmware

Driving the acquisition process:

- Read/write cyclic loop of the chip LIRA – (OK).
- Analog to digital conversion of the samples – (OK).
- Digital noise reduce the quality of the reconstructed signal.



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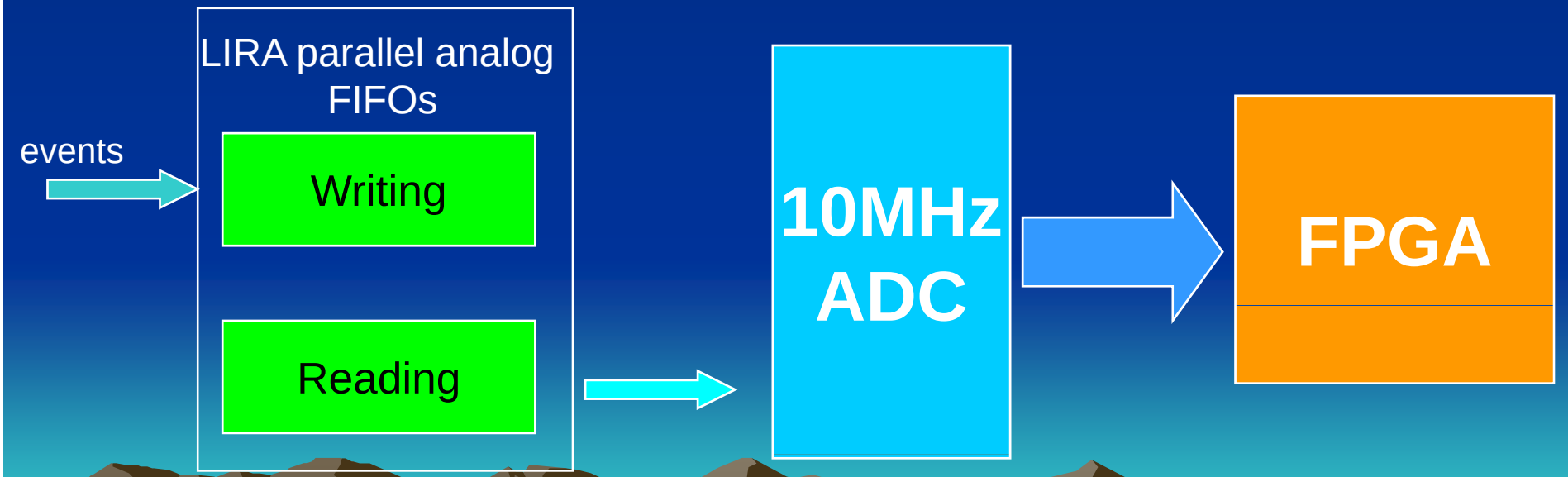

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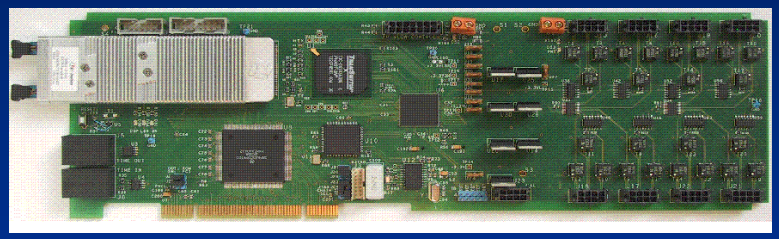
Communication test bench

Floor Control Module OFF Shore

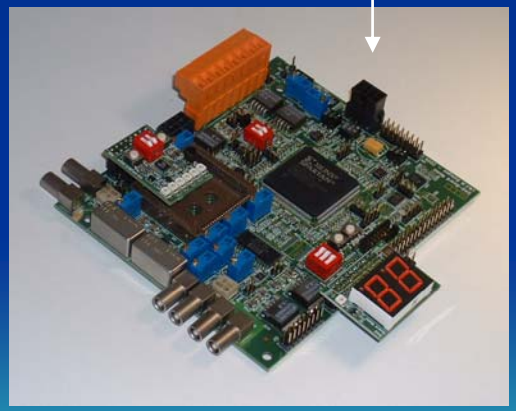
Fiber optics

(15 db attenuators)

Floor Control Module ON Shore



Twisted pair cables



Daq board with chip LIRA

PCI bus connection

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Communication test results

- Slow Control protocol working properly
  - Periodic Data Packet – OK
  - Remote command execution – OK
  - Error Check – OK
- Data sending
  - Some problems in data transmission - under investigation.
- Timing
  - Time stamp – OK
  - Synchronization of the time counter - OK

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Conclusions

- Analog fast acquisition and slow data conversion working properly.
- Communication towards and from the concentrator is established.
- Reached the compatibility over the present data transmission system.

Further improvements

- Sensor peripherals must be added to monitor the environmental parameters.
- Optimization in choice of commercial components to lower power consumption.
- Realization of a new board with the newest chip of the LIRA family: SAS chip (ref. Lo Presti presentation).
- Digital noise reduction.

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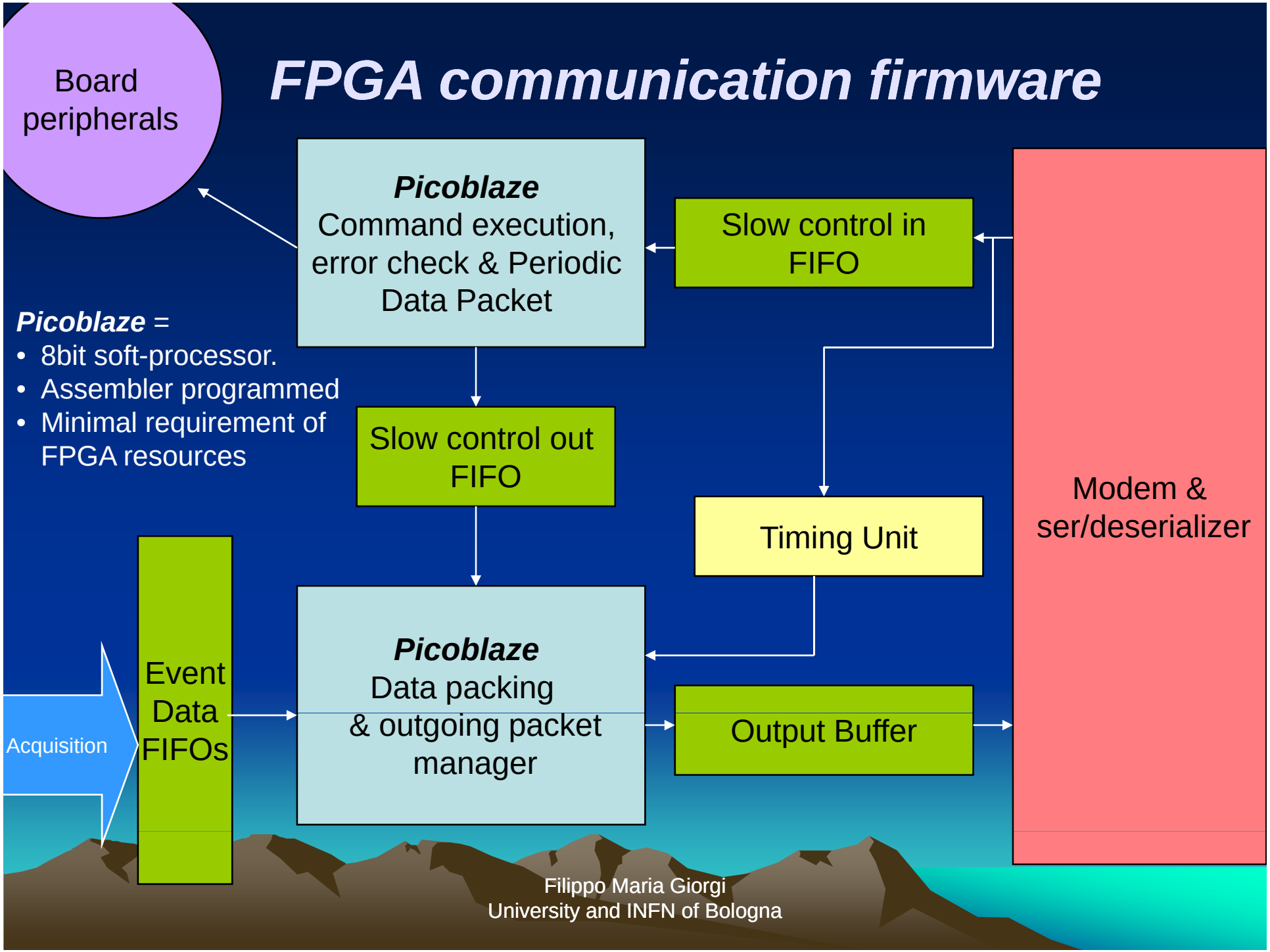
Power consupmtion (mW)

PLL on Board	70
PLL embedded FPGA	50
LIRA digital	100
driver rs485	10
driver lvds	30
clock driver	165
Output FPGA	35
core FPGA	50
ADC	10
LIRA analog	100
Voltage regulators (6)	100
TOT	**720**

FPGA communication firmware



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