Low Power Front End for the Optical Module of a Neutrino Underwater Telescope

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Summary

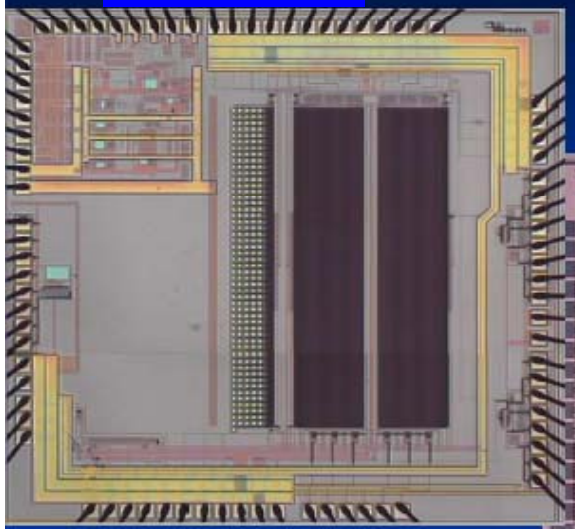
- Front end electronics for a Km^3 submarine neutrino detector:
  - LIRA chip
    - Test of the first prototype of the Front-end using LIRA chip (CT-BO) see F. Giorgi talk
  - Study and design of the new front-end
  - Specifications
  - Architecture
  - Status of work

LIRA Chip

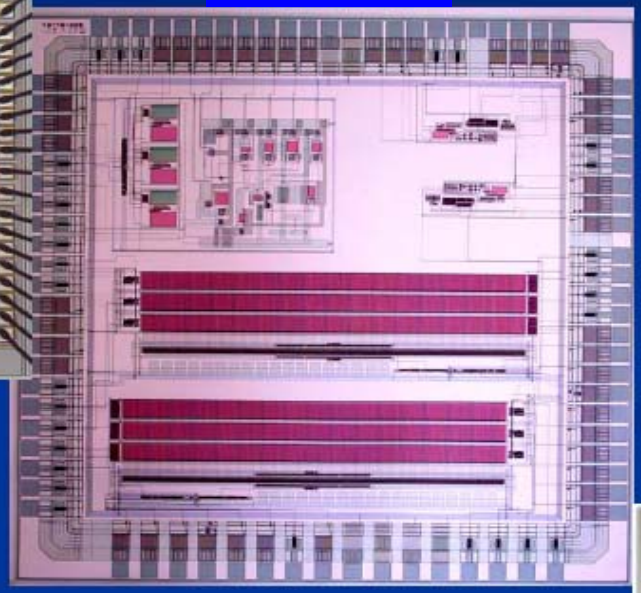
LIRA01 and LIRA02

Not Submitted to foundry

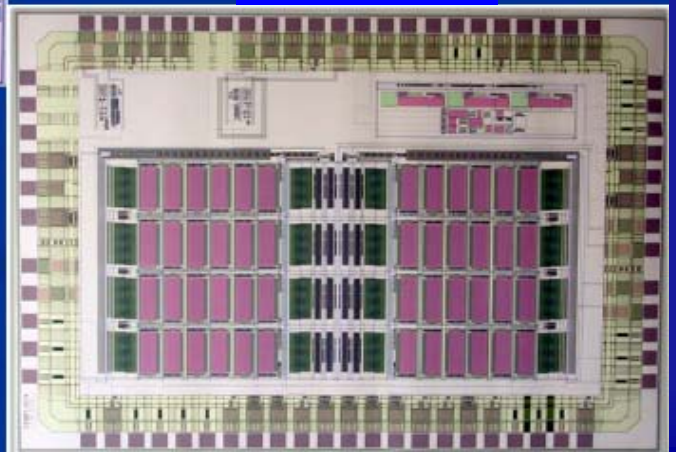
LIRA03



LIRA04



LIRA05



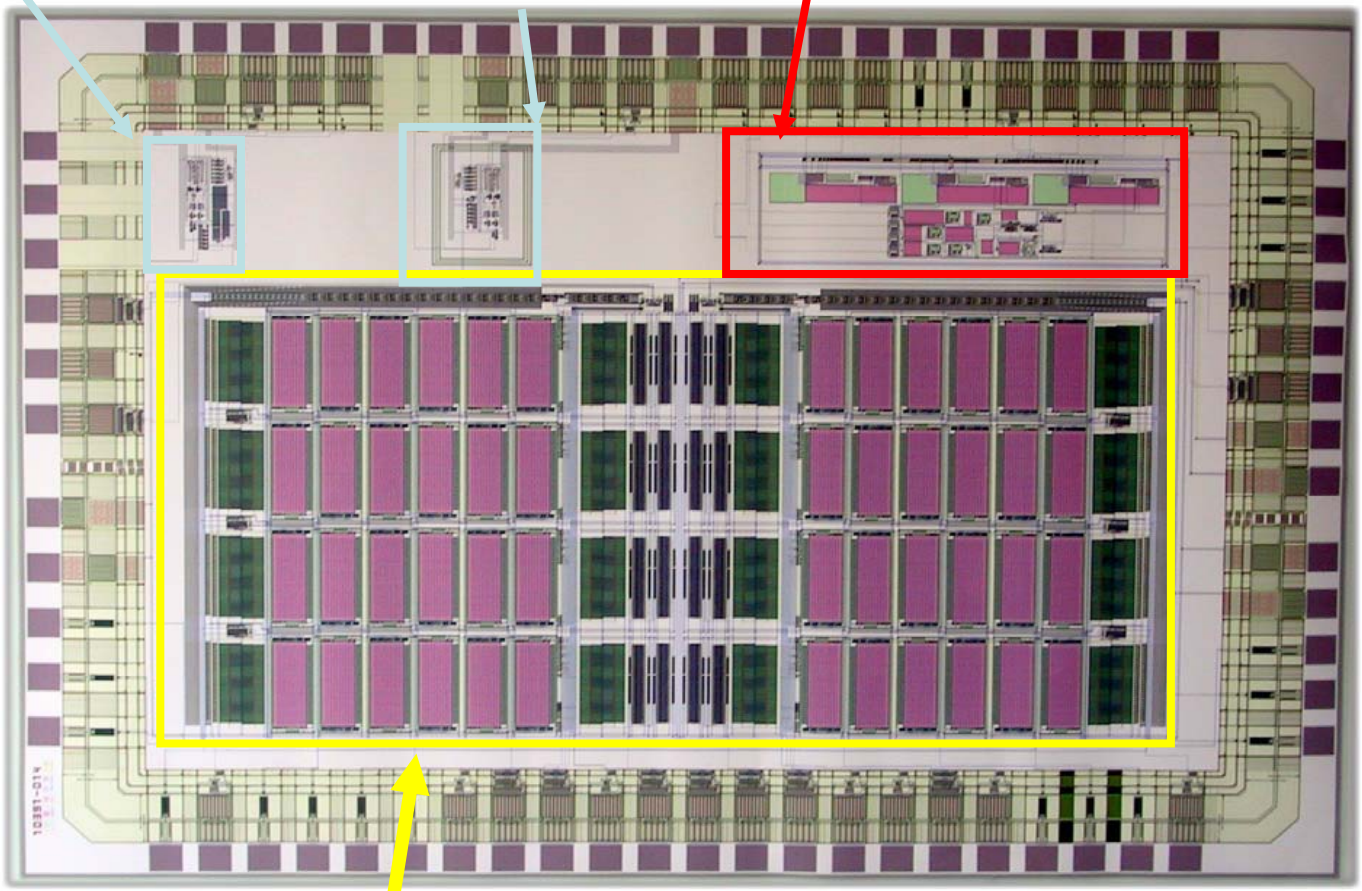
AMS 0,35 µm CMOS Technology

Europractice MPW

PLL Stand Alone 400 MHz
Slave Clock Generator

LIRA's PLL
Shielded

Trigger and Single
Photon Classifier TSPC



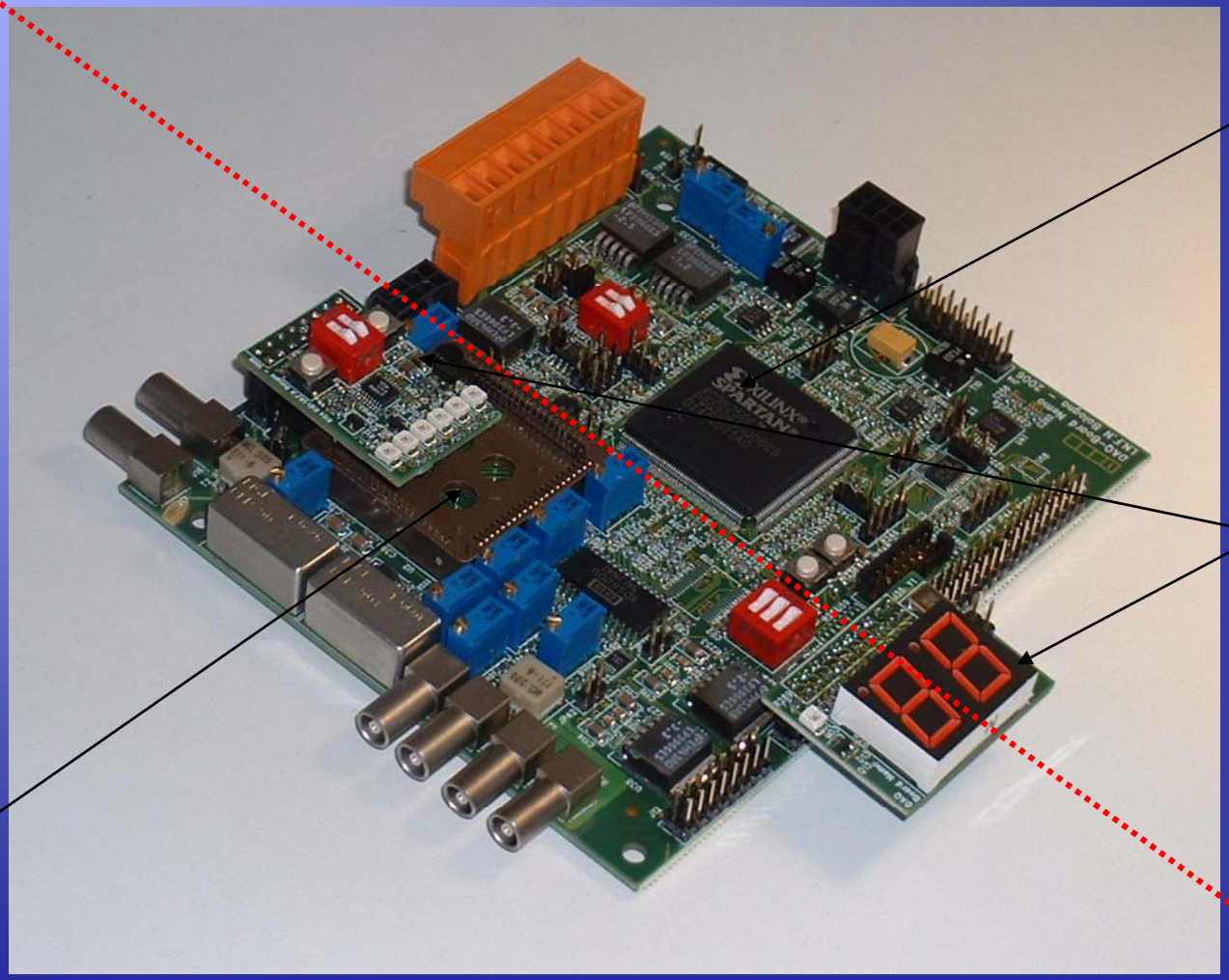
2 AM 200 MHz Write 10 MHz Read

LIRA05 CHIP CMOS 0,35 μm AMS technology

LIRA Chip

- 2 SCA 3 ch.x256 cells working alternatively in read and write mode to reduce dead time
  - 200 MHz sampling 10 MHz transfer
  - 9 bit resolution
  - Anode and last dynode sampled (double linear dynamic)
  - 20 MHz master clock sampled for time stamp
- Trigger and Single Photon Classifier
  - 3 5-bit DAC with slow control interface
- PLL to produce 200 MHz on chip
- 120 mW total power dissipation!!

Front end using LIRA chip



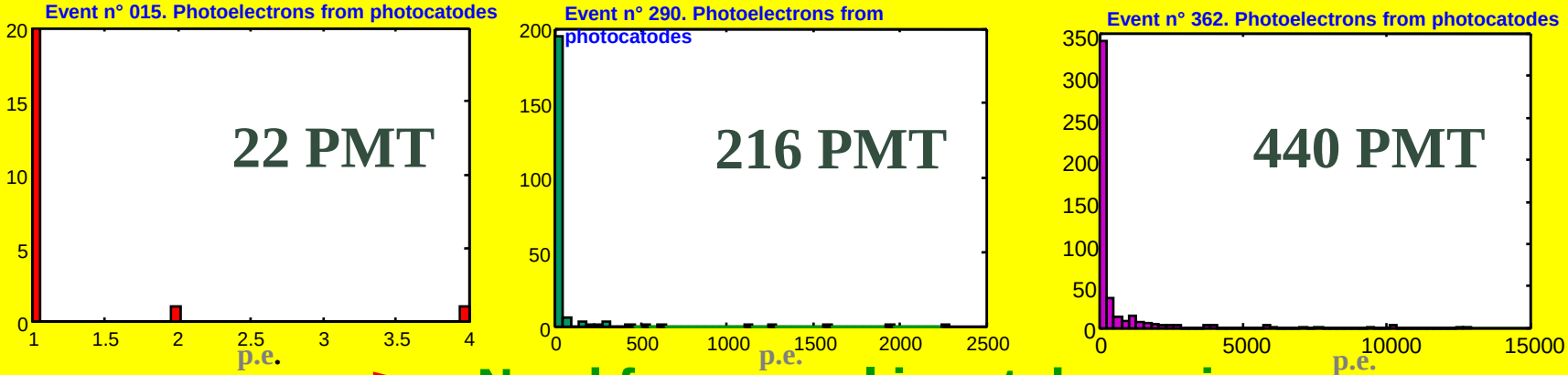
See F. Giorgi talk

Simulations

- High energy neutrino events in NEMO detector
- ^{40}K spe background
- Seawater Optical properties
- Optical module spacing, orientation and position
- Hits in each pmt of the detector in presence of an event

Charge Dynamics

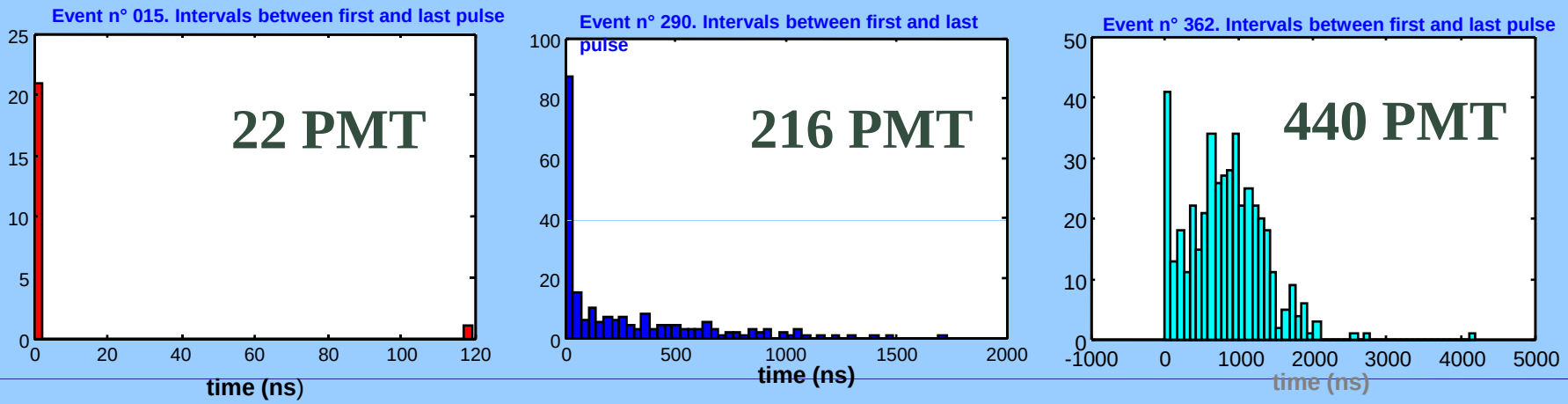
p.e. spectra of three typical high energy neutrino events



Need for several input dynamics

Time Dynamics

Maximum signals length spectra of three typical high energy events

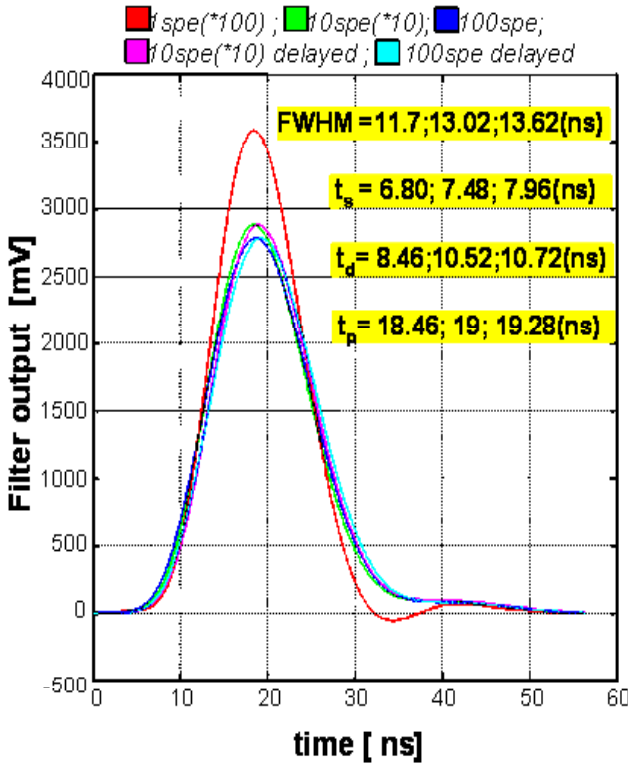


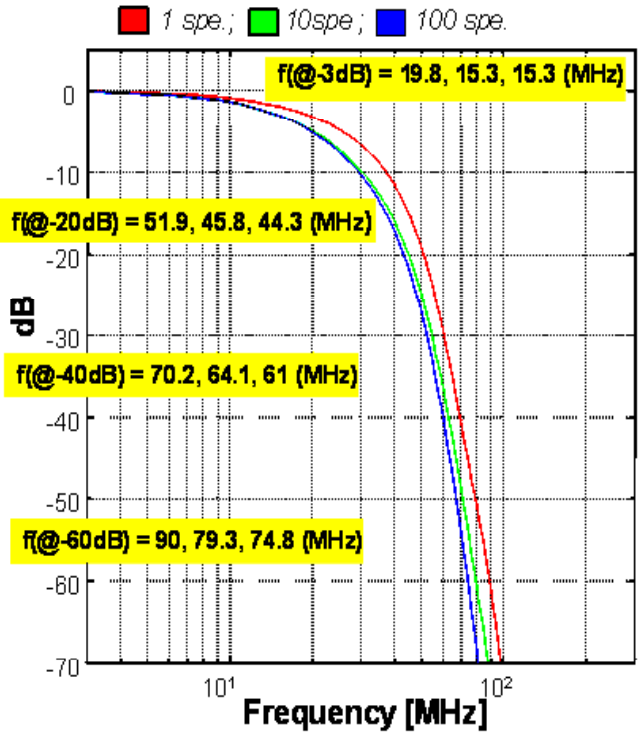
Specialized Samplers

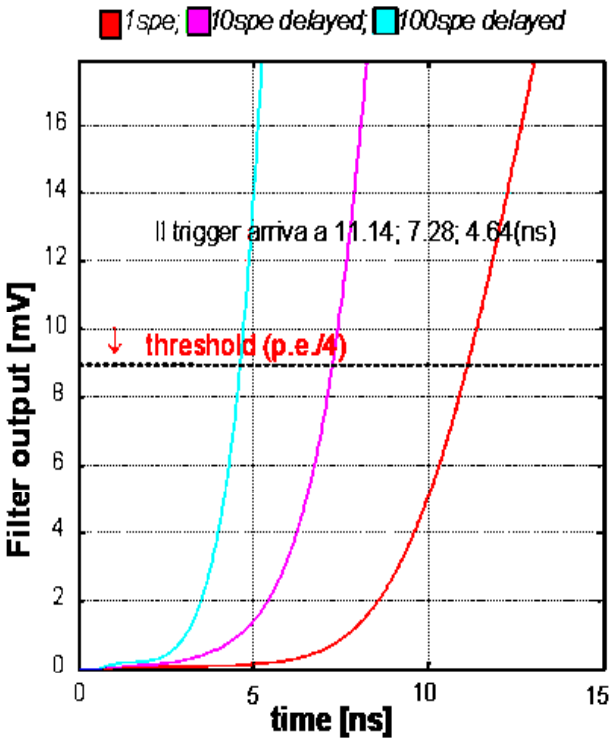
Study and Design of the Front-End Electronics

- **Simulation of neutrino events in a realistic detector (NEMO like)**
- **Simulation of the real Optical Module response**
- **Optimal Signal Filtering**
- **Simulation of the Front-End chain with realistic performances**
- **Evaluation of the detector performances as regards to acquisition parameters**
- **Considerations on Power Dissipation and data flow**
- **ASIC design**

Filtered PMT Signal







Typical filtered signals (1, 9.3 and 94 p.e.).

A ¼ p.e. threshold gives a fluctuation of about 7 ns. We foresee to sample 2-3 leading edge zeros and 2-3 trailing edge zeros. Signals must be delayed respect to trigger with a delay line.

The filter is necessary to avoid aliasing at 200Msample/sec.

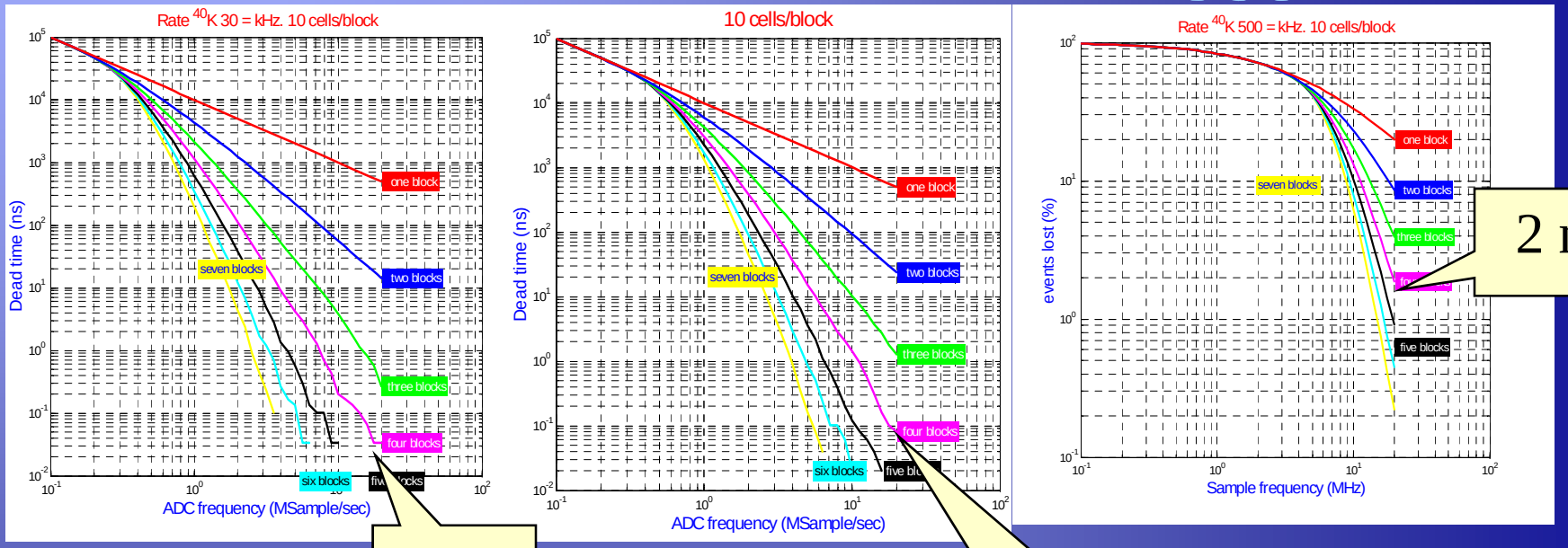
Signals measured with $PMT_{gain} = 5 \cdot 10^7$. PMT works not linearly for high photons levels.

It is useful to reduce the PMT gain to achieve a greater linear dynamics.

Lower ageing of PMT!

^{40}K Rate vs Readout frequency

30kHz 50kHz 500kHz

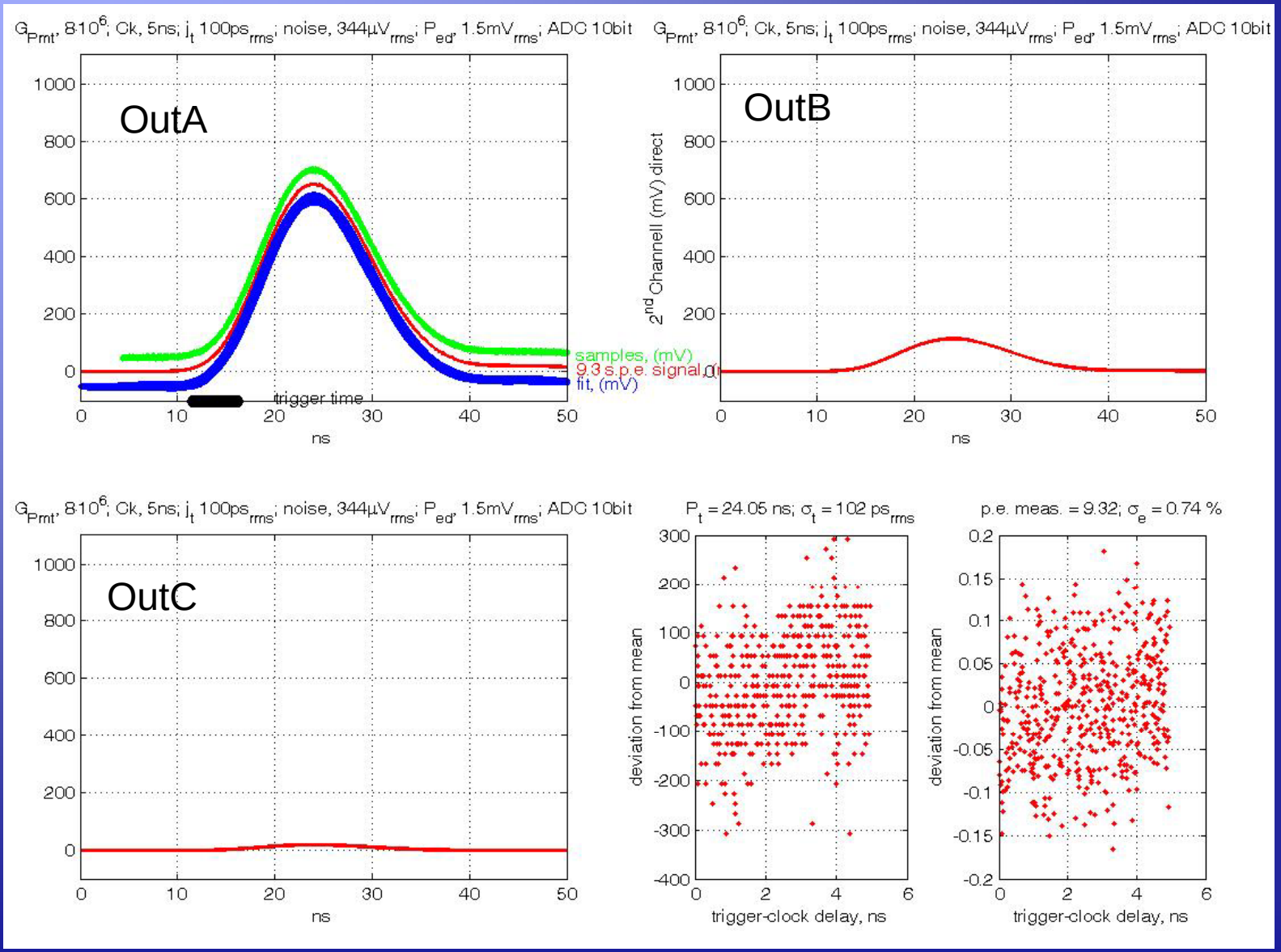


Dead time vs. ADC freq.

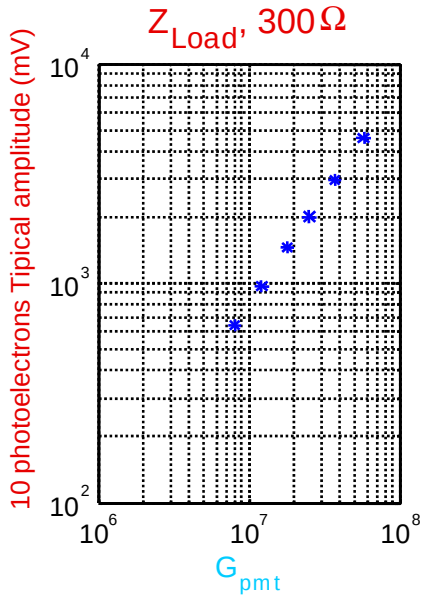
We must use a buffer solution to limit dead time.
A p.e. signal is long less than 40 ns. At 200Msample/sec we will use 10 cell blocks.
We have simulated dead time vs block number for different ^{40}K rates.

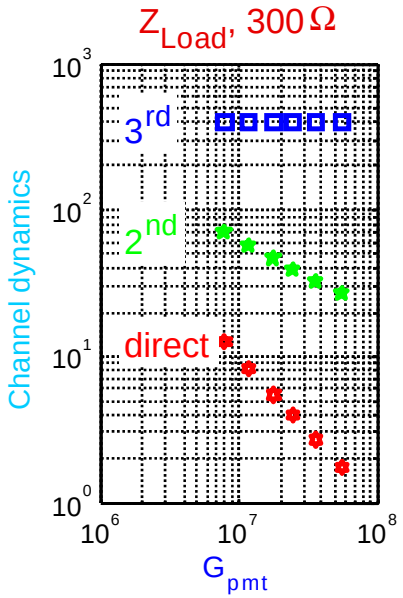
Four 10-cell block are able to limit dead time at reasonable dead time

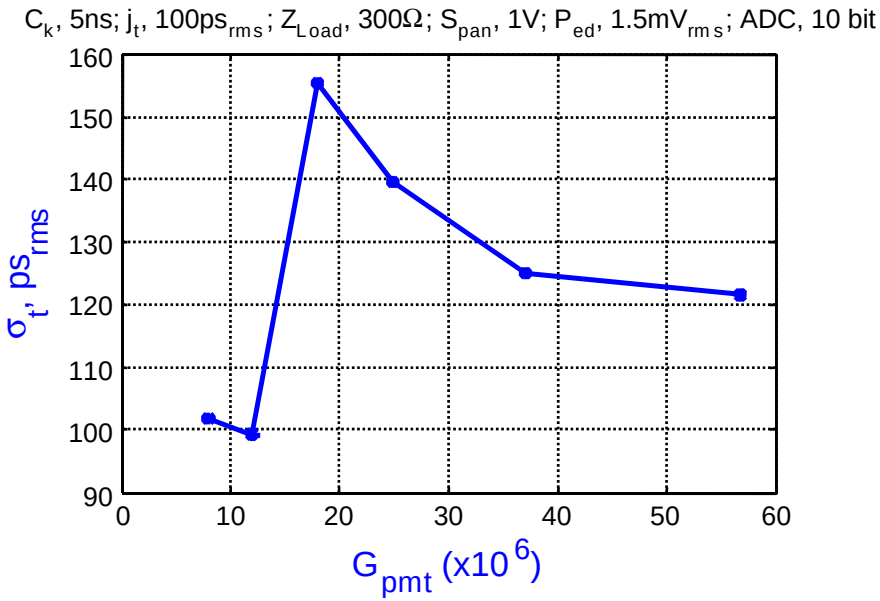
10 p.e.

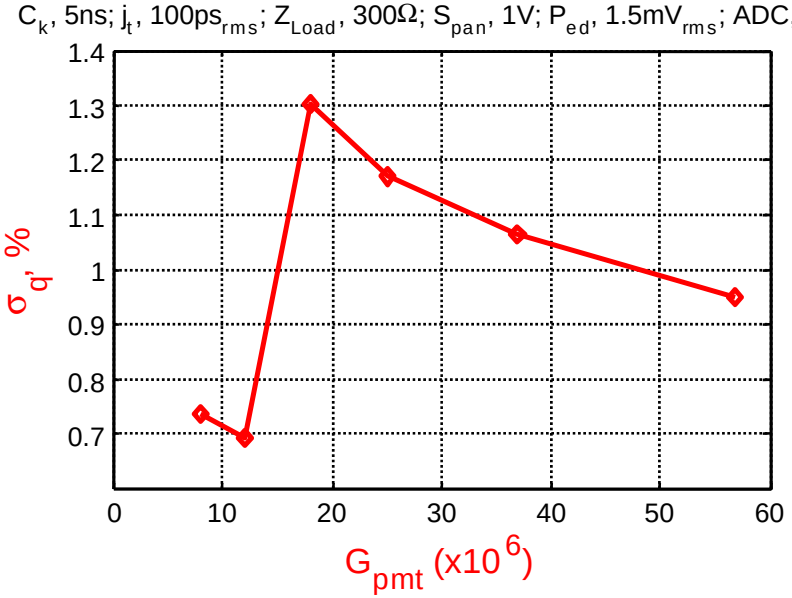

G_Pmt, 8·10^6; Ck, 5ns; j_t 100ps_rms; noise, 344µV_rms; P_ed, 1.5mV_rms; ADC 10bit
OutA
samples, (mV)
9.3 s.p.e. signal
fit, (mV)
trigger time
ns
OutB
2nd Channell (mV) direct
OutC
P_t = 24.05 ns; σ_t = 102 ps_rms
p.e. meas. = 9.32; σ_e = 0.74 %
deviation from mean
trigger-clock delay, ns

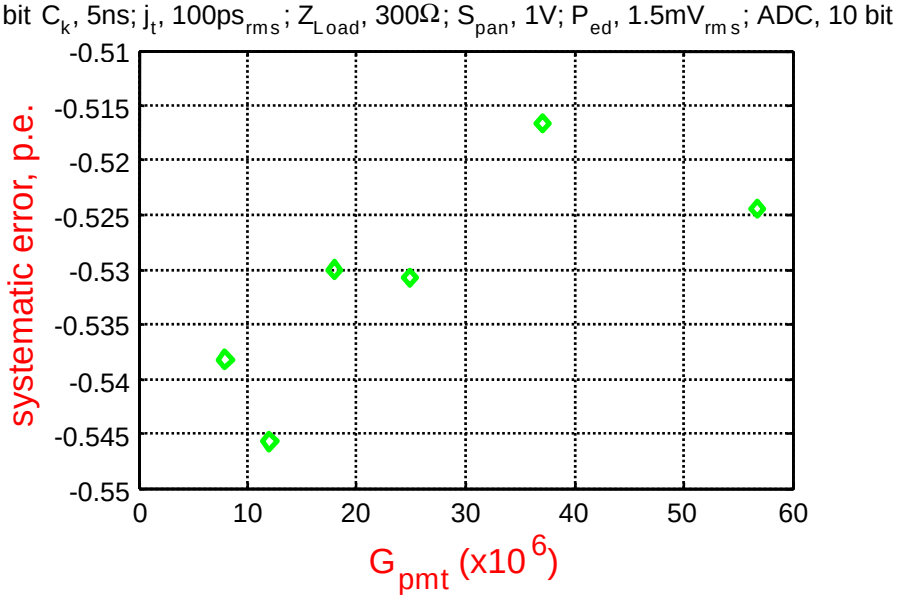
10 p.e.


Z_{Load}, 300 Ω
10 photoelectrons Tipical amplitude (mV)
10^4
10^3
10^2
10^6
10^7
10^8
G_{pmt}


Z_{Load}, 300 Ω
Channel dynamics
10^3
10^2
10^1
10^0
3rd
2nd
direct
10^6
10^7
10^8
G_{pmt}

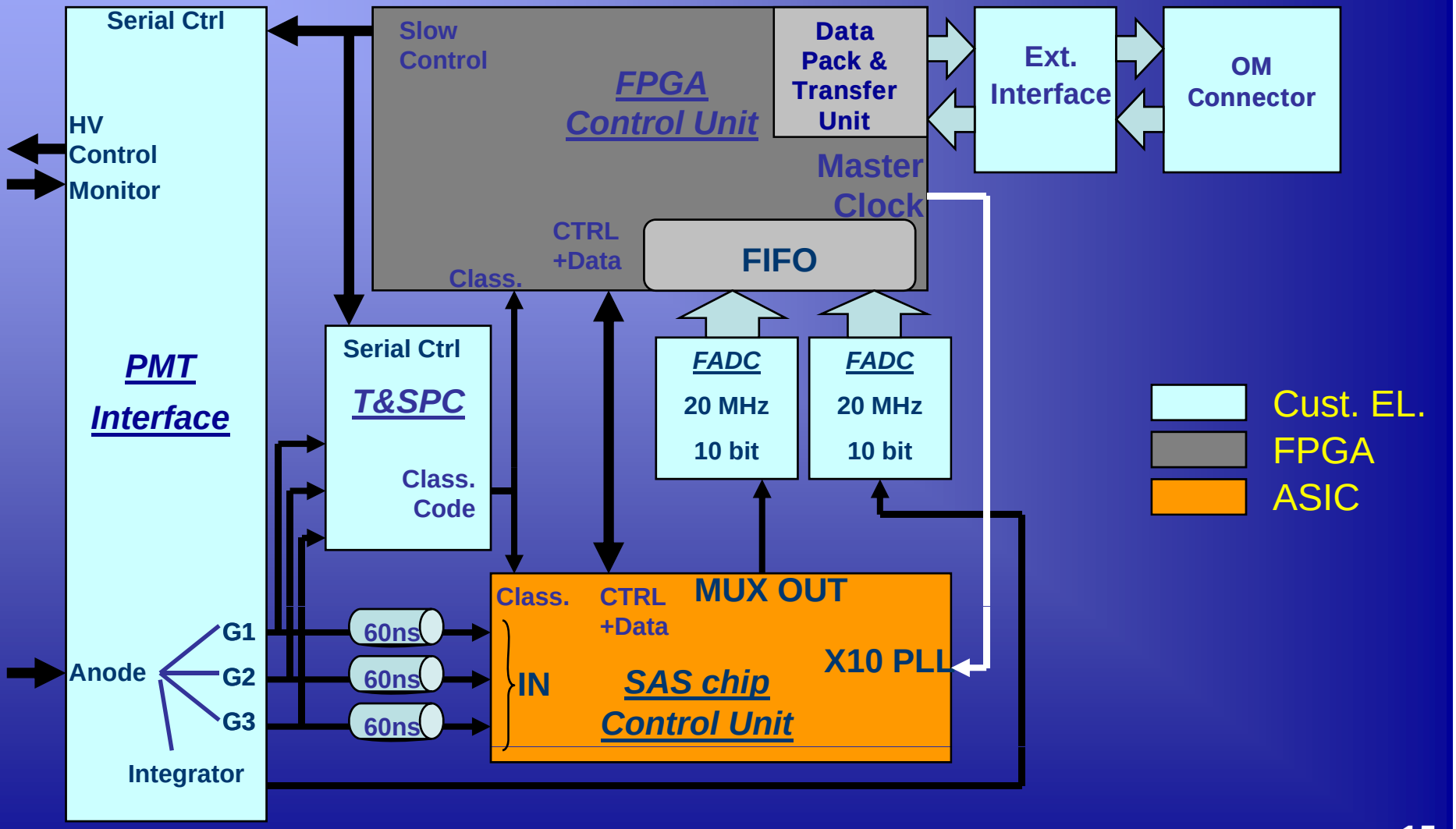

C_k, 5ns; j_t, 100ps$_{rms}$; Z_{Load}, 300Ω; S_{pan}, 1V; P_{ed}, 1.5mV$_{rms}$; ADC, 10 bit
σ_t, ps$_{rms}$
160
150
140
130
120
110
100
90
0
10
20
30
40
50
60
G_{pmt} (x10^6)


C_k, 5ns; j_t, 100ps$_{rms}$; Z_{Load}, 300Ω; S_{pan}, 1V; P_{ed}, 1.5mV$_{rms}$; ADC, 10 bit
σ_q, %
1.4
1.3
1.2
1.1
1
0.9
0.8
0.7
0
10
20
30
40
50
60
G_{pmt} (x10^6)

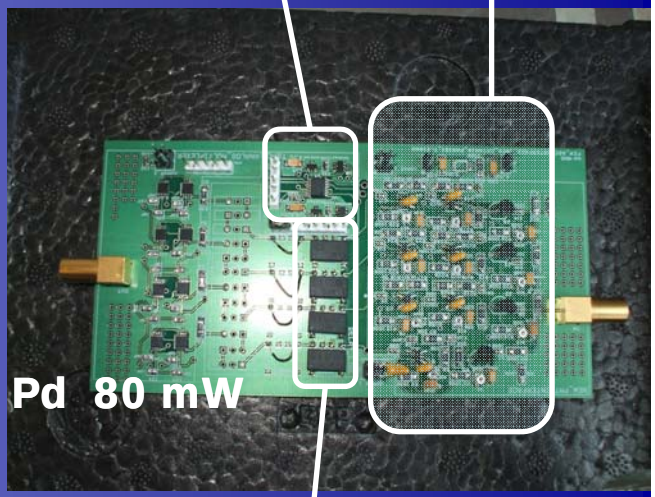

C_k, 5ns; j_t, 100ps$_{rms}$; Z_{Load}, 300Ω; S_{pan}, 1V; P_{ed}, 1.5mV$_{rms}$; ADC, 10 bit
systematic error, p.e.
-0.51
-0.515
-0.52
-0.525
-0.53
-0.535
-0.54
-0.545
-0.55
0
10
20
30
40
50
60
G_{pmt} (x10^6)

General Requirements	*Front End Specifications*
Low Power Dissipation	**< 500 mW in each Optical Module (MO) -> Full-custom VLSI ASIC**
Flexibility	**Acquisition param. by Slow Control**
High Dynamic Range	**Linear Dynamic Range :** > 512 PE / 60 ns **3 ranges: 8 PE / 60 ns; 64 PE / 60 ns; 512 PE/ 60 ns** **Signal reconstruction up to 640ns** **Time and charge 12000 PE / 10 μs**
Minimum Dead Time	**Dead Time < 1 ns** **Background 30 KHz (^{40}K in 10" PMT)**
Optimal Resolution	**Time resolution 200 ÷300 ps** **Charge resolution 2 ÷ 3 %**
Low Cost	

Optical Module Low Power Front-end
Architecture



PMT Interface Block Diagram



3MHz @ -3dB

10MHz @ -60dB

Ra

Rb

Protection

-1

Filter

Integrator

x1

Protection

-1

x4

Filter

Delay

OUT A

R1

/8

Protection

-1

x4

Filter

Delay

OUT B

R_{tot} =

300Ω

R2

/64

R3

Protection

-1

x4

Filter

Delay

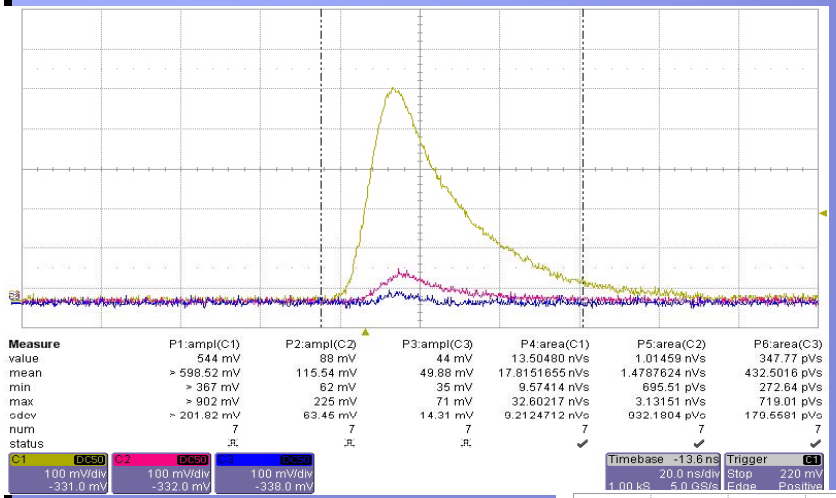
OUT B

30MHz@ -3dB

100MHz@ -60dB

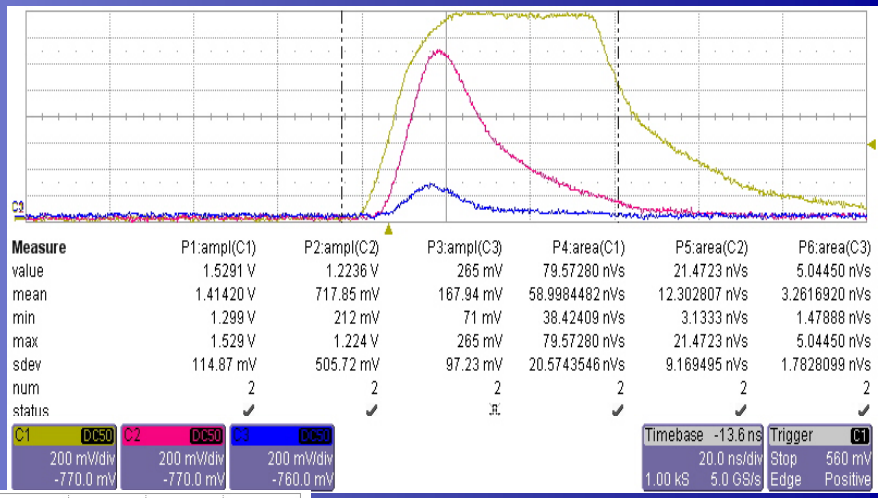
IC Delay Line 30 ns

PMT interface - measurements



Measure	P1:ampl(C1)	P2:ampl(C2)	P3:ampl(C3)	P4:area(C1)	P5:area(C2)	P6:area(C3)
value	544 mV	88 mV	44 mV	13.50480 nVs	1.01459 nVs	347.77 pVs
mean	> 598.52 mV	115.54 mV	49.88 mV	17.8151655 nVs	1.4787624 nVs	432.5016 pVs
min	> 367 mV	62 mV	35 mV	9.57414 nVs	695.51 pVs	272.64 pVs
max	> 902 mV	225 mV	71 mV	32.60217 nVs	3.13151 nVs	719.01 pVs
sdev	> 201.82 mV	63.45 mV	14.31 mV	9.2124712 nVs	932.1804 pVs	179.5581 pVs
num	7	7	7	7	7	7
status				✓	✓	✓

C1 DC50 100 mV/div -331.0 mV | C2 DC50 100 mV/div -332.0 mV | C3 DC50 100 mV/div -338.0 mV | Timebase -13.6 ns 20.0 ns/div 1.00 kS 5.0 GS/s | Trigger C1 Stop 220 mV Edge Positive

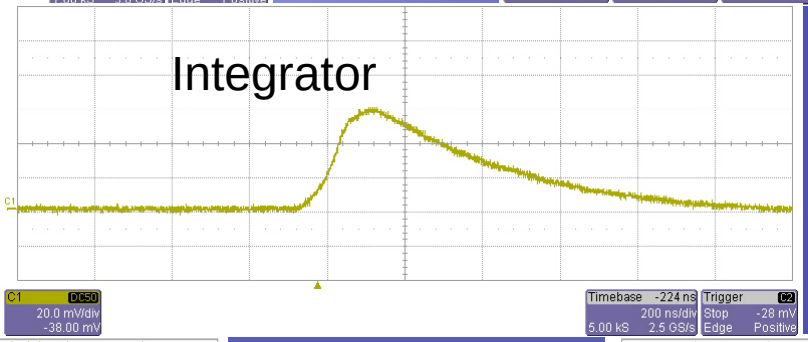


Measure	P1:ampl(C1)	P2:ampl(C2)	P3:ampl(C3)	P4:area(C1)	P5:area(C2)	P6:area(C3)
value	1.5291 V	1.2236 V	265 mV	79.57280 nVs	21.4723 nVs	5.04450 nVs
mean	1.41420 V	717.85 mV	167.94 mV	58.9984482 nVs	12.302807 nVs	3.2616920 nVs
min	1.299 V	212 mV	71 mV	38.42409 nVs	3.1333 nVs	1.47888 nVs
max	1.529 V	1.224 V	265 mV	79.57280 nVs	21.4723 nVs	5.04450 nVs
sdev	114.87 mV	505.72 mV	97.23 mV	20.5743546 nVs	9.169495 nVs	1.7828099 nVs
num	2	2	2	2	2	2
status	✓	✓		✓	✓	✓

C1 DC50 200 mV/div -770.0 mV | C2 DC50 200 mV/div -770.0 mV | C3 DC50 200 mV/div -760.0 mV | Timebase -13.6 ns 20.0 ns/div 1.00 kS 5.0 GS/s | Trigger C1 Stop 560 mV Edge Positive

< 8 pe

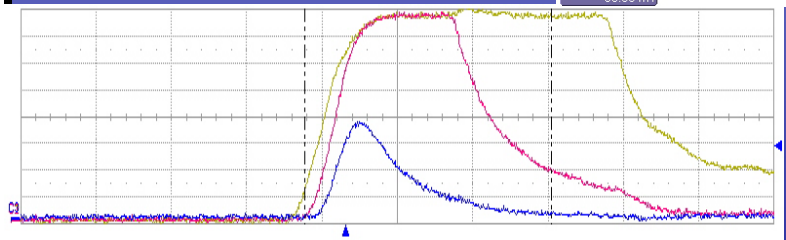
64 pe ÷ 512 pe



C1 DC50 20.0 mV/div -38.00 mV | Timebase -224 ns 200 ns/div 5.00 kS 2.5 GS/s | Trigger C2 Stop -28 mV Edge Positive

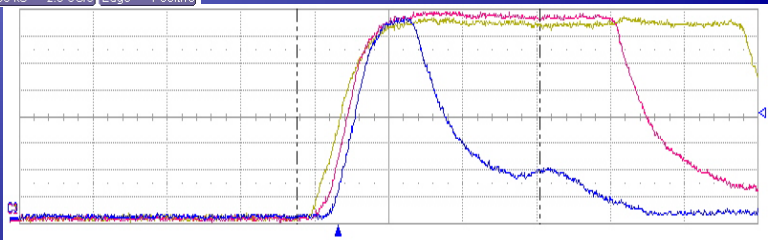
8 pe ÷ 64 pe

> 512 pe



Measure	P1:ampl(C1)	P2:ampl(C2)	P3:ampl(C3)	P4:area(C1)	P5:area(C2)	P6:area(C3)
value	1.538 V	1.1101 V	734 mV	91.20836 nVs	39.7636 nVs	15.94643 nVs
mean	1.40504 V	1.241647 V	804.34 mV	91.3733500 nVs	40.078230 nVs	18.4755356 nVs
min	1.245 V	1.0769 V	672 mV	89.71281 nVs	38.5120 nVs	15.72015 nVs
max	1.538 V	1.5380 V	1.008 V	93.19888 nVs	41.9592 nVs	23.76003 nVs
sdev	121.00 mV	209.971 mV	145.95 mV	1.4279569 nVs	1.424786 nVs	3.7378443 nVs
num	3	3	3	3	3	3
status		✓		✓	✓	✓

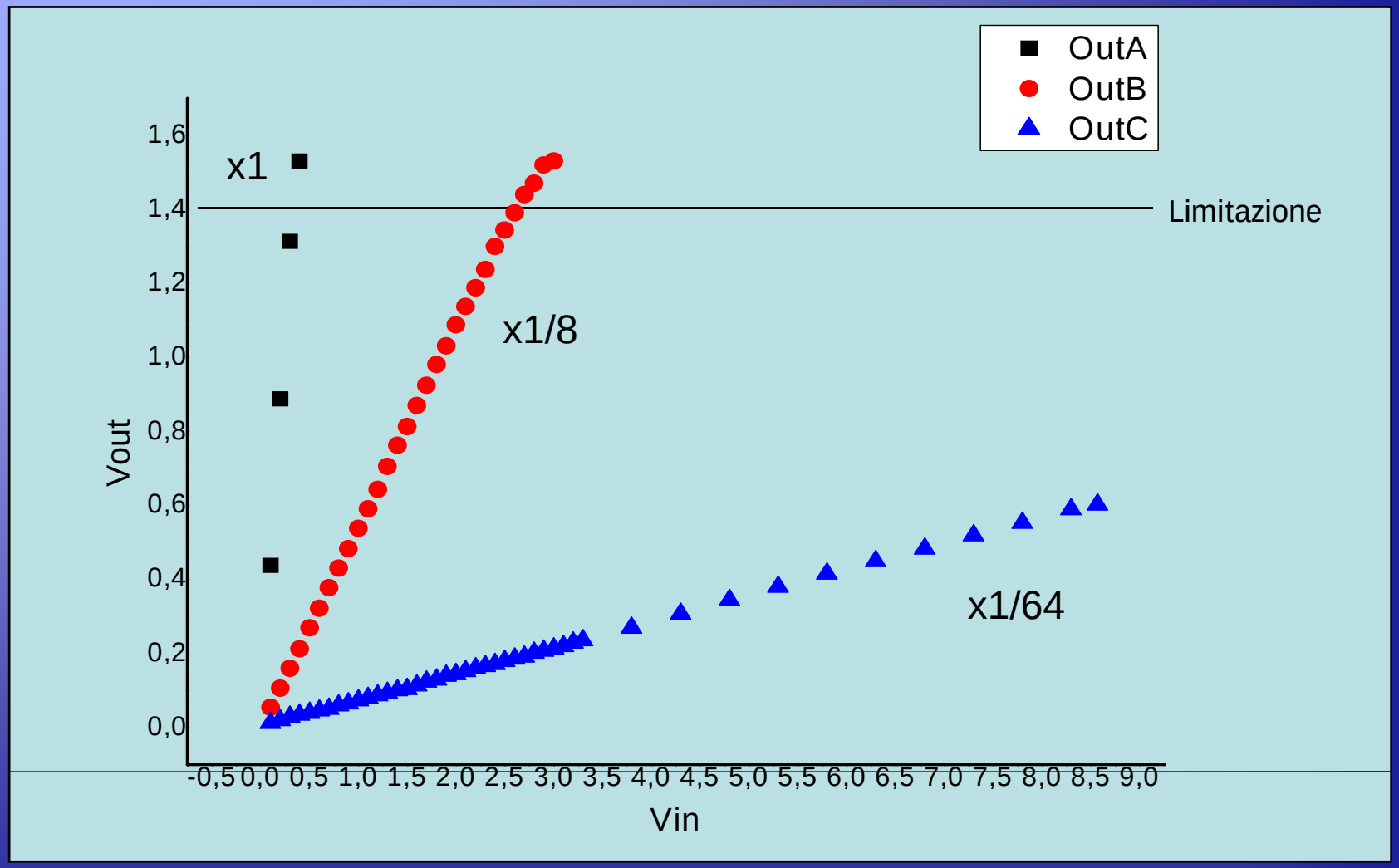
C1 DC50 200 mV/div -770.0 mV | C2 DC50 200 mV/div -770.0 mV | C3 DC50 200 mV/div -760.0 mV | Timebase -13.6 ns 20.0 ns/div 1.00 kS 5.0 GS/s | Trigger C3 Stop 534 mV Edge Positive



Measure	P1:ampl(C1)	P2:ampl(C2)	P3:ampl(C3)	P4:area(C1)	P5:area(C2)	P6:area(C3)
value	1.4434 V	1.4975 V	1.503 V	79.00358 nVs	31.5752 nVs	44.11429 nVs
mean	1.459862 V	1.47395 V	697.54 mV	85.4078348 nVs	33.509545 nVs	17.4822392 nVs
min	958.8 mV	925 mV	230 mV	76.90522 nVs	26.3001 nVs	5.01445 nVs
max	1.8208 V	1.591 V	1.520 V	92.56071 nVs	35.0860 nVs	58.48284 nVs
sdev	81.254 mV	152.09 mV	371.73 mV	2.4885022 nVs	1.177605 nVs	12.9029243 nVs
num	665	665	665	665	665	665
status	✓	✓		✓	✓	✓

C1 DC50 200 mV/div -770.0 mV | C2 DC50 200 mV/div -770.0 mV | C3 DC50 200 mV/div -760.0 mV | Timebase -13.6 ns 20.0 ns/div 1.00 kS 5.0 GS/s | Trigger Single Logic

PMT interface - linearity



Test with 100mV ÷ 8,56 V equivalent to anode current pulse 333uA ÷ 28mA -> @ range 3pe ÷ 280 pe ($5*10^6$, 300Ω)

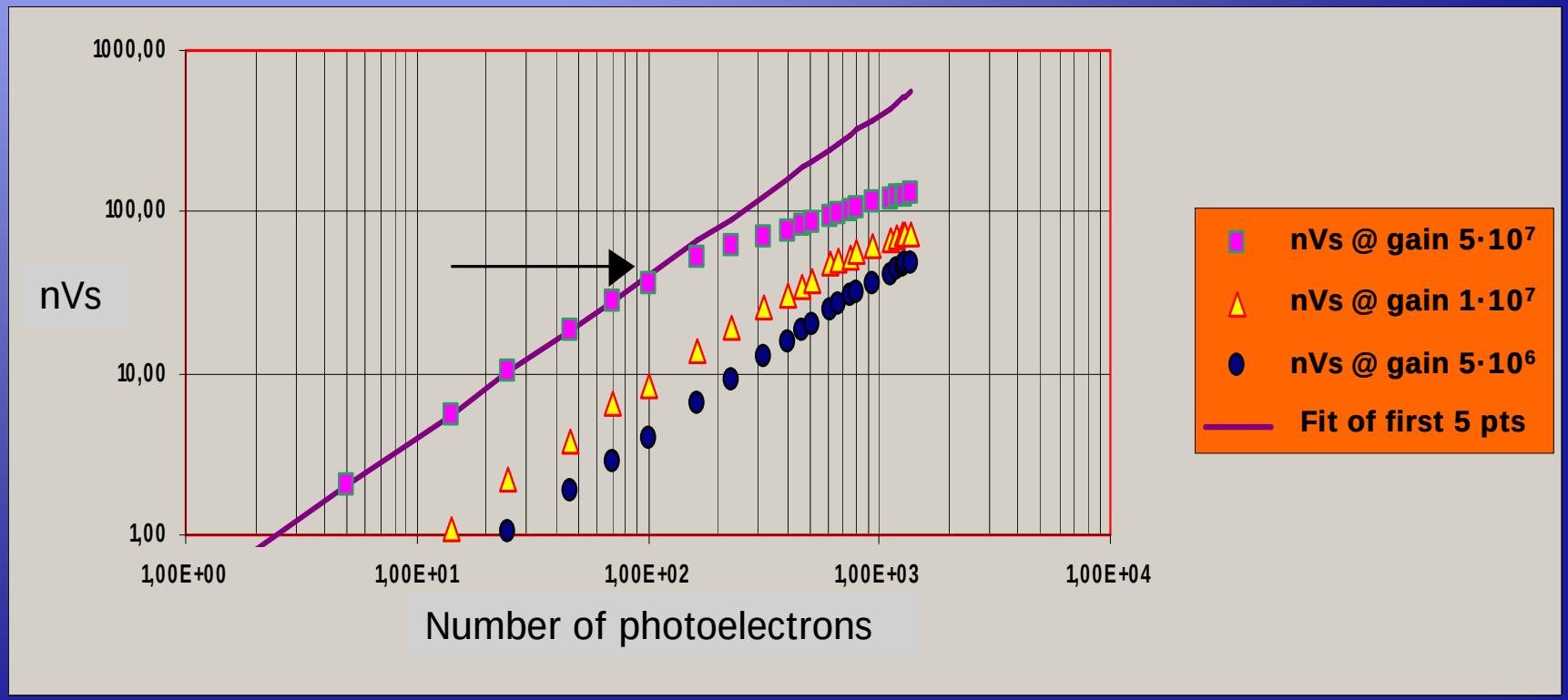
PMT saturation @ 1nC = about 1250 pe ($5*10^6$, 300Ω)

PMT dynamic range VS Gain

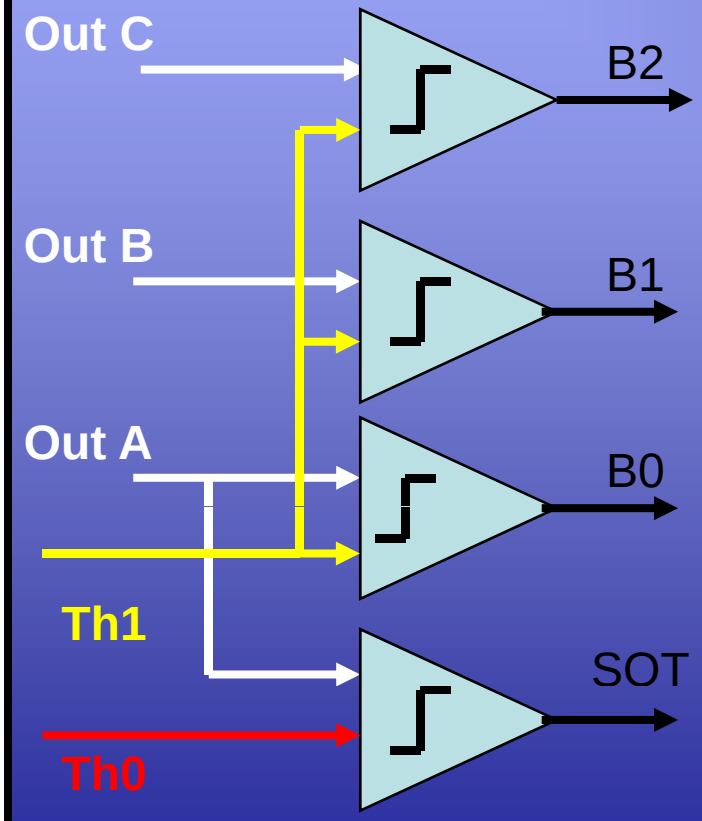
The effect of saturation seems to be determined by the anodic pulsed current and independent from the gain.

Limit Value of about 1 nC

120-150 p.e. @ gain $5 \cdot 10^7$



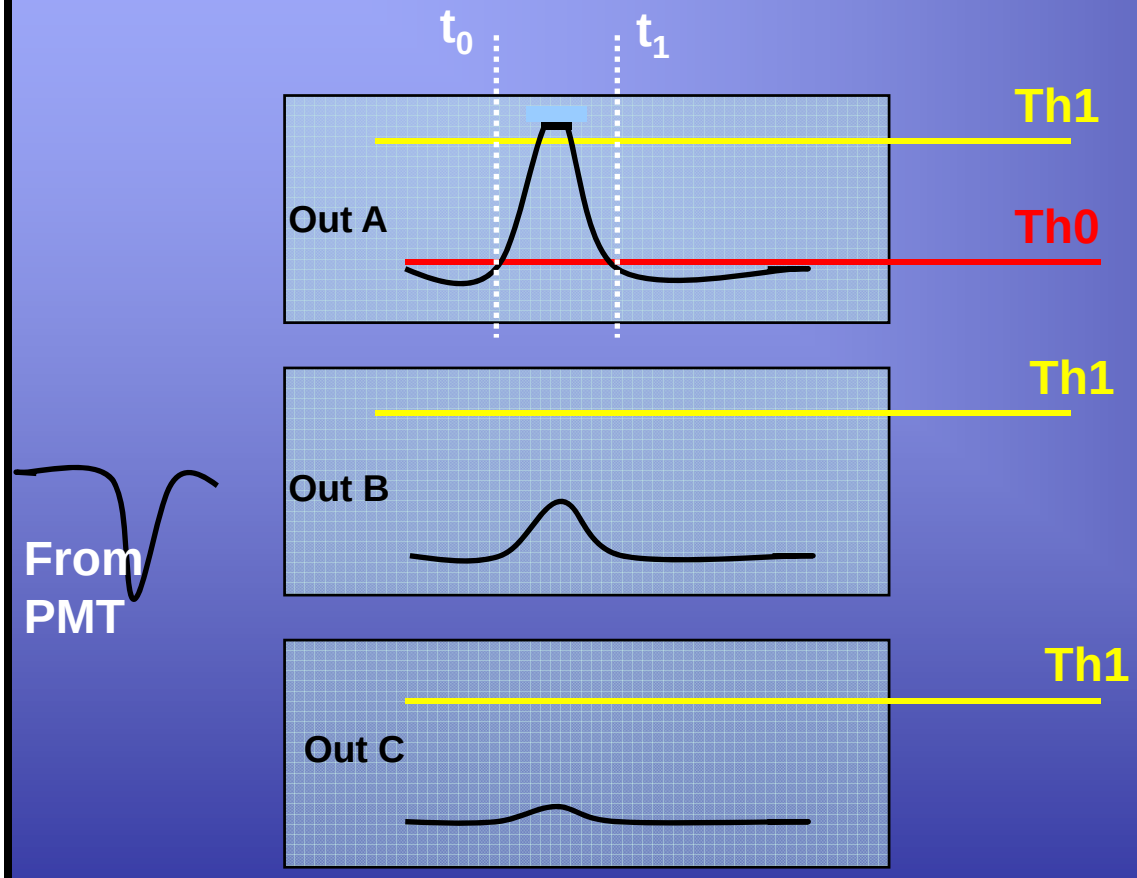
Trigger & Single Photon Classifier
block diagram



Fast comparator
with hysteresis

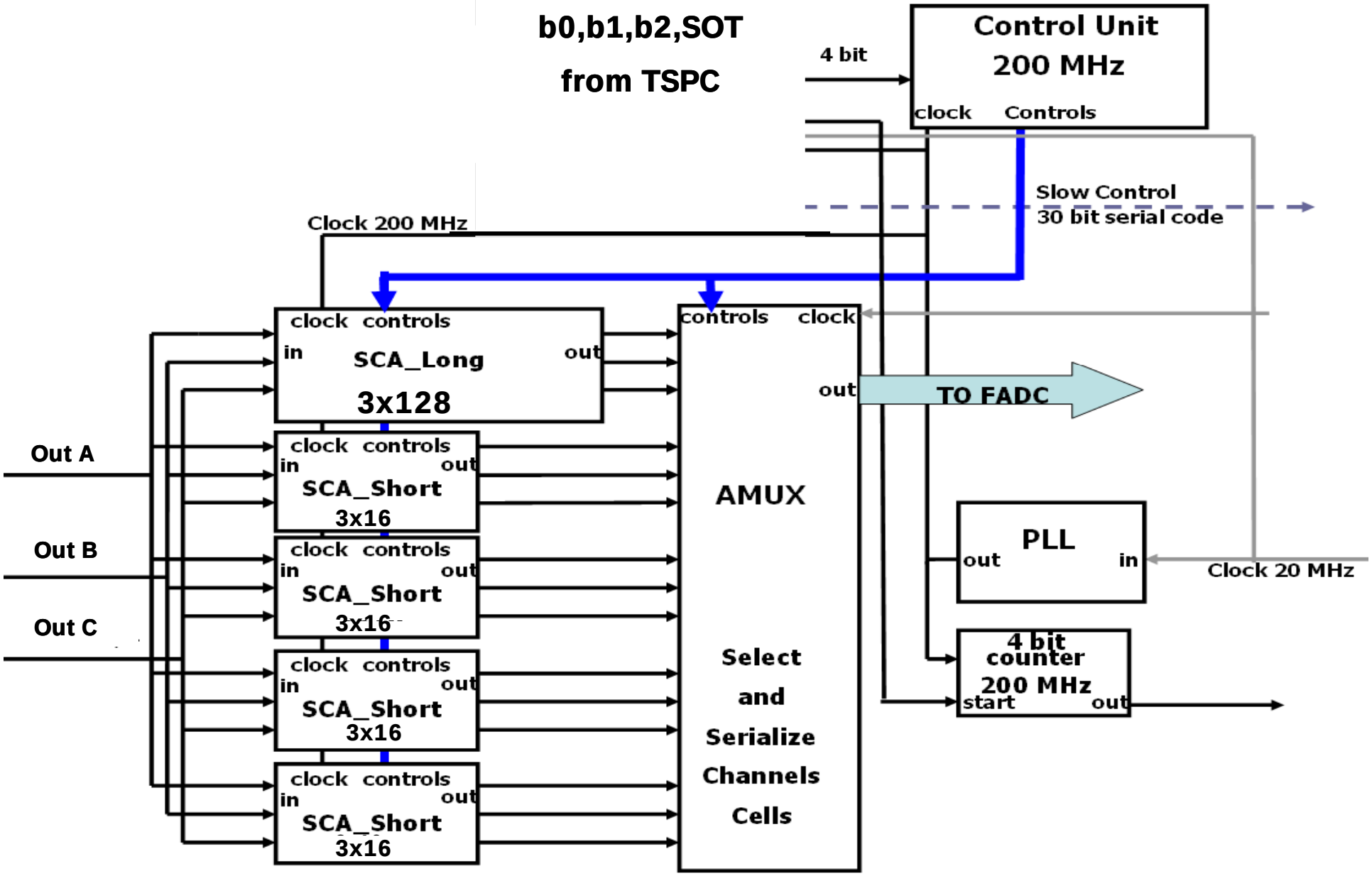
- B0, B1, B2 = PMT signal classification code
- SOT, Signal Over Threshold, twofold use:
  - Rising edge Trigger;
  - SOT width determines sampling mode (Short, Long, Integ.)
- Th0 e Th1 generated by 2 6-bit ***DAC*** serial code (Slow Control).
  - Th0 trigger threshold;
  - Th1 Out of range threshold.
- Asynchronous and always active.

An example…



- @ t_0 event trigger;
- $\Delta t = t_1 - t_0$ compared to Short length (60 ns);
- If bigger after a Short also a Long sampling of the signal.
- The classification code is:
  - B0=1; B1=0; B2=0.
- OutB samples will be converted!!

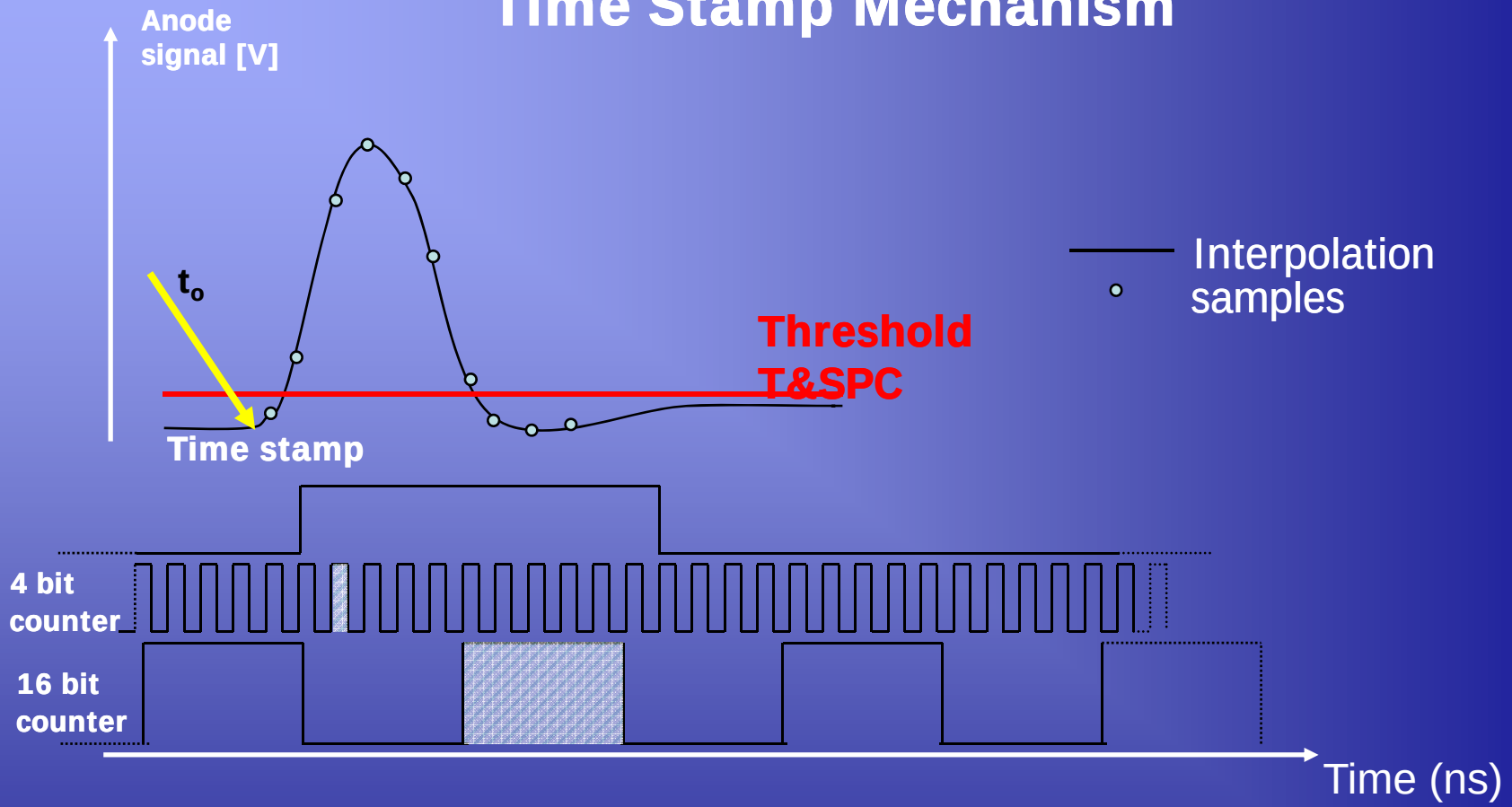
CHIP SAS - block diagram (Smart Autotriggering Sampler)



Sampling

- 3 sampling modes:
  - SAS_SHORT
    - 4 independent memory banks: sampling @ START (T&SPC)
      - 3 channels 16 cells
      - 200 MHz sampling 20 MHz transfer
      - Serial transfer towards ADC
  - SAS_LONG
    - T&SPC enabled: signal over Threshold more than 60 ns
      - 3 channels 128 cells
      - 200 MHz sampling 20 MHz transfer
      - Serial transfer towards ADC
  - FADC (external 10b 20 MHz ADC)
    - T&SPC enabled: signal over Threshold more than 640ns
      - Integrated signal
      - 10 bit 20 MHz Flash ADC
      - 1 Ksample record length

Time Stamp Mechanism

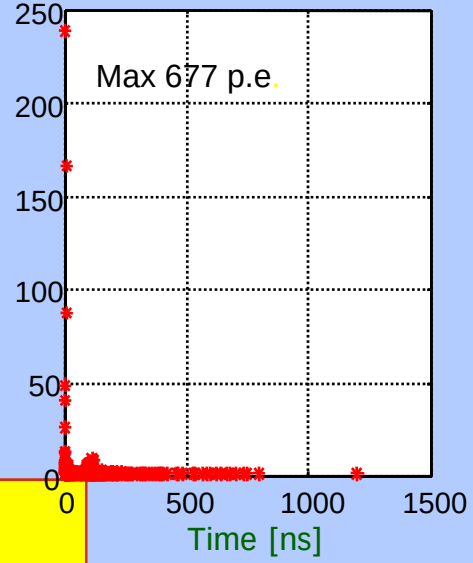


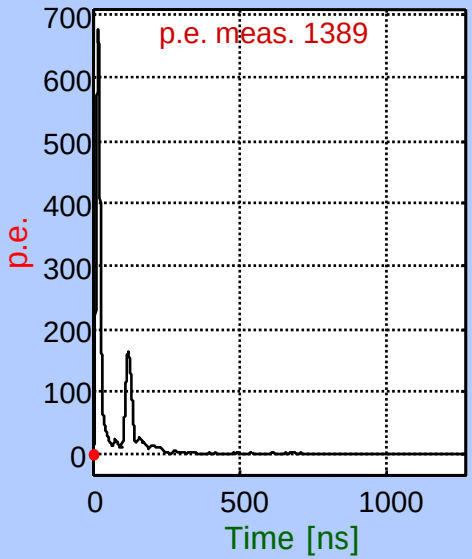
Time Stamp = 20 bit sent to data acquisition

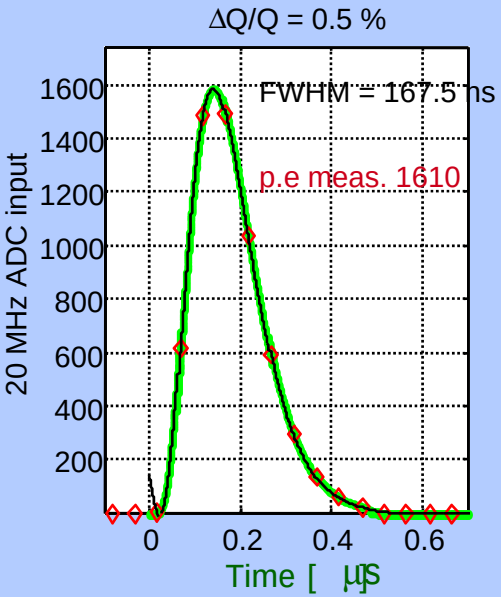
- One time stamp for sampler
- Dedicated FIFO

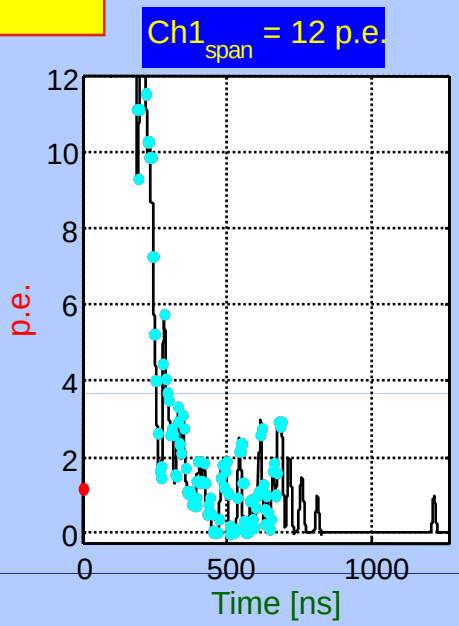
t_0 reconstructed offline

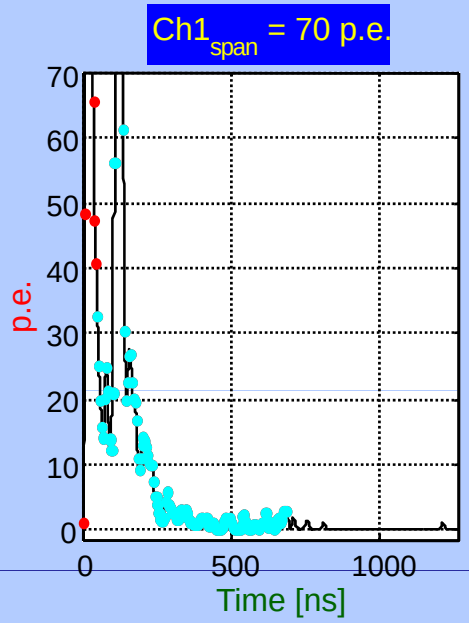
$G_{pmt}=8\cdot10^6$
$Z_L=300\Omega$

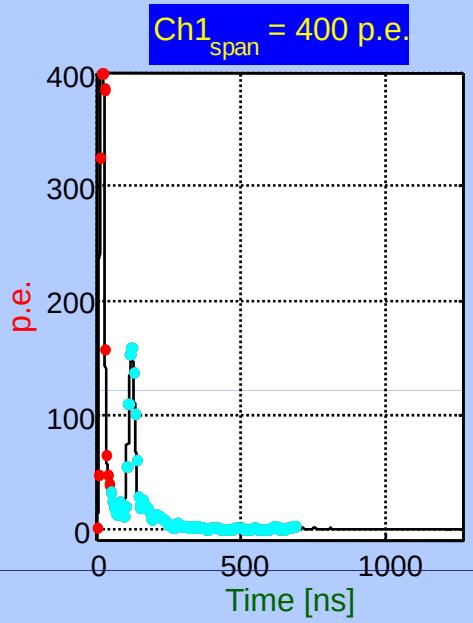


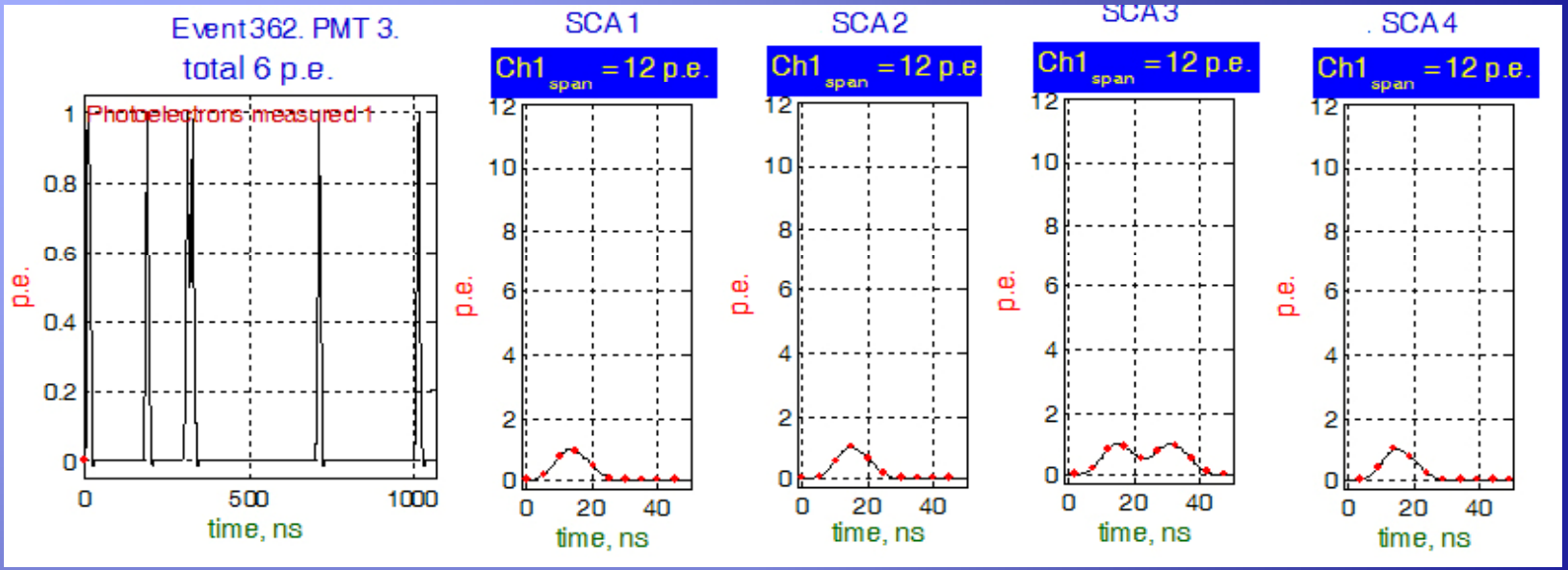












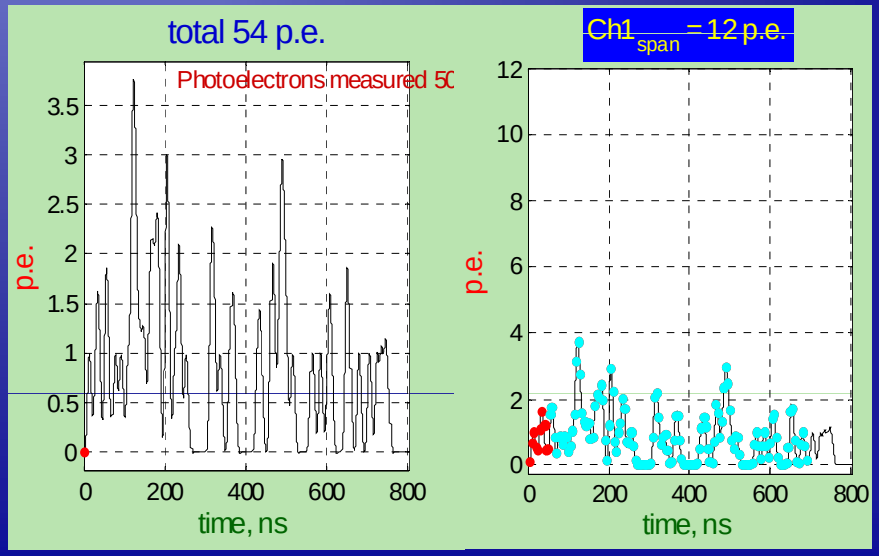
Very rare event -> 5 successive pulses @ more than 50 ns

4 events fully sampled– 1 lost

$G_{pmt}=8\cdot10^6$;
$Z_L=300\Omega$

Structured signal ->

well reconstructed with 128 cells

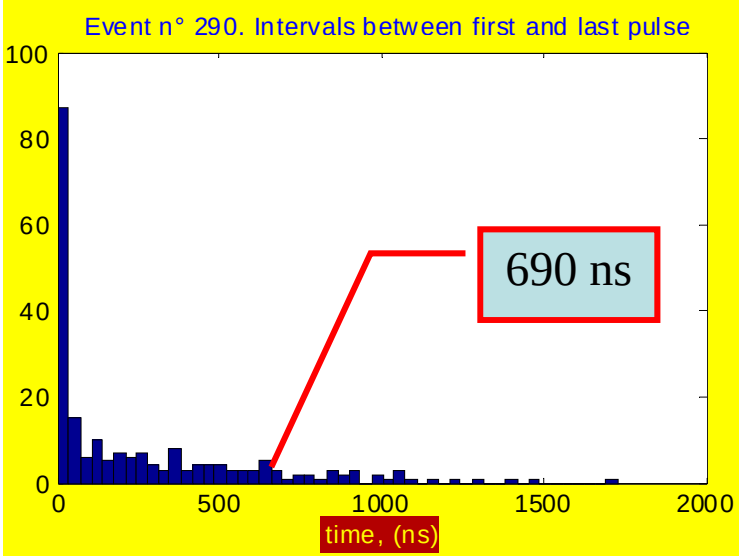


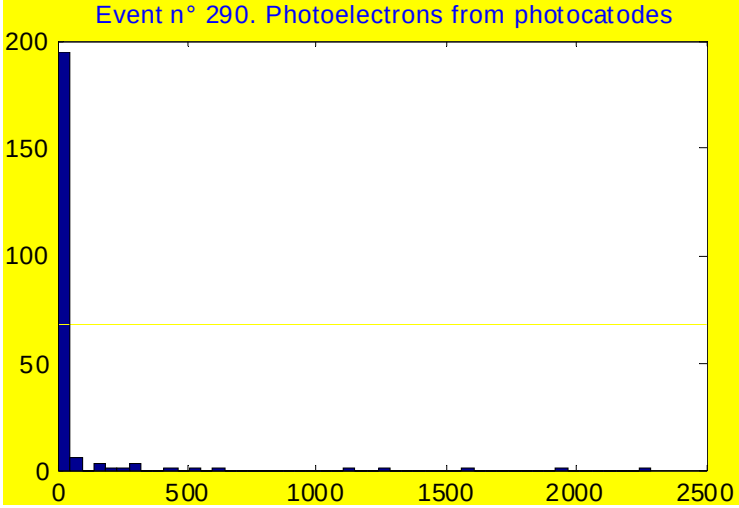
domenico.lopresti@ct.infn.it

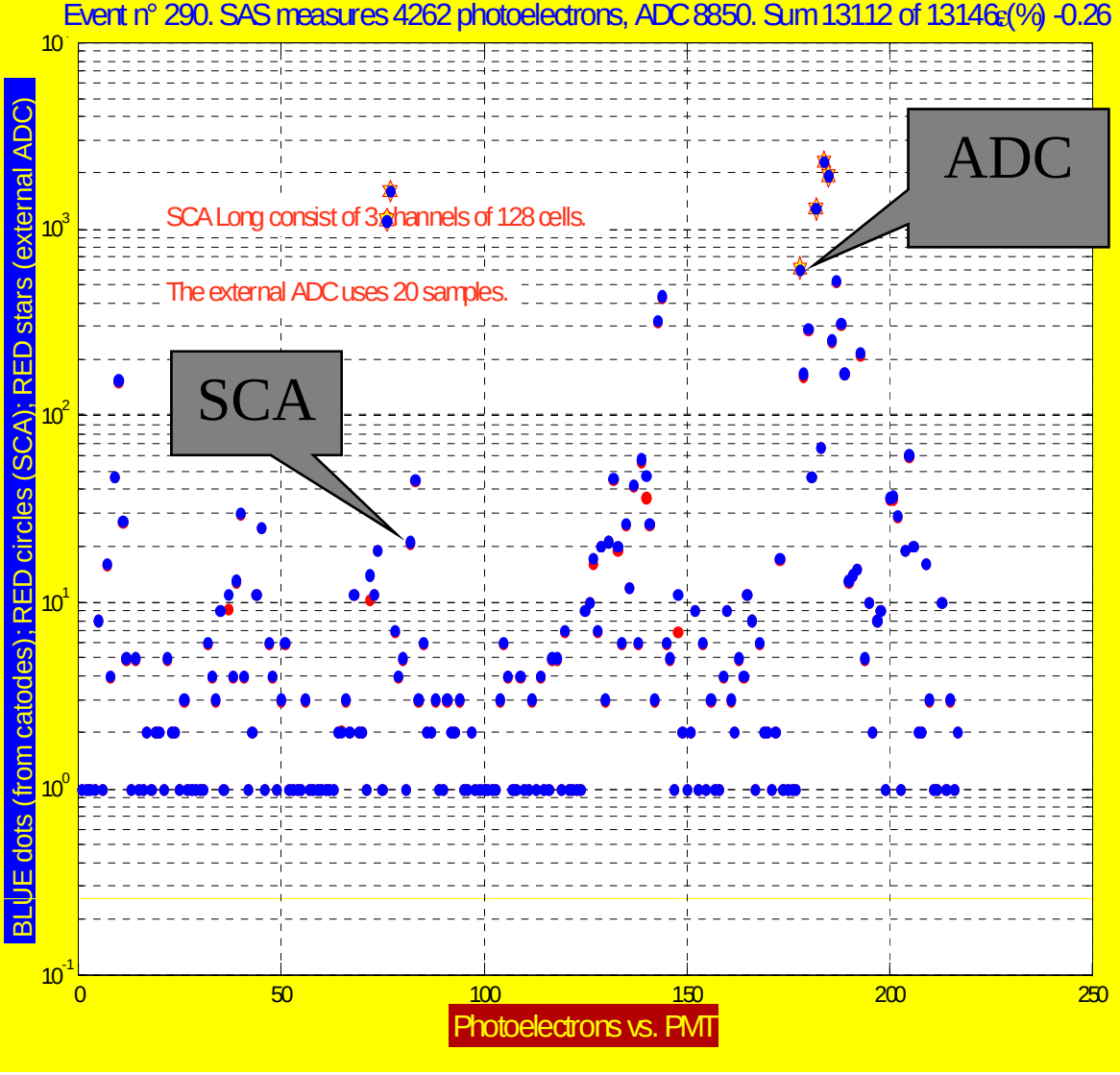
In this event we have 13097 p.e.

We are able to measure its charge using a 128 SCA (640ns) with an error < 0.26 %

$G_{pmt}=8\cdot10^6$; $Z_L=300\Omega$







Conclusions

- The front end electronics architecture has been defined and under design;
- PMT interface and TSPC ready;
- Master Control Unit (FPGA) ready;
  - See F. Giorgi talk
- ASIC ready soon (beginning of 2008);
- Test in NEMO phase 2

Thank You