Architecture of a general purpose embedded Slow-Control-Adapter ASIC for future high-energy physics experiments

Alessandro Gabrielli

on behalf of the DACEL Collaboration

(BO-BA-FI-PG-PD-TO-CERN_Mic)

Physics Department of Bologna University & INFN Bologna, Viale Berti Pichat 6/2 40127 Bologna Italy Tel. +39-051-2095052 FAX +39-051-2095297

E-mail: alessandro.gabrielli@bo.infn.it

Meeting at Common Atlas CMS Workshop 19-21 March 2007 - CERN

The GBT

A single link for Timing, Trigger, Slow Control and DAQ in experiments

A. Marchioro
CERN/PH-MIC

Aim: electronics upgrade

LHC → SLHC → beyond

Project Participants

- CERN: PH-MIC & ED & ATE
- INFN: Bari, Bologna, Torino
- IN2P3: Marseille

.. then PD-FI-PG

Presented by A.Marchioro

Meeting at Common Atlas CMS Workshop 19-21 March 2007 - CERN

Outline

- General Aim of the Project
  - Architecture
  - Proposed TTC functionality
- Some details on proposed Error Correction
- Proposal for interface to Slow Control
- Progress & Plans

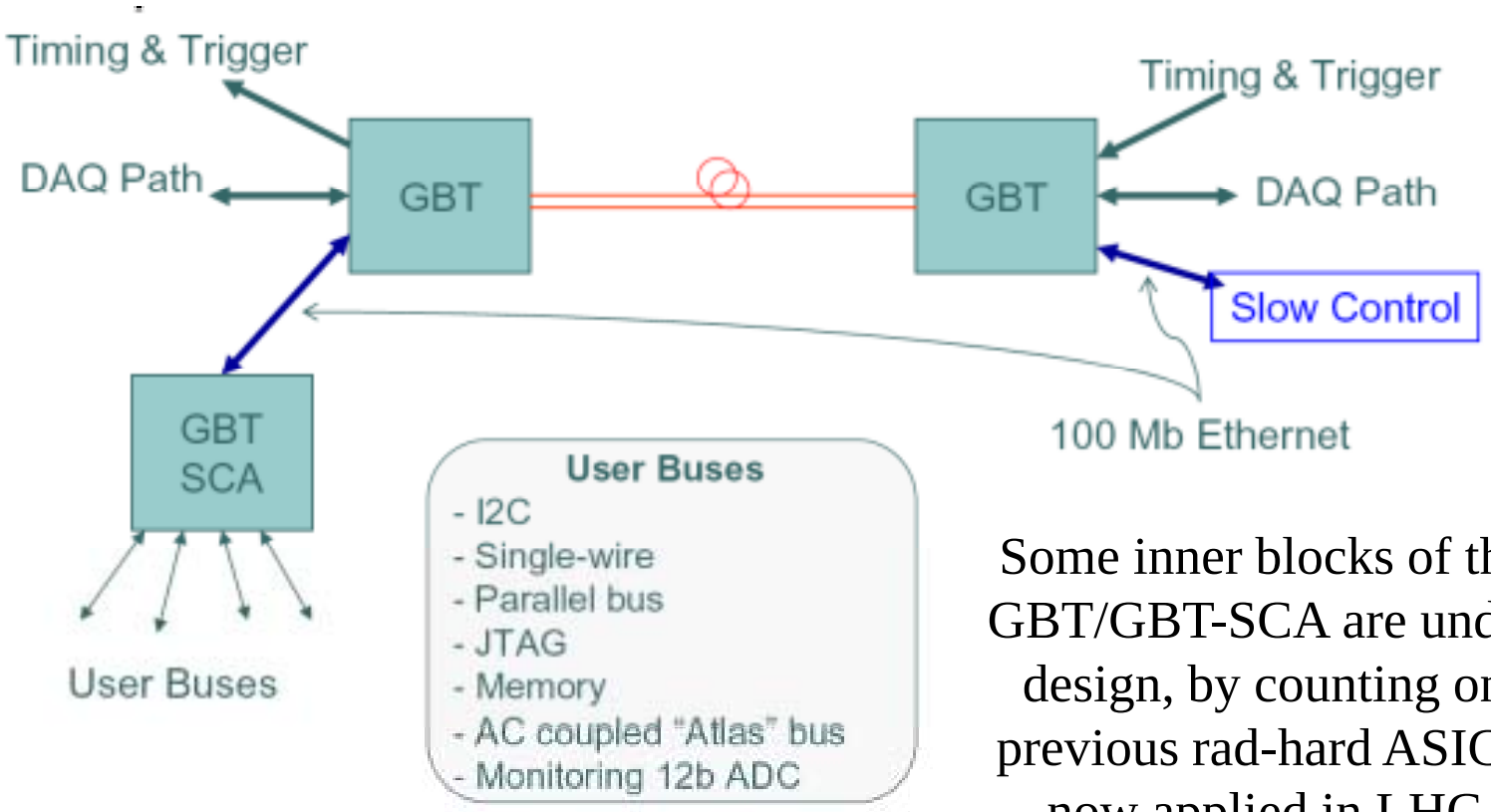
Bologna-Bari

are in charge for the **Slow-Control** architecture

to be designed in 130nm CMOS technology

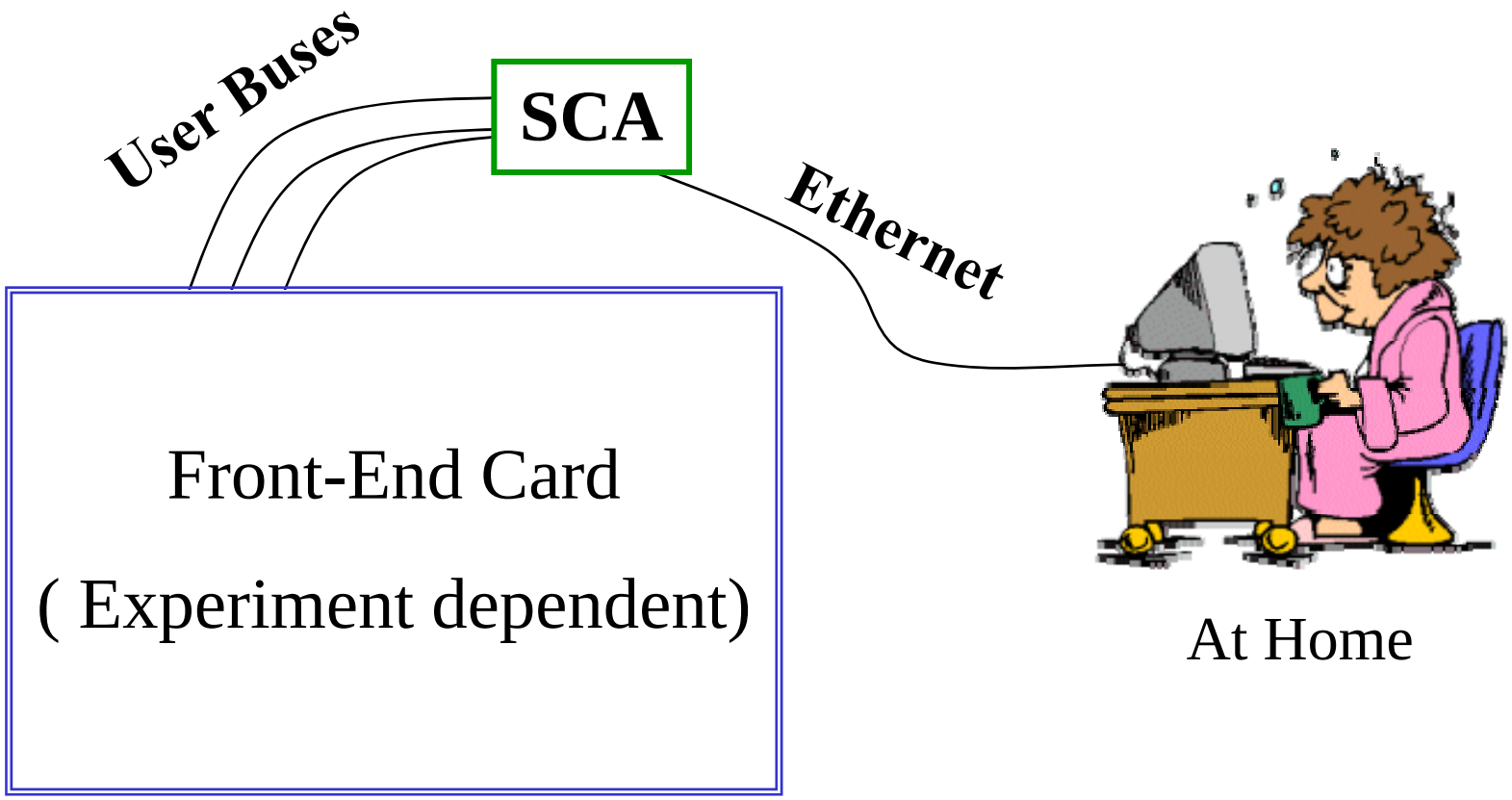
Presented by A.Marchioro

The proposed architecture for a common 800Mb/s optical link + Slow-Control

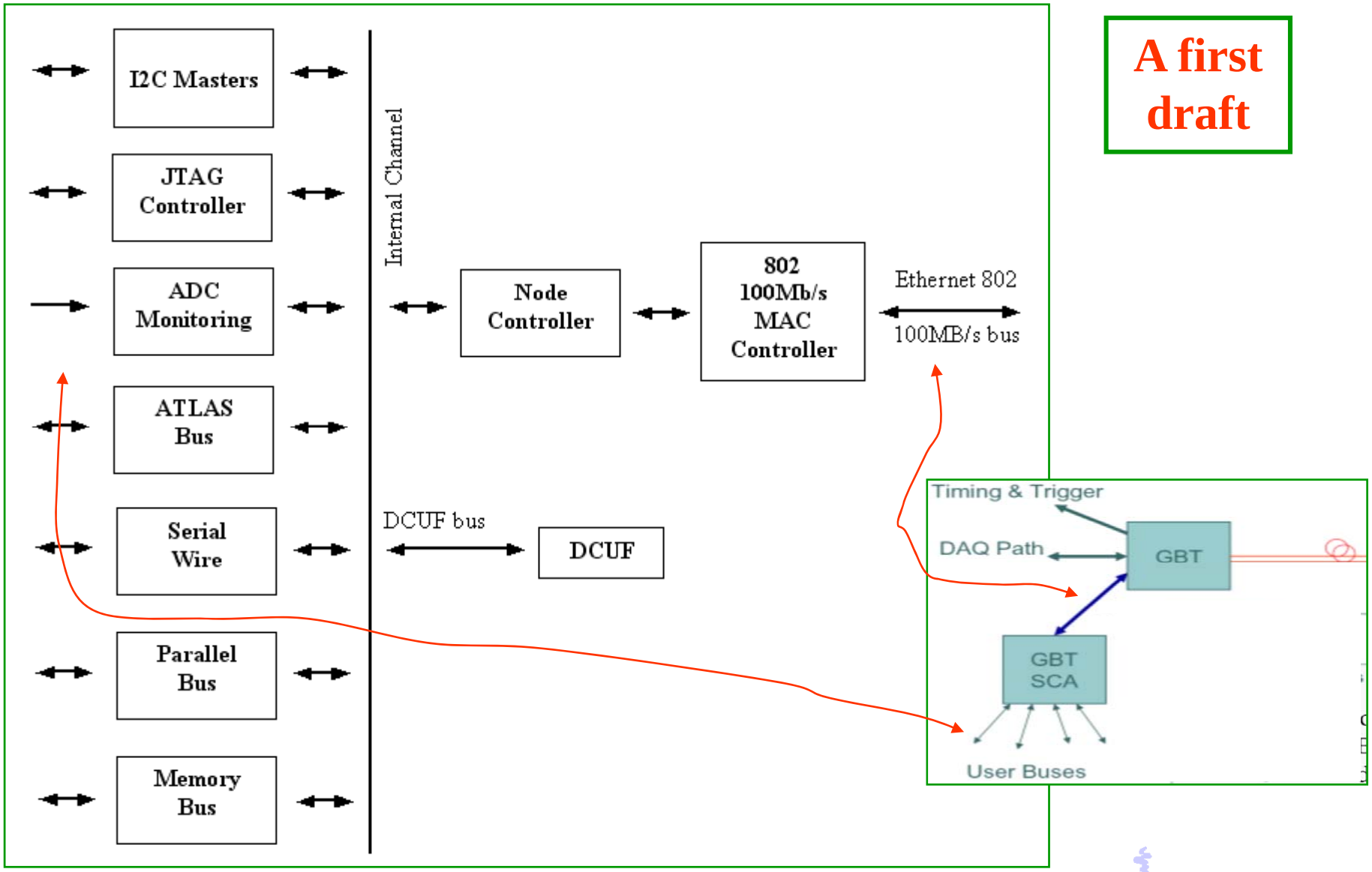


Some inner blocks of the GBT/GBT-SCA are under design, by counting on previous rad-hard ASICS now applied in LHC

Fast Ethernet IEEE-802 100MB/s protocol



The Slow-Control



Fast Ethernet IEEE-802 100MB/s protocol

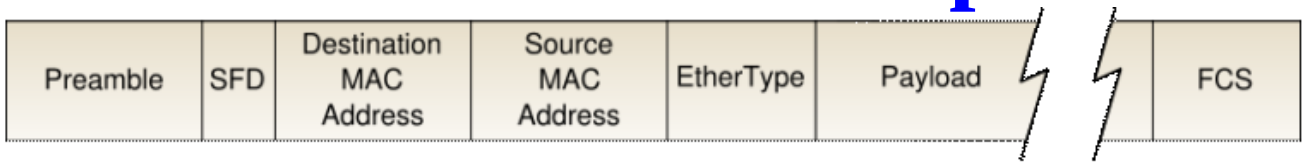


Fig. 4a: Standard IEEE 802.3 Ethernet MAC data frame

GBT-SCA is aimed at interfacing with commercial components that support the IEEE-802 100MB/s protocol, except for physical-layer and clock rate

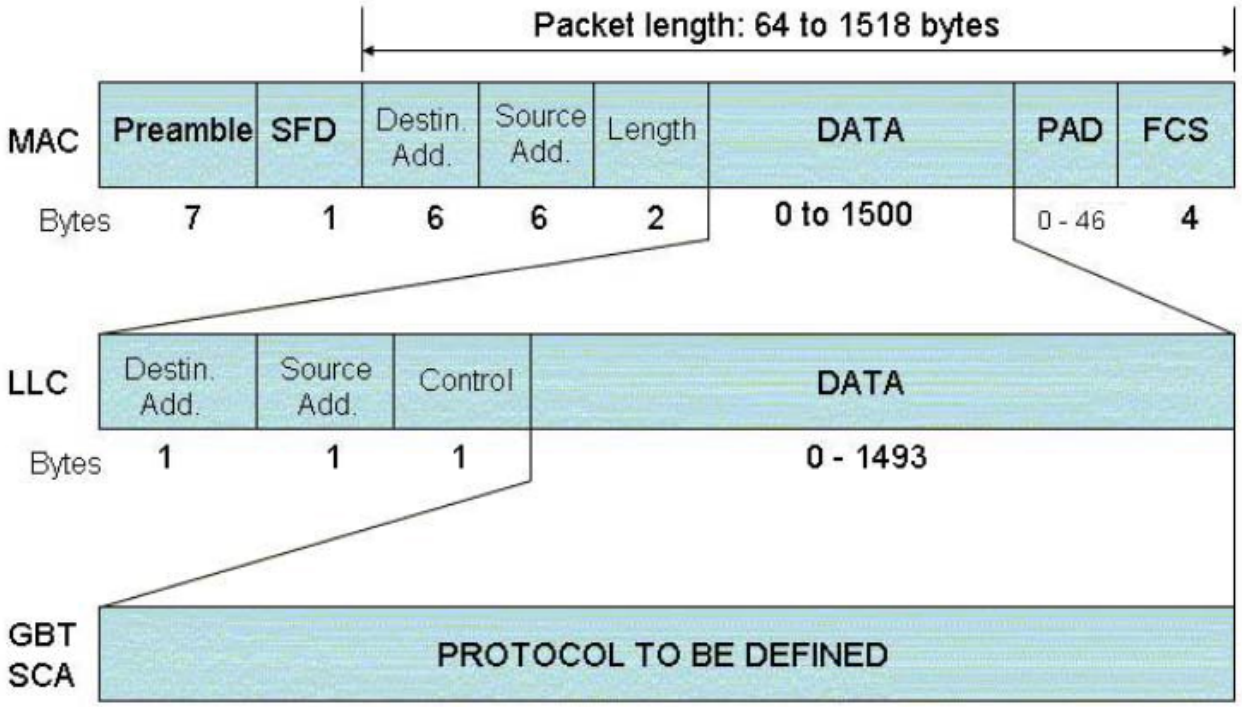


Fig. 4b: LLC frame

The ASIC design

The chip is mainly digital and:

- it will be designed via commercial 130nm technology,
- some internal blocks will be derived from previous ASICS,
- it will not exploit enclosed-gate-layouts for TID effects,
- it will be provided with redundant logic to face SEE problems:
  - triple-redundancy in space,
  - triple-redundancy in time,
  - Hamming-like code correction,

To be investigated via prototypes

The ASIC design

….

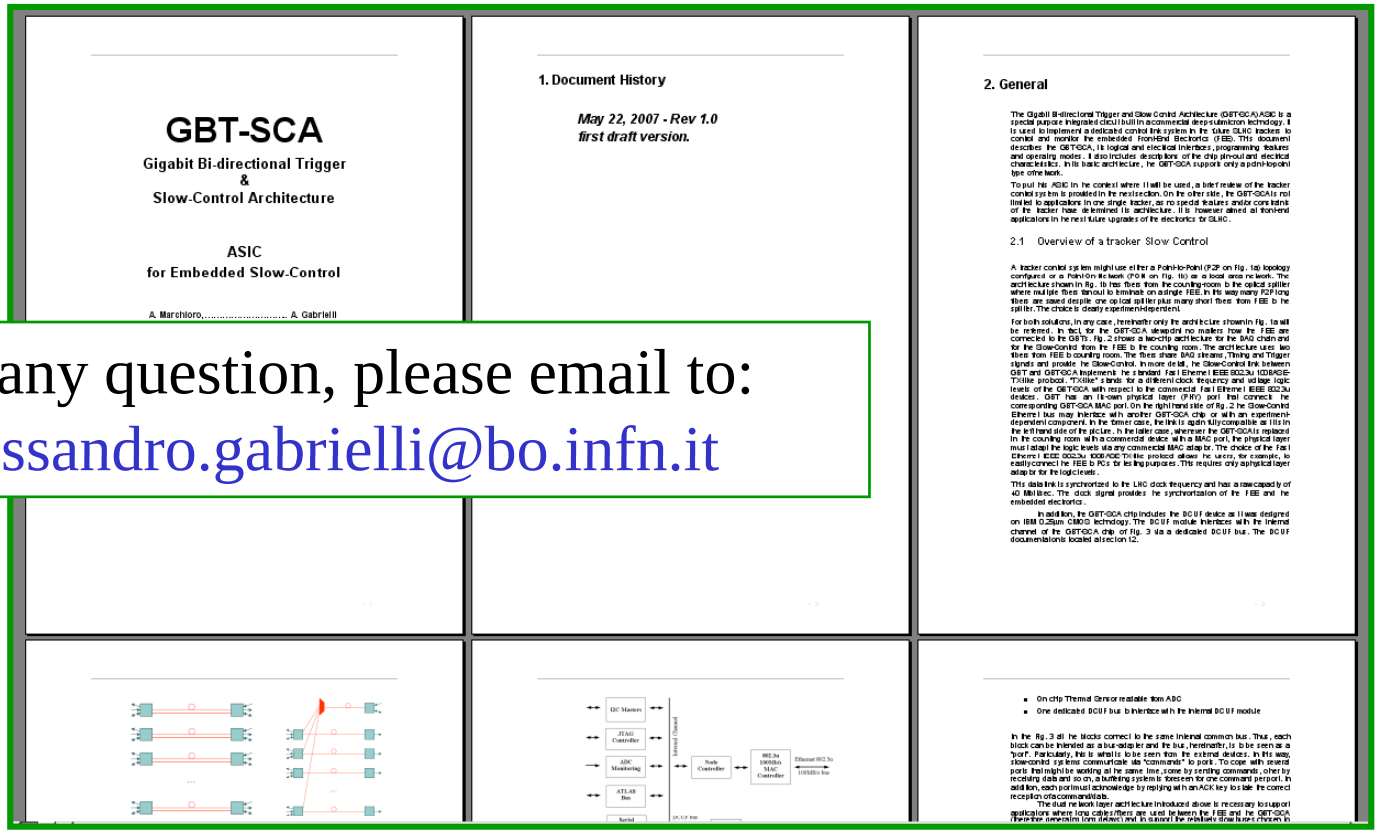
- it will be developed via Verilog code,

- it will be designed by Bologna-Bari with the supervision of CERN

- it will be implemented on a FPGA-based board first (Bari), then the ASIC will be designed

The GBT-SCA Users' Manual

Everyone is invited to partecipate to define the GBT-SCA spec. depending on the experiment requirements



For any question, please email to:
alessandro.gabrielli@bo.infn.it

CONCLUSIONS

- The project is at the beginning but **ongoing**

- The project **IS NOT** experiment-dependent

- The main aim is to let users test their FEC at home (first) via common buses and standard protocols

- It is planned to submit some block prototypes first to test the anti-SEU logic

- It is planned to submit the GBT-SCA by Q4/2007 →Q1/2008