CMOS technologies in the 100 nm range for rad-hard front-end electronics in future collider experiments

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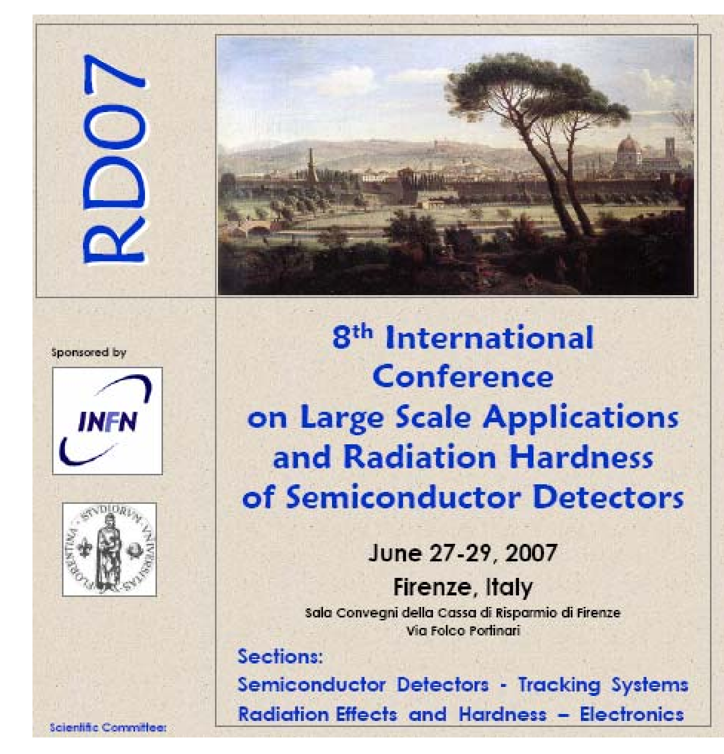


Motivation

- Future generation of HEP experiments (LHC upgrade, ILC, Super B-Factory): mixed signal integrated circuits for the readout of silicon pixel and microstrip detectors designed in 130 nm (90 nm) CMOS processes
- Industrial technology development is driven by digital circuits; the critical aspects for detector readout chips are noise performance, power dissipation and radiation damage
- Inner SLHC detectors: ultra-deep submicron systems exposed to ionizing radiation doses of 100 Mrad and beyond
- While the scaling of the gate oxide thickness to about 2 nm gives a high degree of radiation tolerance, issues such as the gate tunneling current and the sidewall leakage associated to lateral isolation oxides must be investigated.
- With special focus on the design of analog front-end circuits for silicon pixel and strip detectors, the impact of ionizing radiation on the noise performance is evaluated and the underlying physical degradation mechanisms are pointed out to provide criteria for improving radiation hardness properties.
- Sensitivity to Single Event Effects (SEE) can be a major problem for digital systems in 100-nm scale CMOS. The discussion of SEE and of circuit design for SEE immunity is beyond the scope of this talk.

Investigated technologies and devices

- Standard open layout PMOS and NMOS transistors from HCMOS9 130 nm and CMOS090 90 nm triple well, epitaxial CMOS technologies by STMicroelectronics

HCMOS9 (L_{min}=130 nm)

Technology features:

- V_{DD} = 1.2 V
- Physical oxide thickness t_{OX}= 2 nm
- C_{OX}=15 fF/μm^2

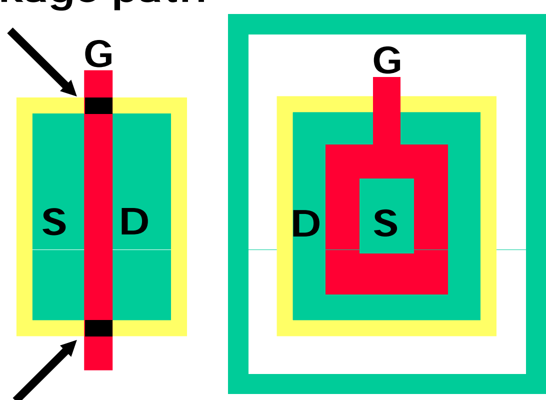
CMOS090 (L_{min}=90 nm)

Technology features:

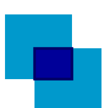
- V_{DD} = 1 V
- Physical oxide thickness t_{OX}= 1.6 nm
- C_{OX}=18 fF/μm^2

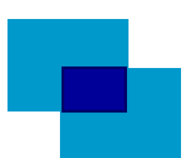
- Enclosed layout NMOS transistors (and standard PMOS) from 2nd 130 nm CMOS vendor (CERN)

Leakage path



Standard Enclosed





Irradiation tests

- Front-end integrated circuits for inner detectors at SLHC must feature a high radiation resistance, up to several hundred Mrad total dose of ionizing radiation.

- Outer SLHC detector layers and less demanding (in terms of rad-hard requirements) collider experiments set radiation tolerance specifications of several Mrad on front-end electronics

10 Mrad irradiation

^{60}Co γ-rays
- 90 nm and 130 nm open layout devices from STMicroelectronics

10 keV X-rays
- PMOS and enclosed NMOS from 2nd 130 nm vendor

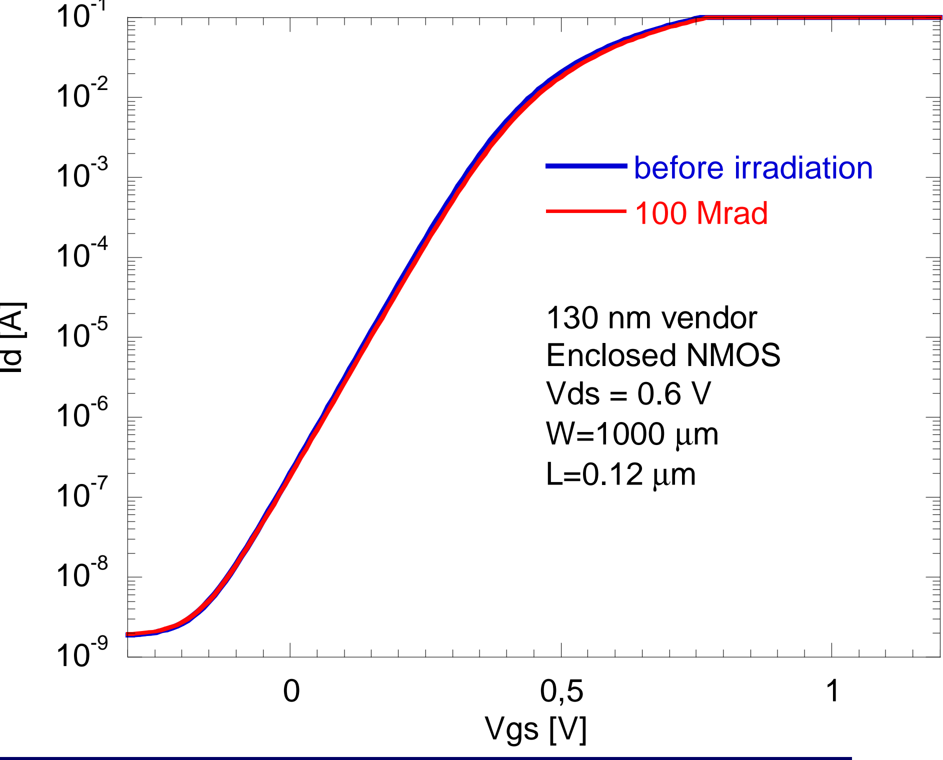
100 Mrad irradiation

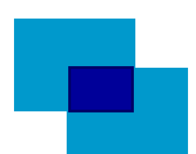
10 keV X-rays
- 90 nm open layout devices from STMicroelectronics
- PMOS and enclosed NMOS from 2nd 130 nm vendor

- The MOSFETs were biased during irradiation in the worst-case condition (all terminals grounded, except gate of NMOS kept at V_{DD})

Ionizing radiation effects and scaling of the gate oxide thickness in ultra deep submicron CMOS

- In very thin gate oxides (2 nm), radiation induced positive trapped charge is removed by tunneling processes
- Effects on threshold voltage and static drain current characteristics are very small; threshold voltage shift at 100 Mrad is of the order of 1 mV, if any
- In PMOSFETs and in enclosed 130 nm NMOSFETs, Id vs Vgs curves are unaffected by irradiation.



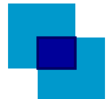


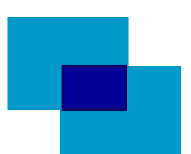
Radiation effects in open layout NMOS

- Radiation induced increase of the drain current is apparent in the constant leakage current zone and in the subthreshold region. This effect is larger in the 130 nm devices, whereas the impact is minor in 90 nm transistors. This behavior is associated to the lateral parasitic transistors at the edge of the device.

I_D [A]
10^{-1} 10^{-2} 10^{-3} 10^{-4} 10^{-5} 10^{-6} 10^{-7} 10^{-8} 10^{-9}
Prerad
10 Mrad
V_{DS}=0.6 V
NMOS 130 nm
W=1000 μm
L=0.13 μm
0 0,5 1
V_{GS} [V]

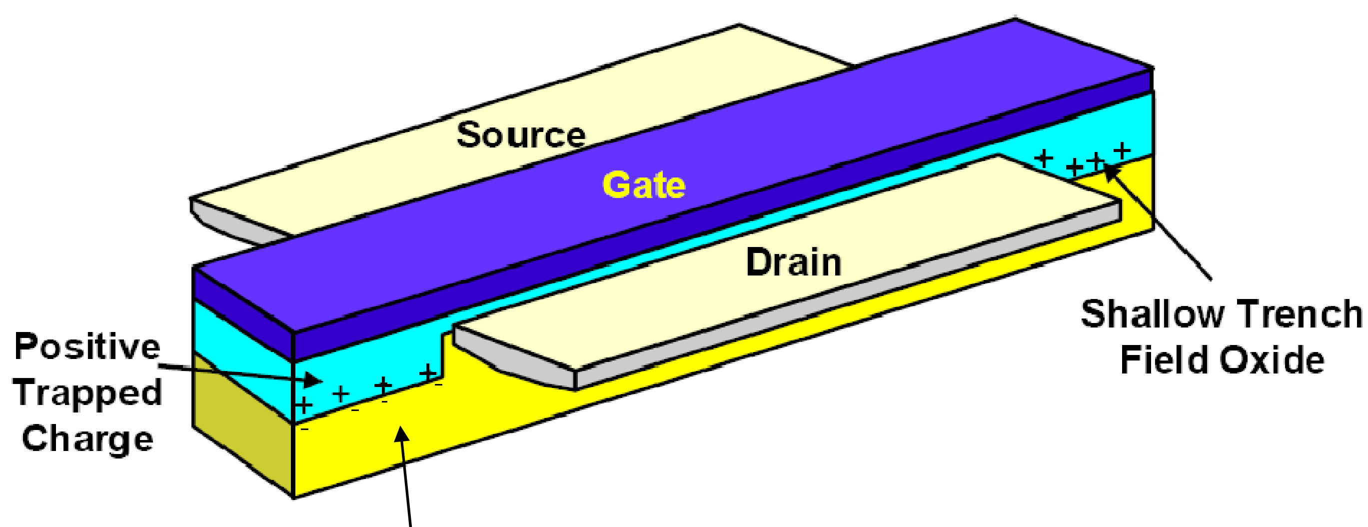
I_d [A]
10^{-1} 10^{-2} 10^{-3} 10^{-4} 10^{-5} 10^{-6} 10^{-7} 10^{-8}
pre-rad
100Mrad
90 nm STMicroelectronics
NMOS, W/L = 200/0.13
Vds=0.6V
-0,2 0 0,2 0,4 0,6 0,8 1
V_{gs} [V]



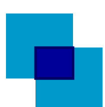


Radiation effects in lateral isolation structures

- In deep submicron bulk CMOS devices exposed to ionizing radiation, the main degradation effects are associated to the thick (~ 300 nm) lateral isolation oxides (STI = Shallow Trench Isolation).

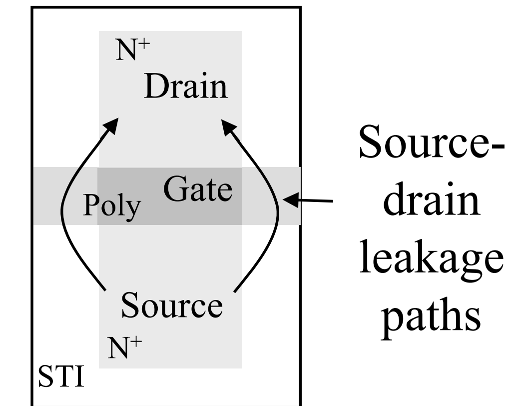


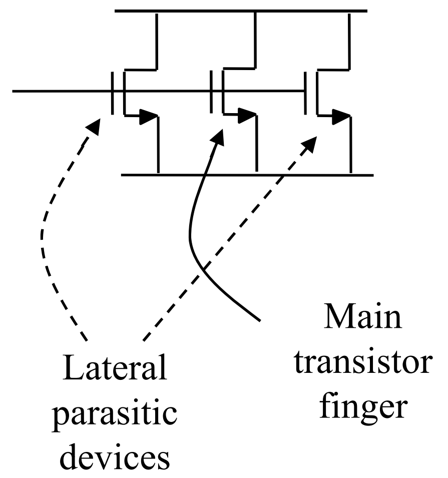
- Radiation-induced positive charge trapped in isolation oxides may invert a P-type region in the well/substrate of NMOSFETs creating a leakage path between source and drain.



Radiation effects in lateral isolation structures

- Lateral parasitic transistors turn on because of charge build up in STI oxides.
- The parasitic devices add a contribution to the total drain current and noise of NMOSFETs.
- We developed a model to account for the white and 1/f noise degradation due to the effect of lateral parasitic transistors.



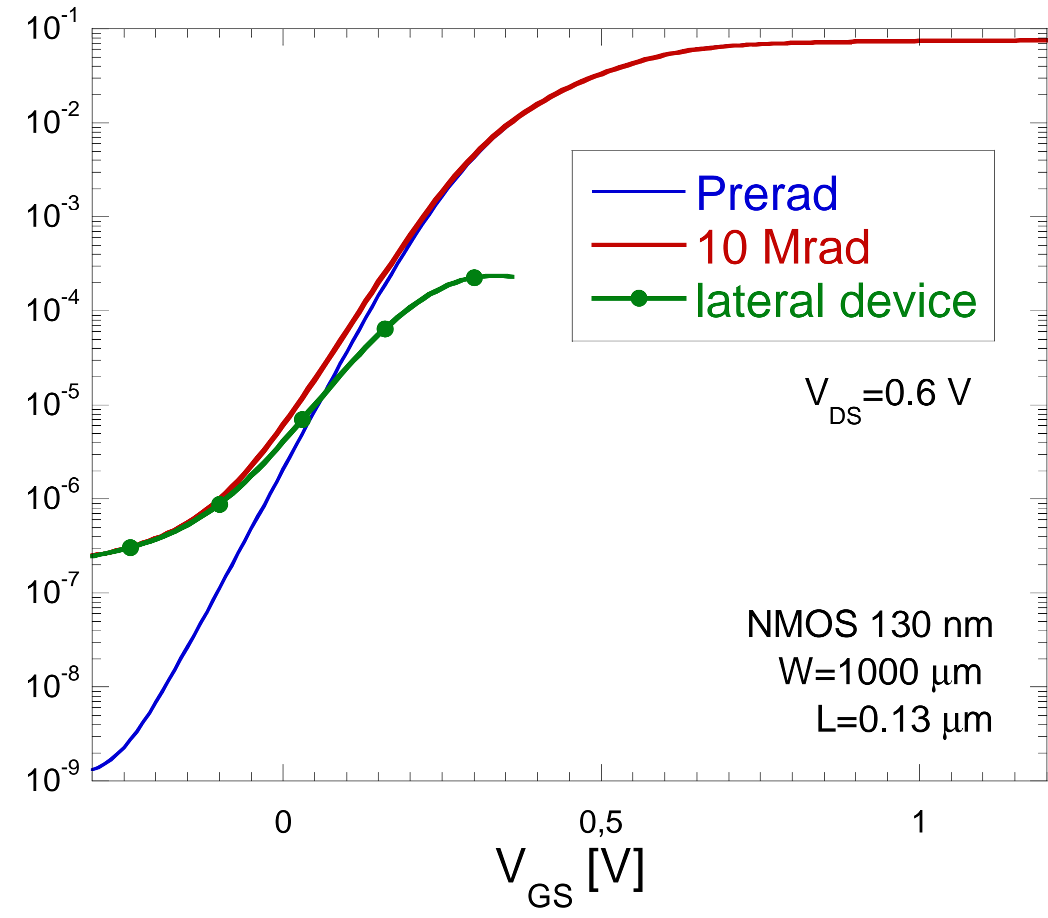


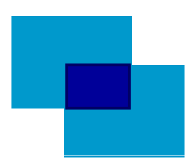
V. Re et al, "Impact of lateral isolation oxides on radiation-induced noise degradation in CMOS technologies in the 100 nm regime", NSREC '07

Radiation effects in lateral isolation structures

- For devices with a large W/L ratio (no narrow channel effect) the total contribution from lateral devices can be disentangled from the drain current of the main transistor controlled by the gate oxide.

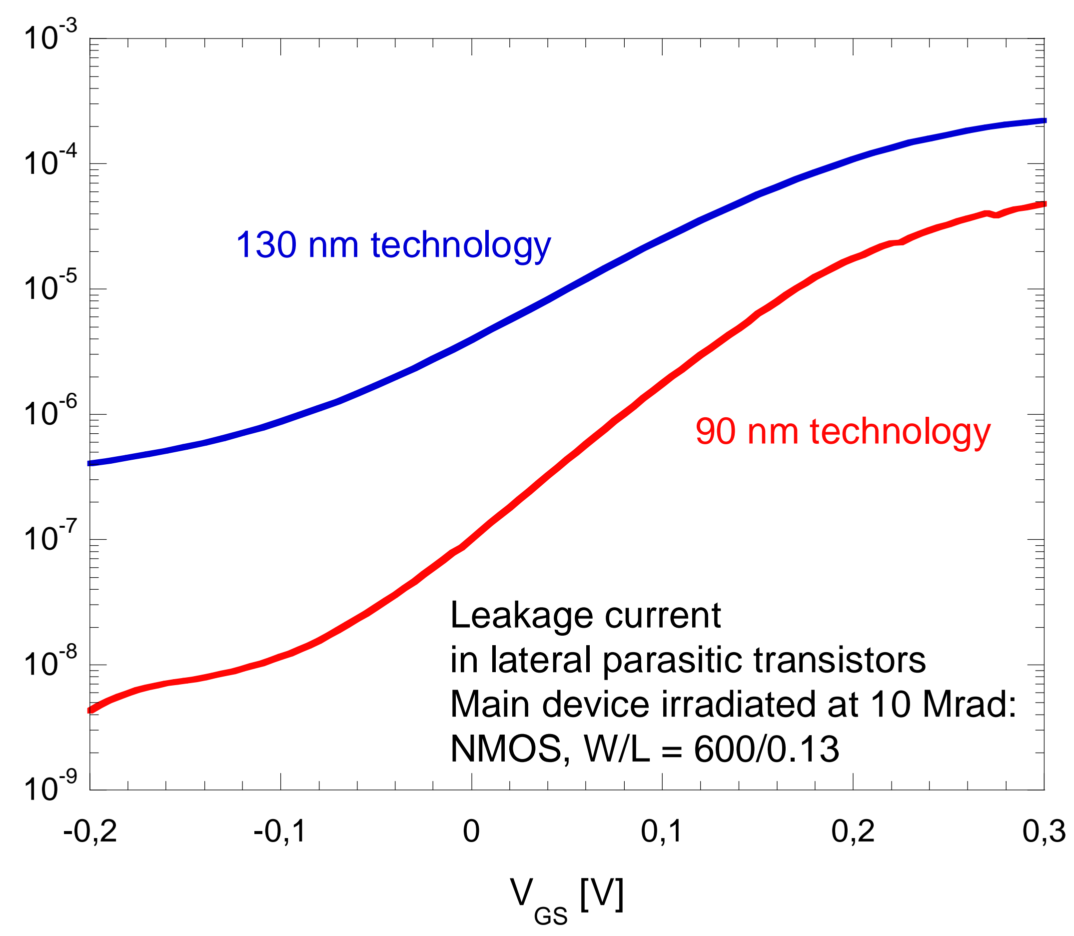
- The impact of lateral parasitic devices is larger at small current densities $I_D \cdot L/W$

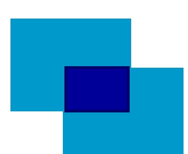




Radiation effects in lateral isolation structures

- The drain current is more severely affected by sidewall leakage in the 130 nm technology as compared to the 90 nm one. This could be explained by a higher doping concentration in the p-type body for the 90 nm process, which mitigates the inversion of the surface along the STI sidewalls.



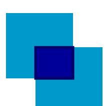


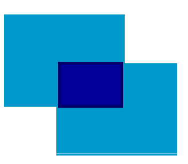
Radiation effects on noise

- Signal-to-noise ratio is a critical issue for the design of silicon tracking and vertexing detectors.

- Noise vs power performance and radiation effects on noise are crucial parameters for the choice of the technology for integrated front-end electronics, especially in view of operating with thin and/or heavily irradiated silicon detectors, where the collected charge will be considerably smaller than for standard 300 μm sensors.

- In 100-nm scale open layout CMOS devices, 1/f noise at small drain current density is among the few parameters which are sensitive to ionizing radiation.





Radiation effects on noise

Noise in the drain current of a MOSFET can be represented through an equivalent noise voltage source in series with the device gate

$$S_V^2(f) = S_W^2 + S_{1/f}^2(f)$$

S_W - white noise

- channel thermal noise (main contribution in the considered operating conditions)

$$S_{ch}^2 = \frac{4k_B T\Gamma}{g_m}, \quad \Gamma = \alpha_W n\gamma$$

- k_B Boltzmann's constant
- T absolute temperature
- α_W excess noise coefficient
- γ channel thermal noise coefficient

- other contributions from parasitic resistances

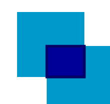
$S_{1/f}$ - 1/f noise

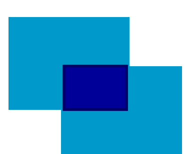
- technology dependent contribution

$$S_{1/f}^2(f) = \frac{K_f}{C_{OX} W L f^{\alpha_f}}$$

- k_f 1/f noise parameter
- α_f 1/f noise slope-related coefficient

- both k_f and α_f depend on the polarity of the DUT





Radiation effects on noise: NMOS 90 nm

- In 90 nm open layout NMOSFETs, at 10 Mrad total dose the main radiation effect is a 1/f noise increase at low current density, due to the contribution of lateral parasitic devices. No increase in the white noise region is detected.

before irradiation
10 Mrad
90 nm process
NMOS W/L=200/0.20
Id=20 μA @ Vds=0.6 V
Noise Voltage Spectrum [nV/Hz$^{1/2}$]
Frequency [Hz]
1000
100
10
1
10^3 10^4 10^5 10^6 10^7 10^8

before irradiation
10 Mrad
90 nm process
NMOS W/L=200/0.20
Id=250 μA @ Vds=0.6 V
Noise Voltage Spectrum [nV/Hz$^{1/2}$]
Frequency [Hz]
1000
100
10
1
10^3 10^4 10^5 10^6 10^7 10^8

Radiation effects on noise: NMOS 90 nm

- At 100 Mrad, there is no sizable difference in radiation effects with respect to 10 Mrad. A further increase of 1/f noise is detected.

Noise Voltage Spectrum [nV/Hz$^{1/2}$]

before irradiation
100 Mrad

90 nm process
NMOS W/L=200/0.20
Id=20 μA @ Vds=0.6 V

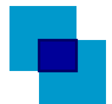
Frequency [Hz]

Noise Voltage Spectrum [nV/Hz$^{1/2}$]

before irradiation
100 Mrad

90 nm process
NMOS W/L=200/0.20
Id=250 μA @ Vds=0.6 V

Frequency [Hz]



Radiation effects on noise: NMOS 130 nm open layout

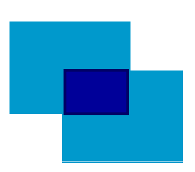
- In 130 nm open layout NMOSFETs, at 10 Mrad total dose the main radiation effect is again a 1/f noise increase at low current density, due to the contribution of lateral parasitic devices. Since the impact of lateral devices is larger for this process, a noise increase in the white spectral region is also detected at low currents.

STM 130 nm process
open layout
NMOS W/L=1000/0.20
Id=100 μA
Vds=0.6 V

Noise Voltage Spectrum [nV/Hz$^{1/2}$]
100
10
1
before irradiation
10 Mrad
10^3 10^4 10^5 10^6 10^7 10^8
Frequency [Hz]

STM 130 nm process
open layout
NMOS W/L=1000/0.20
Id=1 mA
Vds=0.6 V

Noise Voltage Spectrum [nV/Hz$^{1/2}$]
100
10
1
before irradiation
10 Mrad
10^3 10^4 10^5 10^6 10^7 10^8
Frequency [Hz]



Radiation effects on noise: NMOS 130 nm enclosed

In 130 nm enclosed NMOSFETs, at 100 Mrad total dose, noise degradation is negligible. This provides evidence for a model where the basic mechanism underlying noise increase in irradiated devices is associated to lateral parasitic transistors.

2nd 130 nm vendor
NMOS enclosed
W/L=1000/0.24
Id=100 μA @ Vds=0.6 V

Noise Voltage Spectrum [nV/Hz$^{1/2}$]

100
10
1
0,1

10^3 10^4 10^5 10^6 10^7 10^8

Frequency [Hz]

before irradiation
100 MRad

2nd 130 nm vendor
NMOS enclosed
W/L=1000/0.24
Id=1 mA @ Vds=0.6 V

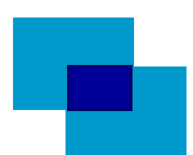
Noise Voltage Spectrum [nV/Hz$^{1/2}$]

100
10
1
0,1

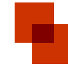
10^3 10^4 10^5 10^6 10^7 10^8

Frequency [Hz]

before irradiation
100 MRad

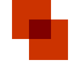


Radiation effects on noise: PMOS

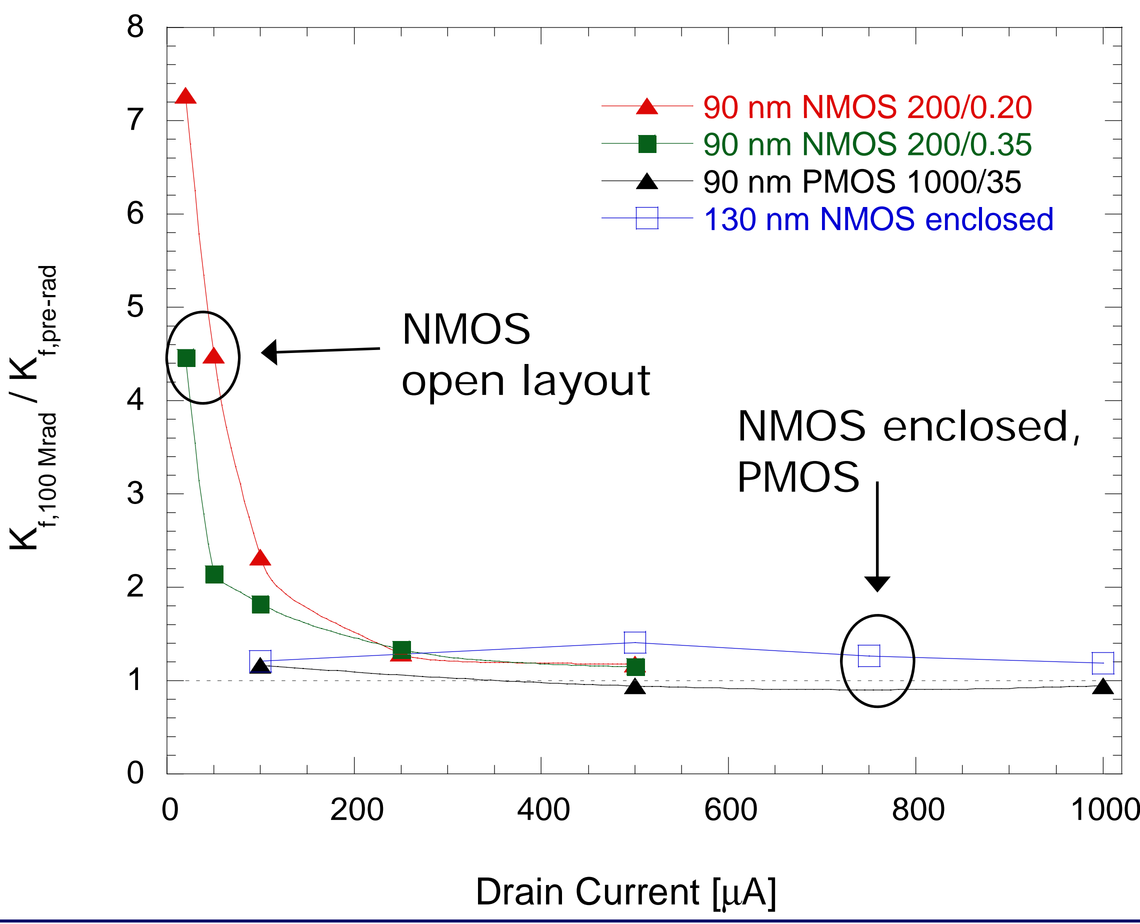


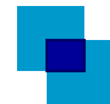
In 130 nm and 90 nm PMOS (open layout), even at 100 Mrad total dose, noise degradation is negligible. This is in agreement with the absence of sidewall leakage current contributions.

1/f noise coefficient K_f



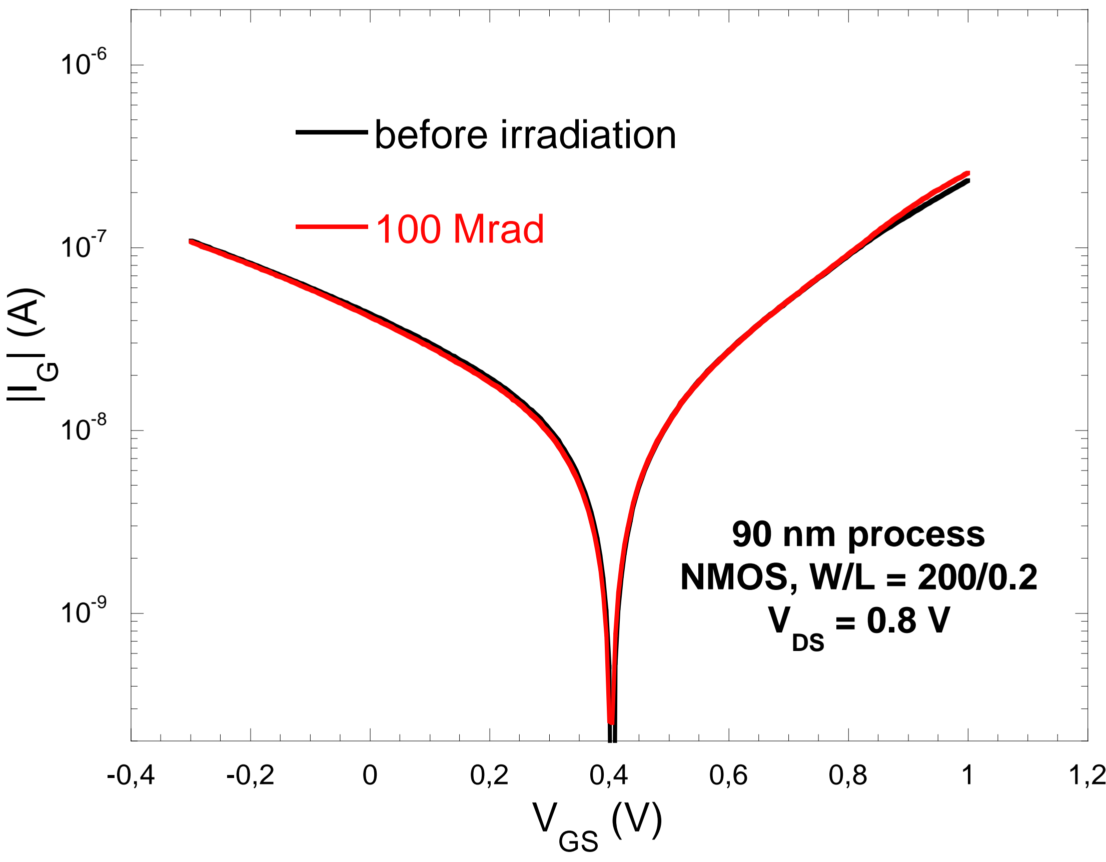
At 100 Mrad total dose, K_f is very close to preirradiation values for enclosed NMOS and for PMOS. Instead, K_f sizably increases at low drain current density for open layout NMOS.





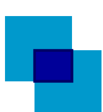
Ionizing radiation effects on the gate leakage current

The absorption of a 100 Mrad total dose marginally affects the gate leakage current (mostly due to direct tunneling through the thin gate oxide). However, there may be reliability problems (hard oxide breakdown) to be investigated.



Thick oxide I/O devices

- In 90 nm CMOS, the gate current due to tunneling effects may play a sizable role affecting the signal-to-noise ratio of a front-end system, especially at peaking times above 100 ns. To avoid this problem, we could use devices with thicker gate oxide and higher VDD available in advanced CMOS technologies.
- However, a thicker gate oxide may give worse noise performances and is more sensitive to ionizing radiation.
- Preliminary tests on the STM 90 nm process show that I/O 2.5 V NMOSFETs have a 1/f noise parameter K_f 20 times bigger than standard core transistors with thin oxide.



Low noise charge preamplifier design

- Circuit designers can take advantage of single device characterization to predict noise behavior of charge sensitive amplifiers

- Equivalent noise charge is the figure of merit to be minimized:

$$ENC = (C_D + C_g)\sqrt{A_1 \frac{4k_B T\Gamma}{g_m}\frac{1}{t_p} + (2\pi)^{\alpha_f} A_2(\alpha_f)\frac{k_f}{C_{OX}WL}\frac{1}{t_p^{1-\alpha_f}}}$$

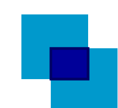
Channel thermal noise contribution

Flicker noise contribution

- C_D detector capacitance
- C_G preamplifier input capacitance
- t_p peaking time
- A_1 A_2 shaping coefficients

- Data extracted from single transistor characterization can be used to plot minimum ENC as a function of the main design parameters (peaking time, power dissipation, polarity and dimensions of the preamplifier input device)

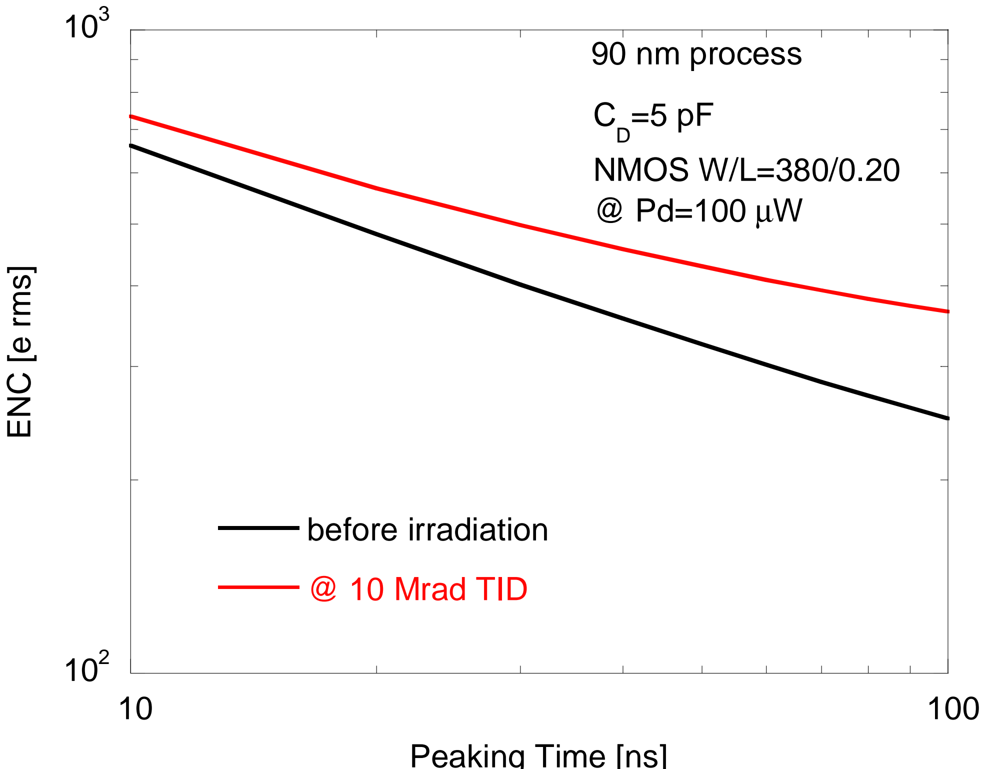
- It is interesting to assess the impact of ionizing radiation effects on the S/N achievable with front-end electronics in 100 nm – scale CMOS



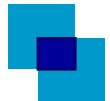
Ionizing radiation effects on signal-to-noise ratio: strip readout with 90 nm electronics, NMOS input

- At 10 Mrad, at the low current density dictated by power dissipation constraints, the 1/f noise increase affects ENC also in 25 – 50 ns peaking time region.

- The device width W is optimized as a function of the detector capacitance for the peaking time region around 50 ns under typical power dissipation constraints

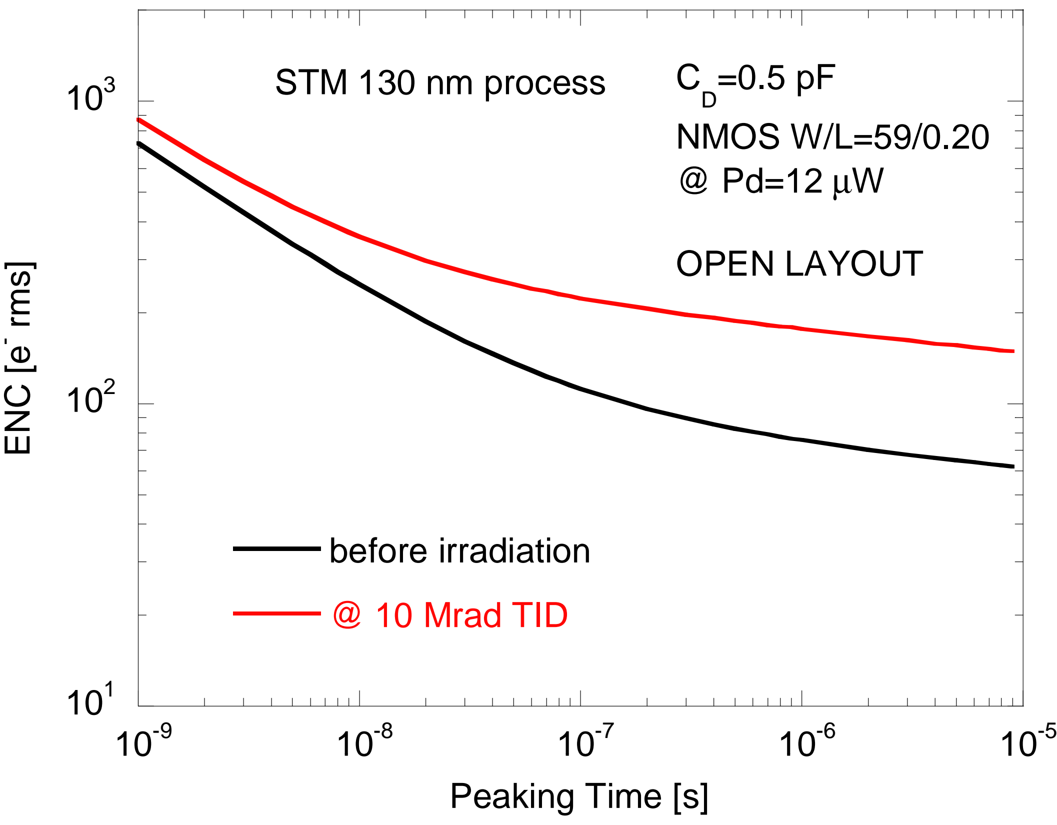


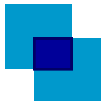
- ENC estimates based on measured noise parameters show that ENC increases by about 20% at t_p = 25 ns (430 e → 520 e) and by about 30 % at t_p = 50 ns (325 e → 430 e) (the noise contribution from the gate leakage current can be neglected in this range)



Ionizing radiation effects on signal-to-noise ratio: pixel readout with 130 nm electronics, standard input NMOS

- Even at 10 Mrad, the white and 1/f noise degradation increase ENC by 60 – 80 % in the 25 – 50 ns peaking time region.



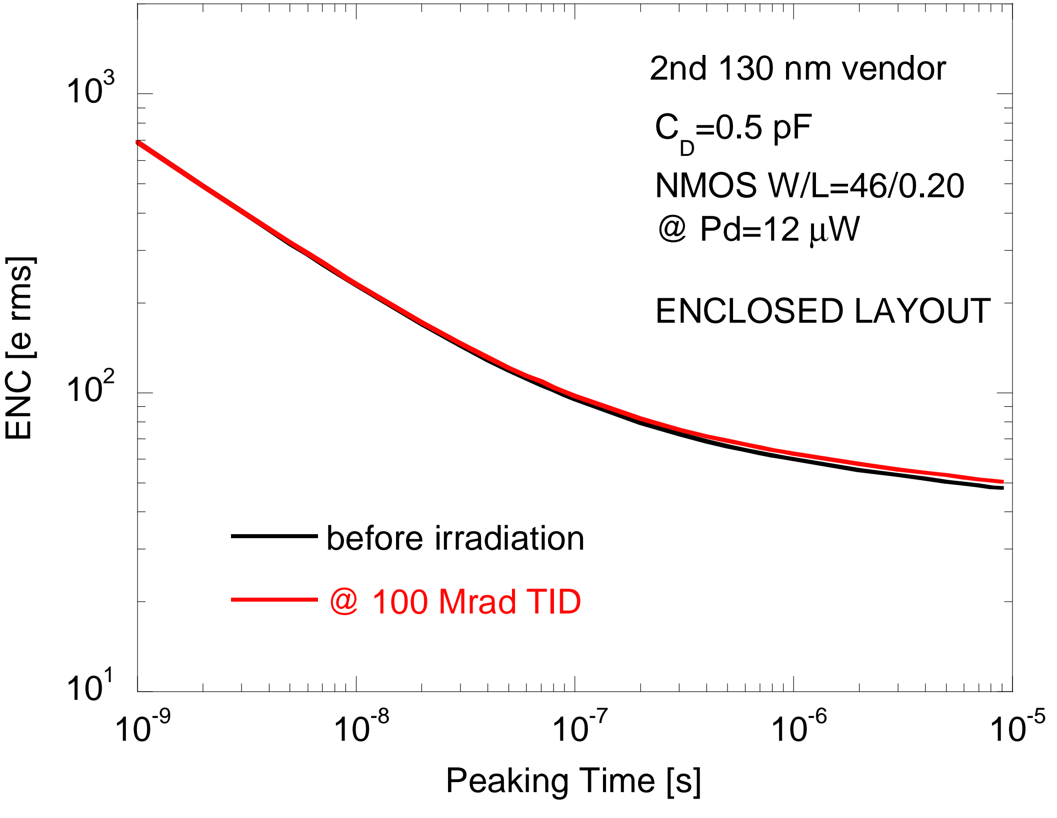


Ionizing radiation effects on signal-to-noise ratio: pixel readout with 130 nm electronics, enclosed input NMOS

- Since there are no lateral parasitic devices turning on and contributing to noise, on the basis of irradiation tests we can predict that ENC is not affected by the absorption of high ionizing radiation doses (100 Mrad).

- ENC = 150 e rms at t_P=25 ns

  ENC = 120 e rms at t_P = 50 ns

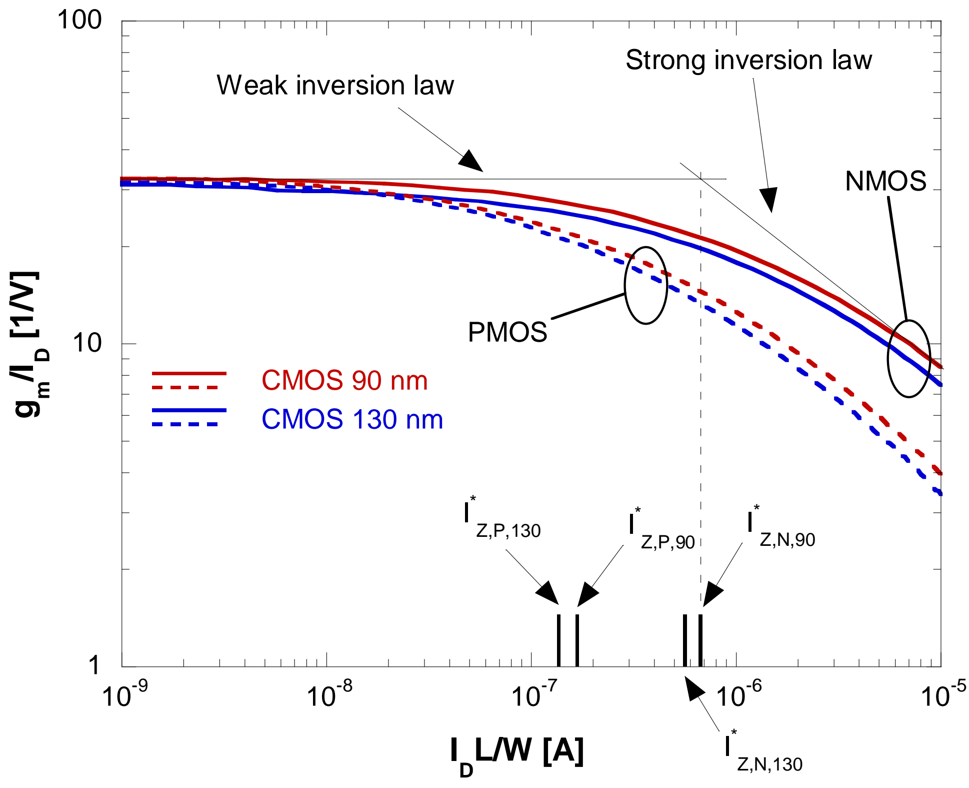


- Irradiation tests have been performed on devices belonging to the 130 nm and 90 nm CMOS technology nodes, likely candidates for the design of readout electronics in future high luminosity collider experiments.
- As a general conclusion, test results confirm that CMOS technologies in the 100 nm regime exhibit a high degree of radiation tolerance and that they are suitable for the design of rad-hard readout electronics (with a few caveats) even for very harsh radiation environments such as the SLHC.
- Experimental results show that in NMOS devices exposed to ionizing radiation 1/f noise increases because of the contribution from the lateral parasitic transistors along the STI sidewalls. White noise may also increase after irradiation if the impact of these parasitic devices on the drain current is large.
- Since the noise increase is mostly evident at low current density, this suggests to carefully evaluate the use of NMOSFETs for low noise functions in analog circuits operating under power dissipation constraints.
- This mechanism does not take place in P-channel devices and in enclosed NMOSFETs, which may be used instead of standard interdigitated devices if a low noise performance after the exposure to high TID levels (as in inner SLHC layers) is an essential requirement.

Backup slides

Operating region

- Drain current in DUTs: from tens of μA to 1 mA → low power operation as in high density front-end circuits

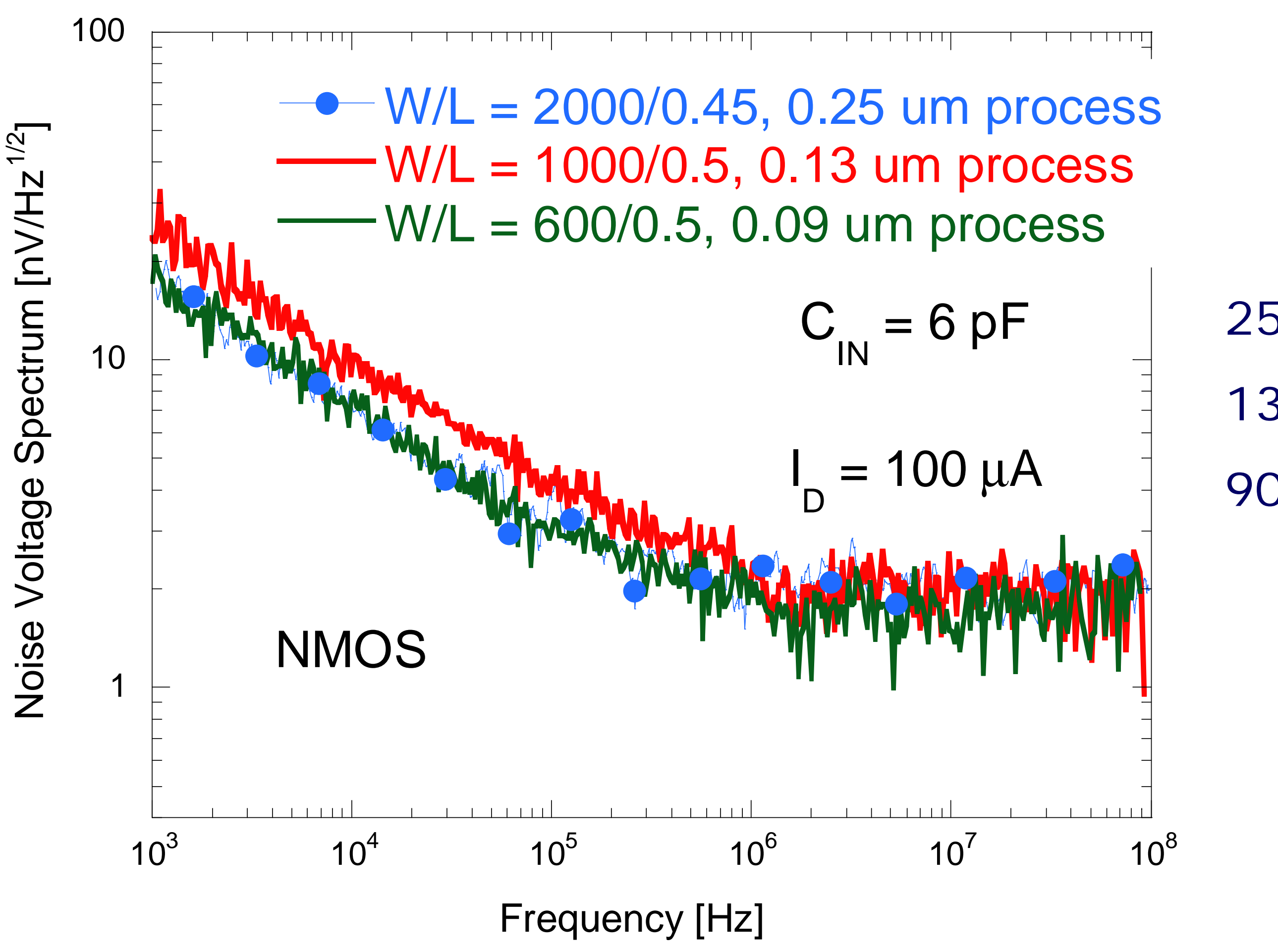


$$I^*_Z = 2\mu C_{OX} n V_T^2$$

- μ carrier mobility
- C_{OX} specific gate oxide capacitance
- V_T thermal voltage
- n proportional to $I_D(V_{GS})$ subthreshold characteristic

- Characteristic normalized drain current I^*_Z may provide a reference point to define device operating region

Noise in different CMOS generations

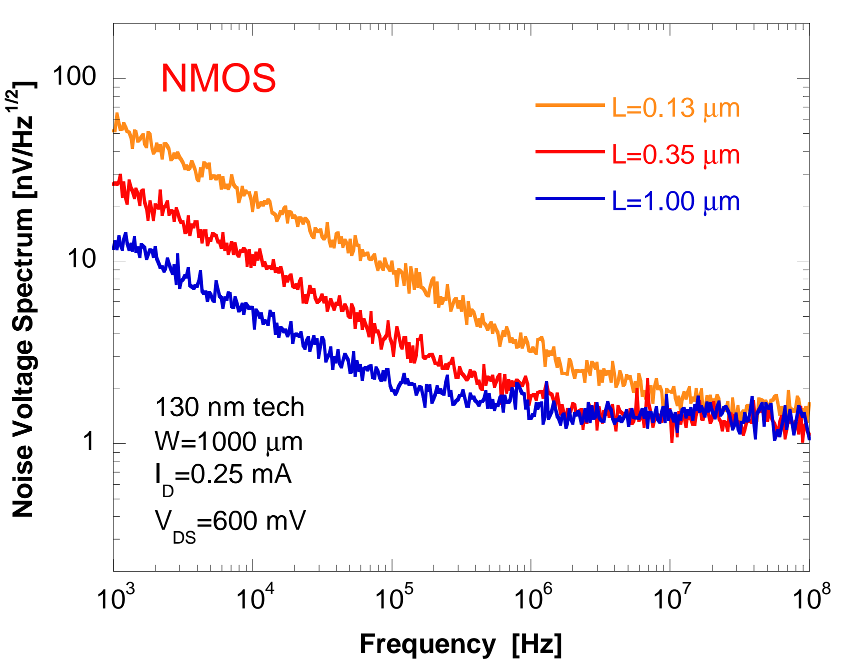


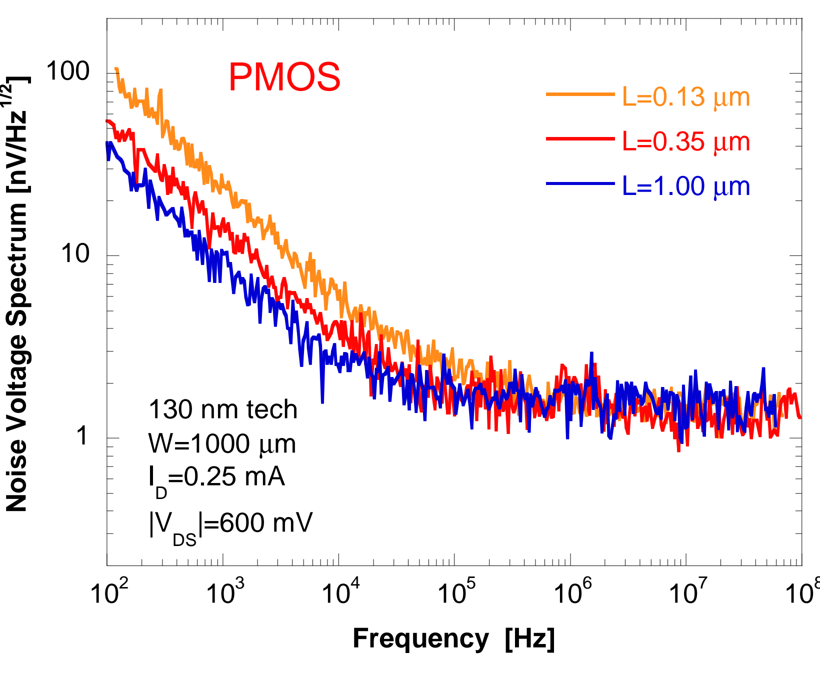
250 nm TSMC

130 nm STM

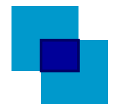
90 nm STM

Noise *vs* gate length – STM 130 nm

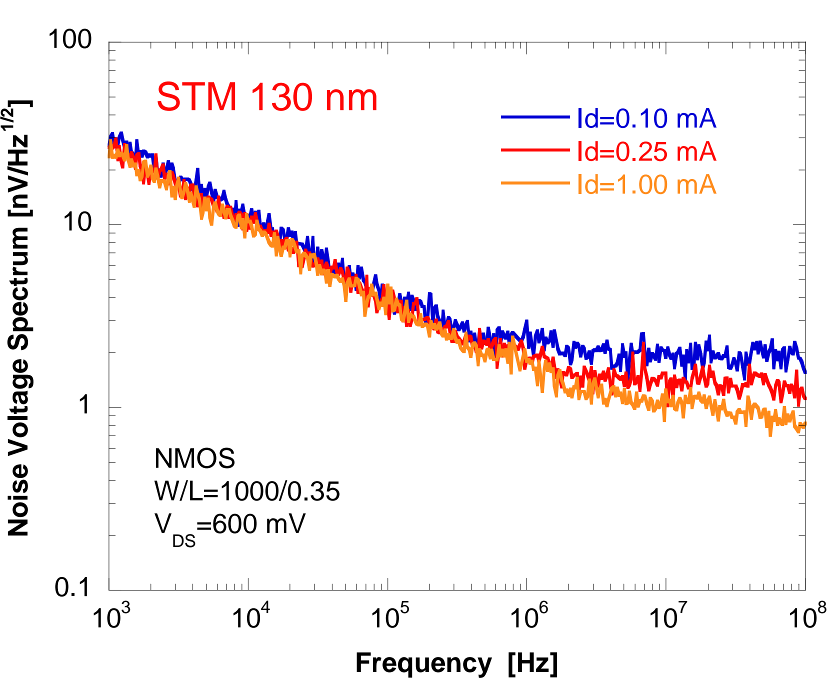


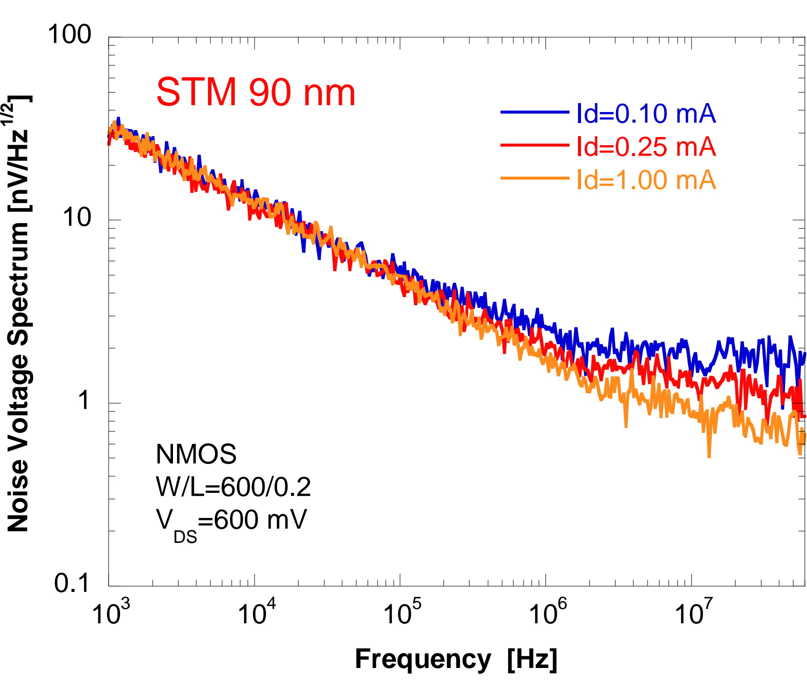


- High frequency, white noise virtually independent of the gate length L, in agreement with g_m behavior
- 1/f noise contribution decreases with increasing channel length, as predicted by the noise equation

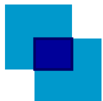


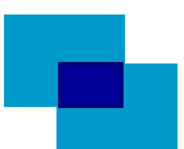
Noise *vs* drain current - NMOS



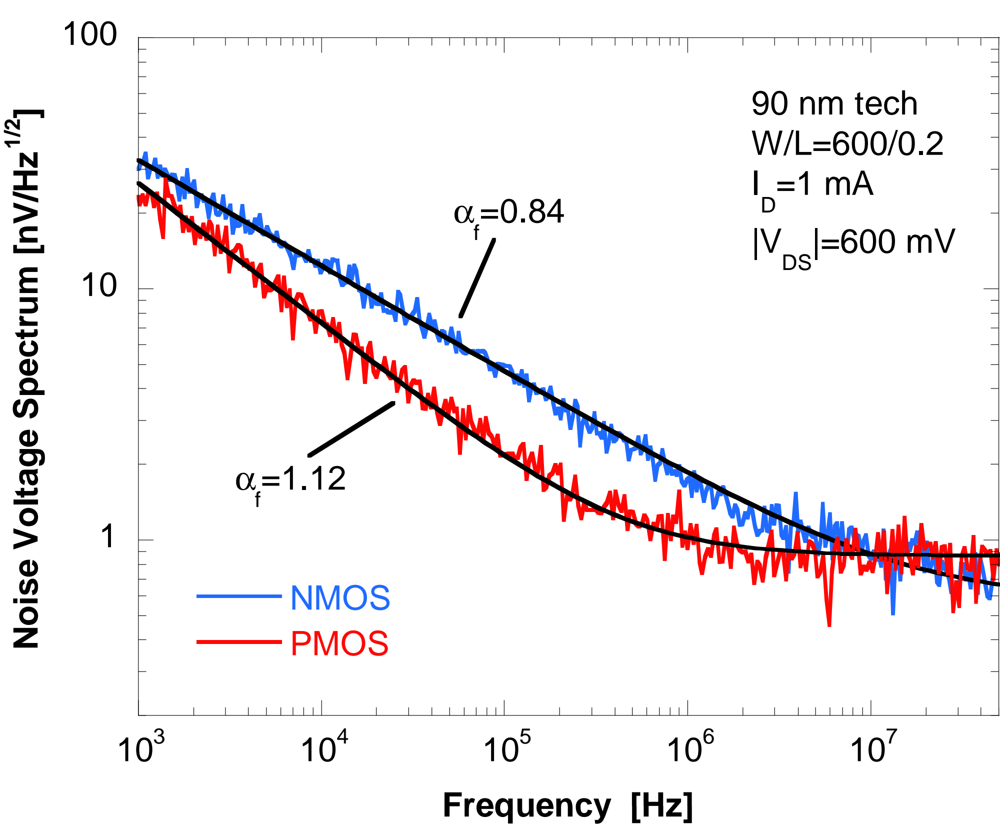


- High frequency, white noise decreases with increasing drain current in both technologies, in agreement with g_m behavior
- 1/f noise contribution is to a large extent independent of the drain current





Flicker noise



- Slope α_f of the 1/f noise term is significantly smaller than 1 in NMOS transistors and larger than 1 in PMOS devices