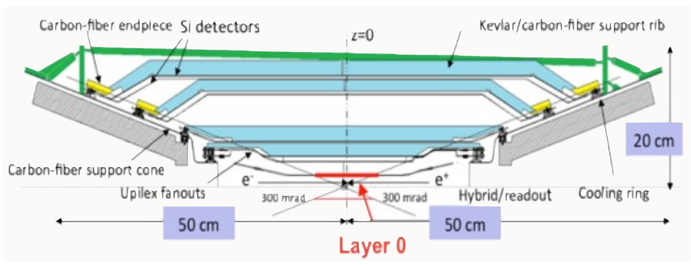
Latest results of the R&D on CMOS MAPS for the Layer0 of the *SuperB* Silicon Vertex Tracker

G. Casarosa, INFN - Sezione di Pisa ~ on behalf of the *SuperB*-SVT Group

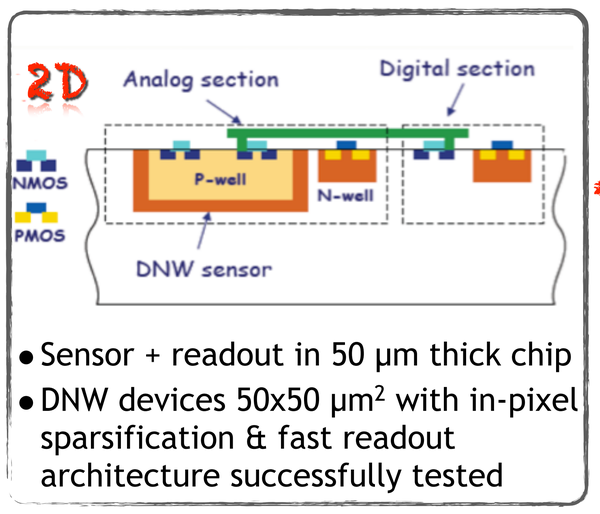
13th Vienna Conference on Instrumentation ~ Feb. 11-15, 2013

giulia.casarosa@pi.infn.it

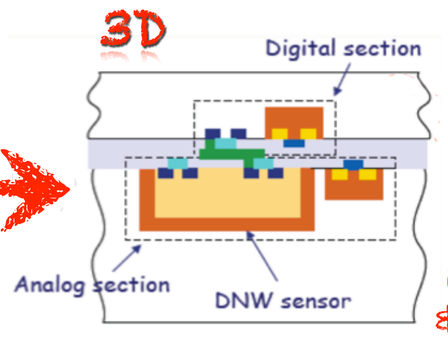
Abstract In ***SuperB*** physics and high background conditions set very challenging requests on readout speed, material budget, radiation damage and resolution for the innermost layer (Layer0) of the Silicon Vertex Tracker (SVT) operated at the full luminosity (10^{36} cm^{-2}s^{-1}). Monolithic Active Pixel Sensors (MAPS) are suited for this application because their thin sensitive region allows grinding the substrate to tens of microns. After achieving in-pixel sparsification and fast time stamping with deep N-well MAPS, developed in the ST 130 nm CMOS technology, further performance improvements are being explored with an intense R&D program, focused on vertical integration and 2D MAPS with the INMAPS quadruple well.

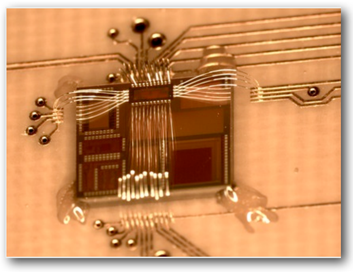


Deep-N-Well MAPS & Vertical Integration



- Sensor + readout in 50 μm thick chip
- DNW devices 50x50 μm^2 with in-pixel sparsification & fast readout architecture successfully tested



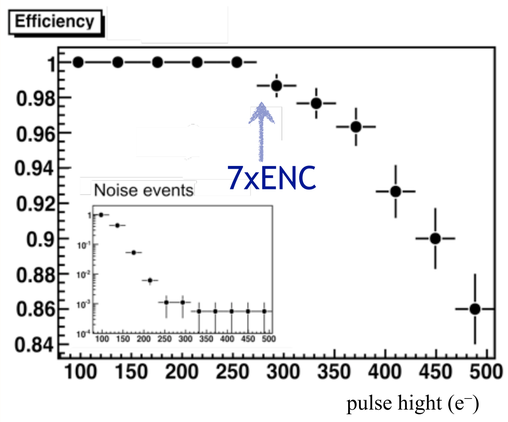


improved performance & higher functionalities

- Two tiers:
  - one for the digital RO + one for the sensor & analog FE
- Reduced surface occupied by competitive N-well
- More space available for in-pixel logic

Charge Collection in the 3D DNW MAPS Matrix (3x3 analog)

- tested on beams:



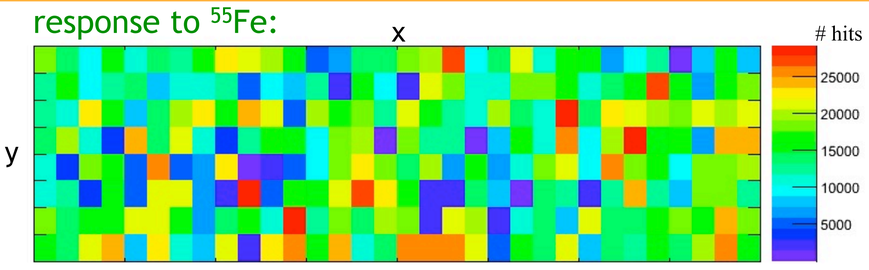
- ➡ cluster signal MPV ≃ 1044 e⁻
- ➡ S/N ≃ 23
- ➡ hit efficiency > 98% up to 7xENC

- tested with ^{55}Fe (5.9 keV γ)
  - ➡ gain ≃ 320 mV/fC
  - ➡ ENC ≃ 45 e⁻

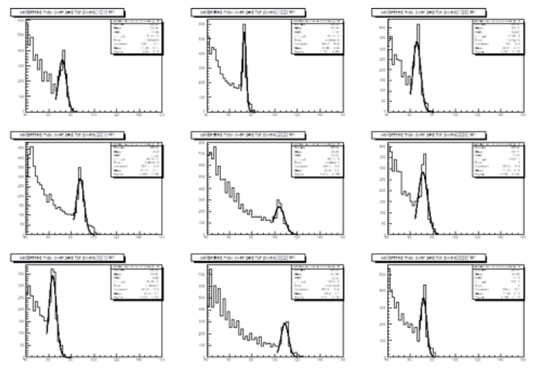
Characterization of the 3D 8x32 DNW MAPS Matrix

- noise scan tests confirm the expected performance:
  - ➡ ENC ≃ 40 e⁻ with 35% dispersion
  - ➡ threshold dispersion ≃ 2.3xENC
- gain calibration with ^{55}Fe shows a large gain dispersion (20%) understood and already fixed for next submission

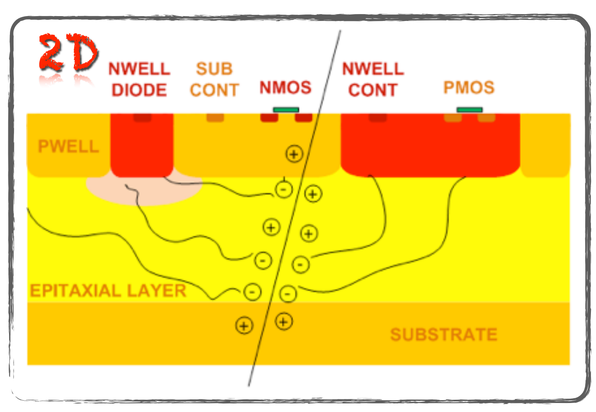
response to ^{55}Fe:

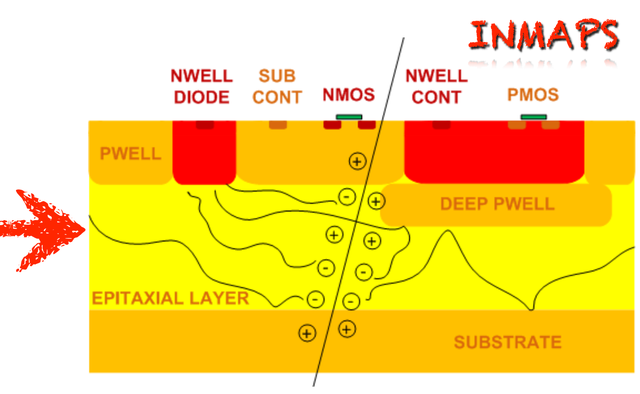


Finally some chips with very good interconnetions between the 2 tiers

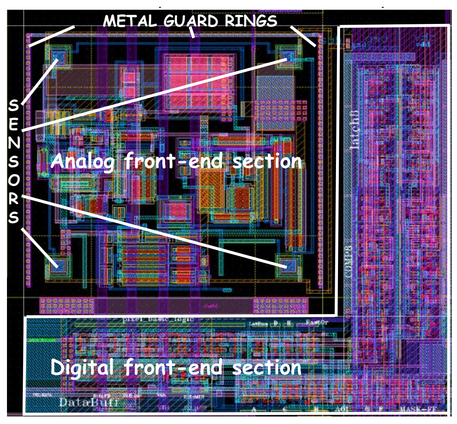


2D MAPS with INMAPS 180 nm



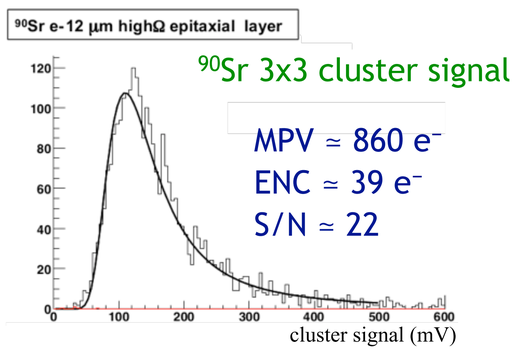


- evolution of the 2D MAPS to a *quadruple* well
- prevents the electrons to be collected by parasitic N-well by enclosing it in a deep P-well
- high-resistivity epitaxial layer (~1 kΩ cm) also available:
  - higher charge collection efficiency and radiation hardness
- implement a new fast (100 MHit/cm^2 target rate & 100 ns timestamp) and flexible readout architecture (triggered & data push)

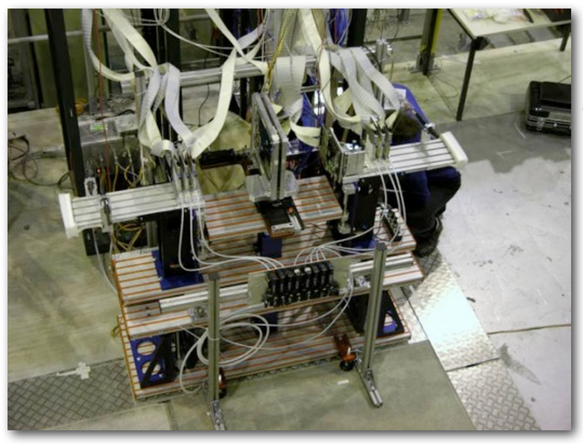


Characterization of the INMAPS Matrix

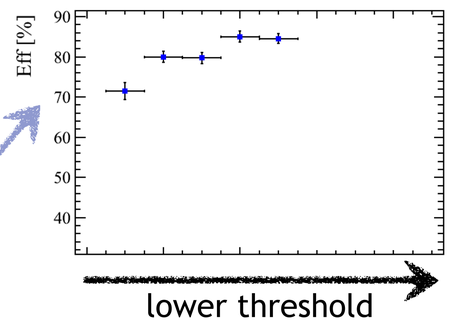
- 3x3 analog matrix:



- tested on beams:

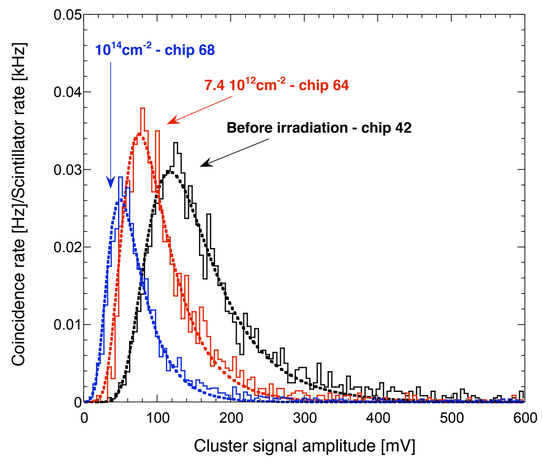


- 32x32 digital matrix:
  - ➡ threshold dispersion ≃ 2xENC
  - ➡ gain calibration with ^{55}Fe shows a good uniformity (5 % dispersion)
  - ➡ both triggered and data push operation modes working as expected

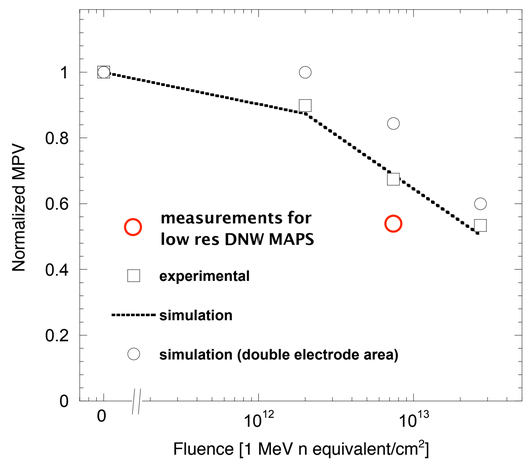


- ➡ matrix efficiency lower than expected
- ➡ efficiency deterioration at low thresholds due to inductions effects still under study

Radiation Hardness Tests on INMAPS



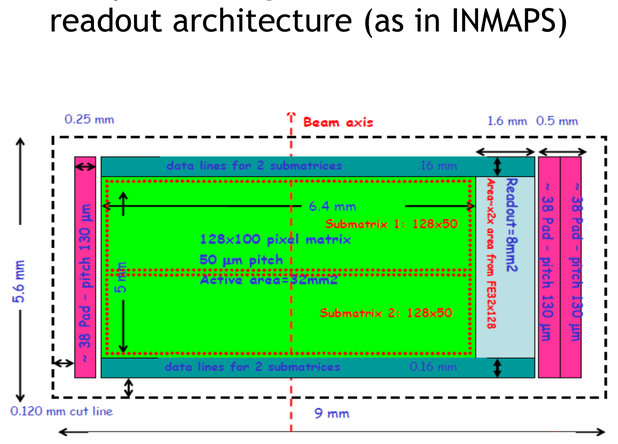
^{90}Sr 3x3 cluster signal



- Improved radiation tolerance w.r.t. low resistivity DNW MAPS
- Radiation hardness may be further improved with an optimized design of electrodes

Further Developments: Next 3D Submission

- *3D Apsel*: a larger CMOS MAPS 3D with optimized sensor design and new readout architecture (as in INMAPS)



charge sensitivity	720 mV/fC
peaking time	300 ns
ENC	42 e⁻
thr. disp. before/after correction	106/15
analog power consum	36 μW/pixel
detector capacitance	320 fF
matrix size	128x100
pixel pitch	50 μm