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Latest results of the R&D on CMOS MAPS for the Layer0 of the SuperB Silicon Vertex Tracker

Physics and high background conditions set very challenging requests on readout speed, low material budget and resolution for the innermost layer (the Layer0) of the SuperB Silicon Vertex Tracker operated at the full luminosity.
Monolithic Active Pixel Sensors are very appealing in this application because the thin sensitive region allows grinding the substrate to tens of microns.
Deep N-well MAPS, developed in the ST 130 nm CMOS technology, achieved in-pixel sparsification and fast time stamping. Further performance improvements are being explored with an intense RD program, including both vertical integration and 2D MAPS with the INMAPS quadruple well.
For the 3D (Tezzaron/Chartered) process, several chips have been characterized with IR laser, radioactive sources and beam. The results on the various sensors (3x3 matrix with analog information available and 8x32 digital matrix) are reported, with the design implemented in the second foundry run.
The other approach exploits the features of the quadruple well and the high resistivity epitaxial layer of the INMAPS 180 nm process. This technology allows overcoming the main limitations of the DNW MAPS, in terms of collection efficiency and radiation hardness in a timeline reasonable for application in SuperB. An irradiation campaign with neutrons has been performed on small matrices and other test-structures. These promising results together with the response of the sensors to high energy charged tracks are presented.

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