Recent developments in silicon detectors

G. Casse
Physics and detectors: a virtuous spiral

Physics experiments update their requirements

Detectors change and enable change of physics interests

Detector technologies evolve towards:
• Faster rates
• Higher resolution
• Increase of multiplicities

1920-1950 nuclear emulsions with cosmics cloud chambers 1 frame/week
1950-1980 bubble chambers spark chambers 1 frame/s
1970-2000 wire chambers
1980-now calorimeters
1980-now silicon trackers LHC $10^7$ frames/s
Silicon detectors

“He was a hard-headed man
He was brutally handsome, and she was terminally pretty ...............”

Silicon sensors and readout electronics
Silicon detectors

Semiconductor detectors developed **1943** (Utrecht) – **1955** (Bell Labs, Oak Ridge)
Surface barrier diodes on Ge (**1949**) and on Si (**1955**)
Diffused Si junctions and p-i-n/n-i-p introduced ~**1958-1960**
Ion-implanted diodes from ~**1960** by J.Mayer and others (e.g. at Philips Amsterdam)
Several diodes on same slice was done 'right away' at AERE, LBL and CEA Saclay
Patent on double-sided Si 'checker board' detector by Philips (NL) in **1967**
Surface barrier microstrip sensors for experiments (**1980**-NA11, 100-200µm strip pitch)

Thanks to E. Heijne, F. Hartmann

G. Casse, 13th VCI, Vienna 11-15 Feb 2013
Silicon detectors

With the improvements of readout electronics (in term of size and performances), silicon was more and more extensively used for Vertex and Tracker detectors at collider experiments: LEP and Tevatron!

**LEP**: DELPHI as an example
Tevatron: CDF as an example
Is the silicon detector development going forward with the same speed?

Conclusions

Carbon nanotubes promise to be very important in the next years as material with unique mechanical, optical and electrical properties.

The possible application area of CNT is extremely large: hydrogen cell, DNA manipulation, medical application, electronics, etc.

We can reasonably claim that we are at the beginning of the POST SILICON ERA.
Silicon detectors: status back there

The spectacular sensors in the LHC. Triumph of silicon technology. Many wonders in the various experimental caverns (silicon drift, silicon microstrip, hybrid pixel sensors):

To get to this quality, a large amount of R&D has been performed to face the occupancy, readout speed and radiation tolerance challenges.

.... but more difficult challenges are to be faced!
Silicon detectors in the future

The immediate challenge: HL-LHC

Possible 20 Year LHC Schedule

- LHC start-up $\sqrt{s} = 900$ GeV
- $\sqrt{s} = 7$ TeV rising to 8 TeV, $\mathcal{L} = 6 \times 10^{33}$ cm$^{-2}$s$^{-1}$, bunch spacing 50 ns
- Go to design energy and nominal luminosity
- $\sqrt{s} = 13-14$ TeV, $\mathcal{L} = 1 \times 10^{34}$ cm$^{-2}$s$^{-1}$, bunch spacing 25 ns
- Injector and LHC Phase-I upgrade to full design luminosity
- $\sqrt{s} = 14$ TeV, $\mathcal{L} = 2-3 \times 10^{34}$ cm$^{-2}$s$^{-1}$, bunch spacing 25 ns
- HL-LHC Phase-II upgrade, crab cavities, new IR, ...
- $\sqrt{s} = 14$ TeV, $\mathcal{L} = 5 \times 10^{34}$ cm$^{-2}$s$^{-1}$ (luminosity levelling) 25 ns
- \(~25\) fb$^{-1}$
- \(\geq 50\) fb$^{-1}$
- \(\geq 300\) fb$^{-1}$
- \(~3000\) fb$^{-1}$
Radiation Background

For strips 3000fb\(^{-1}\) 
\(\times 2\) implies survival required up to 
\(~1.3 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2\)

I. Dawson et al.

G. Casse, 13\(^{th}\) VCI, Vienna 11-15 Feb 2013
Serious issues: granularity and radiation damage

The increase in granularity required by the increased multiplicity will impact significantly on the services (power in, cooling, data links ....).

The increase in radiation dose compromises the ability of the sensors to operate till the end of the physics program.

V, V_2 and V_3 Formation - Particle Dependence

- 10 MeV protons
- 24 GeV/c protons
- 1 MeV neutrons

Initial distribution of vacancies in (1μm)^3 after 10^{14} particles/cm^2

Final constellation of V_2 and V_3

[Mika Huhtinen ROSE TN/2001-02]
Summary – defects with strong impact on the device properties

**Point defects**
- \( E_{i}^{BD} = E_{c} - 0.225 \) eV
- \( \sigma_{n}^{BD} = 2.3 \cdot 10^{-14} \) cm²
- \( E_{i}^{I} = E_{c} - 0.545 \) eV
  - \( \sigma_{n}^{I} = 2.3 \cdot 10^{-14} \) cm²
  - \( \sigma_{p}^{I} = 2.3 \cdot 10^{-14} \) cm²

**Cluster related centers**
- \( E_{i}^{116K} = E_{v} + 0.33 \) eV
- \( \sigma_{p}^{116K} = 4 \cdot 10^{-14} \) cm²
- \( E_{i}^{140K} = E_{v} + 0.36 \) eV
- \( \sigma_{p}^{140K} = 2.5 \cdot 10^{-15} \) cm²
- \( E_{i}^{152K} = E_{v} + 0.42 \) eV
- \( \sigma_{p}^{152K} = 2.3 \cdot 10^{-14} \) cm²
- \( E_{i}^{30K} = E_{c} - 0.1 \) eV
- \( \sigma_{n}^{30K} = 2.3 \cdot 10^{-14} \) cm²

**Reverse annealing**
- Positive charge (higher introduction after proton irradiation than after neutron irradiation)
- Leakage current (+ neg. charge)
- Reverse annealing (neg. charge)
Can silicon survive these doses?

Reverse current increase

$N_{\text{eff}}$ changes, $V_{\text{FD}}$ increase

G. Casse, 13th VCI, Vienna 11-15 Feb 2013
Operation of high resistivity Si detectors

Full depletion for optimal operation!
Radiation damage: operation scenario (LHC)

Evaluating the Evolution of $V_{\text{DEP}}$ and $I_{\text{LEAK}}$ in the SCT

In the ATLAS Inner Detector Technical Design Report (1997) $V_{\text{DEP}}$ and $I_{\text{LEAK}}$ were predicted for SCT sensors.

Assumed LHC luminosity profile:
- 3 years @ $10^{33}$ cm$^{-2}$s$^{-1}$
- 7 years @ $10^{34}$ cm$^{-2}$s$^{-1}$

($\sim 1.4 \times 10^{14}$ 1 MeV $\eta_\text{eq}$ cm$^{-2}$)

ATLAS maintenance scenarios (days@temp yr$^{-1}$):

Predictions re-evaluated with new radiation damage model and updated inputs.

Paul Dervan
RESMDD10 Florence
October 2010
For improved mip charge collection after irradiation

\( p\text{-in-}n \) versus \( n\text{-in-}p \) (or \( n\text{-in-}n \)) detectors

**n-type silicon after high fluences:**
- (type inverted)

**p-type silicon after high fluences:**
- (still p-type)

\( p^+\text{on-}n \) versus \( n^+\text{on-}p \)

__p-on-n silicon, under-depleted:__
- Charge spread – degraded resolution
- Charge loss – reduced CCE

__n-on-p silicon, under-depleted:__
- Limited loss in CCE
- Less degradation with under-depletion
- Collect electrons (faster than holes)

Comments:
- Instead of \( n\text{-on-}p \) also \( n\text{-on-}n \) devices could be used
N-side read-out helps radiation tolerance of Si detectors.

Schematic changes of Electric field after irradiation

Effect of trapping on the Charge Collection Efficiency (CCE)

Collecting electrons provide a sensitive advantage with respect to holes due to a much shorter $t_c$. P-type detectors are the most natural solution for $e$ collection on the segmented side.

$Q_{tc} \approx Q_0 \exp(-t_c/\tau_{tr})$, $1/\tau_{tr} = \beta \Phi$.
The Charge Correction Method (based on TCT) for determination of effective trapping times requires fully (over) depleted detector – so far we were limited to $10^{15}$ cm$^{-2}$.
Effect of trapping on the Charge Collection Distance

\[ Q_{tc} \approx Q_0 \exp\left(-t_c/\tau_{tr}\right), \quad 1/\tau_{tr} = \beta \Phi. \]

\[ v_{\text{sat,e}} \times \tau_{tr} = \lambda_{av} \]

\[ \beta_e = 4.2 \times 10^{-16} \text{ cm}^2/\text{ns} \quad \text{G. Kramberger et al., NIMA 476(2002), 645-651.} \]

\[ \beta_h = 6.1 \times 10^{-16} \text{ cm}^2/\text{ns} \]

\[ \lambda_{\text{Max,n}} (\Phi=1 \times 10^{14}) \approx 2400\mu\text{m} \]

\[ \lambda_{\text{Max,n}} (\Phi=1 \times 10^{16}) \approx 24\mu\text{m} \]

\[ \lambda_{\text{Max,p}} (\Phi=1 \times 10^{14}) \approx 1600\mu\text{m} \]

\[ \lambda_{\text{Max,p}} (\Phi=1 \times 10^{16}) \approx 16\mu\text{m} \]

After heavy irradiation the charge collection distance (CCD) of silicon sensors becomes much shorter than the detector thickness.

A maximum signal of just over 1500 e\textsuperscript{-} should be expected after 1\times10^{16} \text{ n}_{eq} \text{ cm}^{-2}. This is a very small signal and it would require extremely low noise electronics for being usable for tracking.
... but the measurements of the most probable value for minimum ionising particles crossing irradiated detectors show more charge than expected from the dependence on fluence of the charge trapping time constant. And even more charge than the one actually ionised by the mip!

I. Mandic (Ljubljana) at the 12th RD50 workshop.
Evidence of a charge multiplication effect: not only the whole charge is recovered, but increased by $f = 1.75$.

140 and 300 $\mu$m n-in-p Micron sensors after $5 \times 10^{15}$ $n_{eq}$ 26MeV p

Also CM in diodes (J. Lange, 15th RD50 workshop).
Effect of thickness!

Preliminary results with 100 and 50µm thick microstrip sensors are really encouraging.

MPV (mip illumination, 40MHz electronics) of sensors of various thicknesses after $2 \times 10^{16} \text{n}_{\text{eq}} \text{cm}^{-2}$.

Degradation of the collected charge (MPV) with fluence.
n-in-p Planar FZ Sensor Irradiations

Measurements show consistent results from various manufacturers

![Graph showing collected charge vs. fluence for different irradiation types and voltages.]

- **Strip Doses**
- **Pixel Doses**

- Neutrons- Micron (900 V)
- Pions- Micron (900 V)
- 26 MeV Protons- Micron (900 V)
- 24 GeV Protons-Micron (900 V)
- Neutrons-HPK ATLAS (900 V)
- 70 MeV Protons- HPK ATLAS (900 V)
- 26 MeV Protons- HPK ATLAS (900V)

**Equation:**

\[ 1.3 \times 10^{15} \text{n}_{eq} \text{ cm}^{-2} \]
Also, good news come from the annealing behaviour of the collected charge: HPK FZ n-in-p, 2E15 n cm$^{-2}$ (26MeV p irradiation)
.. And after very high (pixel) fluences: FZ n-in-p, $1 \times 10^{16}$ n cm$^{-2}$ (26MeV p irradiation)
Different detector structure: 3D Detectors
Even more radiation hard.

- Array of electrode columns passing through substrate
- Electrode spacing $\ll$ wafer thickness (e.g. 30µm:300µm)
- Benefits
  - $V_{\text{depletion}} \propto (\text{Electrode spacing})^2$
  - Collection time $\propto$ Electrode spacing
  - Reduced charge sharing
- More complicated fabrication - micromachining

Planar

3D

Proposed by S. Parker and C. Kenney of the University of Hawaii in 1995.
Double-sided 3D Production

Hole etching

- Deep Reactive Ion Etching
  - F plasma etches away base of hole
  - CF₂ coating protects sidewall
  - Limit on depth : diameter ratio
  - 250μm depth, 10μm diameter

Charge collection simulation and measurements

Test-beam Results

Pixel efficiency map: fold efficiency to 1 (±0.5) pixel

- **SCC55 CNM-3D**: un-irrad, HV=20V, Eff.=99.4%
  0 degrees
- **SCC105 FBK-3D**: un-irrad, HV=20V, Eff.=98.77%
  0 degrees
- **SCC81 CNM-3D**: n-irrad HV=160V, Eff.=97.46%
  0 degrees
- **SCC34 CNM-3D**: p-irrad, HV = 160V, Eff.=98.96%
  15 degrees

- High efficiency (>97%) after irradiation (5E15 n_eq/cm²) has been achieved
- Slim edge: 200um

S. Grinstein (IFAE) - RESMD12

UNIVERSITY OF LIVERPOOL
Technology is mature: looking for being installed in part of the ATLAS-IBL pixel detector.
HL-LHC with a large amount of silicon detectors!

In surface ....

.... and channel count (Millions)....

G. Casse, 13th VCI, Vienna 11-15 Feb 2013
A lot of other activities with Si sensors

In HEP:
HL-LHC, HE-LHC, super KEKB, super B factories, ILC, CLIC, MuC.

Other areas of Science and Technology:
Space Science, Medical Imaging, Inland Security Imaging, FEL, Syncrotron Radiation Sources, TEM, ......

Large variety of sensors and ideas:
Hybrid pixels, microstrips, drift, monolithic pixels, fast CCDs, novel connectivity, edgeless sensors ......

Describing all the silicon detector activities is quite a labour, and of coarse some important development will not be mentioned.....
A lot of other activities with Si sensors

- **Charge-Coupled Devices (CCDs), CPCCD (Column Parallel CCDs)**
- **Monolithic Active Pixels (MAPS) based on CMOS technology**
- **DEPFETs (DEpleted P channel Field Effect Transistor)**
- **SOI (Silicon on Insulator)**
- **ISIS (Image Sensor with In Situ Storage)**
- **Hybrid Active Pixel Sensors (HAPS) and 3D integration concepts**
- These basic technologies are coming in different flavours and specific technology combinations:
  - Standard CCDs as used in digital cameras are not fast enough, proposed *column parallel readout* CPCCD helps or *Short Column Charge-Coupled Device (SCCCD)*, where a CCD layer and a CMOS readout layer is *bump* bonded together.
  - Chronopixels are CMOS sensors, with the capability to store the bunch ID (time).
  - ISIS sensors combine CCD and active pixel technology, a CCD like storage cell together with CMOS readout implemented.
  - Also **Flexible Active Pixels (FAPs) integrate storage cells in the traditional MAP cells.**
  - **Fine Pixel CCDs** (FPCCDs, 5 x 5 µm²).
Requirements from other future experiments

$e^+e^-$ colliders (ILC, CLIC):
- Bunched beam structures
- Distance from beam axis: $\sim 15 \text{ mm}$
- Single point resolution: $\leq 5\mu\text{m}$
- $0.1 \chi_0$ per layer (100 $\mu\text{m}$ Si equivalent)
- Radiation tolerance $\leq 2\times10^{12} \text{n}_{\text{eq}} \text{cm}^{-2}$

SuperB factories:
- Distance from beam axis: $\sim 15 \text{ mm}$
- High granularity ($\leq 50\mu\text{m}^2$)
- Radiation tolerance $\leq 5\times10^{13} \text{n}_{\text{eq}} \text{cm}^{-2}$

Possible detector technologies (all requiring significant R&D):
- Monolithic pixels and hybrid pixels.

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**Beam Parameters**

<table>
<thead>
<tr>
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<th>CLIC</th>
<th>ILC</th>
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<tbody>
<tr>
<td>Beam energy</td>
<td>100s GeV to 3 TeV</td>
<td>100s GeV to 1 TeV</td>
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<tr>
<td>Train rate (Hz)</td>
<td>50</td>
<td>5</td>
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<tr>
<td>Train length (us)</td>
<td>0.156</td>
<td>910</td>
</tr>
<tr>
<td>Bunches per train</td>
<td>312</td>
<td>1300</td>
</tr>
<tr>
<td>Bunch separation (ns)</td>
<td>0.5</td>
<td>700</td>
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<tr>
<td>Train separation (ms)</td>
<td>20</td>
<td>200</td>
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<tr>
<td>Duty Cycle (%)</td>
<td>0.00078</td>
<td>0.45</td>
</tr>
</tbody>
</table>
CMOS detectors: MAPs

**Standard CMOS processing.** Introduced in late 1990s as R&D. Active pixel cell with an NMOS transistor. Charge collected by drift towards the charge collecting diode.

The absence of drift field is a drawback when radiation damage is involved!
But substantial improvement have been achieved and the current radiation tolerance is in line with many applications!

CMOS Monolithic Active Pixel Sensors

- Used by industry (digital camera)
- Have been modified for charged particle detection since 1999 by IPHC Strasbourg
- Foreseen for STAR, CBM, ALICE, ILC...
  => Sharing of R&D costs.

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<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>Single point res.</td>
<td>$\sim 5 , \mu m$</td>
<td>$1.5 , \mu m$</td>
<td>$1 , \mu m$</td>
<td>$4 , \mu m$</td>
</tr>
<tr>
<td>Material budget</td>
<td>$&lt; 0.3% , X_0$</td>
<td>$\sim 0.1% , X_0$</td>
<td>$\sim 0.05% , X_0$</td>
<td>$\sim 0.05% , X_0$</td>
</tr>
<tr>
<td>Rad. hard. non-io.</td>
<td>$&gt;10^{13} , n_{eq}$</td>
<td>$10^{12} , n_{eq}/cm^2$</td>
<td>$&gt;3 \cdot 10^{14} , n_{eq}$</td>
<td>$&gt;10^{13} , n_{eq}$</td>
</tr>
<tr>
<td>Rad. hard. io</td>
<td>$&gt; 3 , Mrad$</td>
<td>$200 , krad$</td>
<td>$&gt; 1 , Mrad$</td>
<td>$&gt; 500 , krad$</td>
</tr>
<tr>
<td>Time resolution</td>
<td>$&lt; 30 , \mu s$</td>
<td>$\sim 1 , ms$</td>
<td>$\sim 25 , \mu s$</td>
<td>$110 , \mu s$</td>
</tr>
</tbody>
</table>

Optimized for one parameter  Current compromise
An example of results after irradiation

MIMOSA-32 prototype
- Technology:
  - 0.18 μm.
  - epitaxial layer: 18 μm thick, High-Resistivity 1-5 kΩ.cm.
  - read-out: rolling shutter.

non-ionising irradiation (2)
- Beam test with 60 GeV Ti:
  - $T_{\text{cooled}} = 30$ °C.
  - 20x20 μm² pixels.
- $S/N \sim 32$ before irradiation $\Rightarrow S/N \sim 26$ after $1.0 \times 10^{13} n_{\text{eq}} / \text{cm}^2$.

“towards a rad-hard sensor with a read-out time $\sim 1.5 \mu$s”
- MIMOSA-32: validation of the 0.18 μm technology.
  - Complete the data analysis of past beam tests (June, July and August): spatial resolution.
  - Next beam test foreseen in November at CERN: other radiation doses, ...
  - New submission of MIMOSA-32 in 0.18 μm in July: test of amplification.
- MIMOSA-22THR: validation of the optimised rolling shutter architecture.
  - Submission December 2012.
  - 2 different chips:
    - translation of MIMOSA-22AHR (0.35 μm techno.) with end-of-column discrimination.
    - simultaneous 2-row encoding with 2 discriminators/column $\Rightarrow$ twice faster.
- SUZE-02: validation of the sparsification.
  - Submission Autumn 2012.
  - Sparsification for 2 and 4 // rows $\Rightarrow$ data flow and power reduction.
  - Submission 2013.
  - Simultaneous 4-row encoding with in-pixel discrimination $\Rightarrow$ 8 times faster.

Isabelle Ripp-Baudot,
September 19th, 2012
SuperB-SVT meeting, Pisa

Dennis Doering,
RESMDD, Florence,

G. Casse, 13th VCI, Vienna 11-15 Feb 2013
Putting a drift field in Monolithic Pixels

In SOI (Si On Insulator) technology the electronics is implanted on a thin silicon layer on top of a buried oxide (BOX): this ensures full dielectric isolation and low junction capacitance (lower power consumption, higher speed applications...). The sensor part is a thick (300µm) high resistivity fully depleted (drift field) bulk. The back-gating effect ($-V_{FD}$) can effects transistor performances. It was introduced in 2003 by ITE, Warsaw (SUCIMA, Silicon Ultra fast Cameras for electron and gamma sources in Medical Applications).

LAPIS (former OKI, Japan) provides a 0.205m Fully Depleted (FD) SOI process on high resistivity substrates (N-type CZ, 700 Ω×cm)
SOI sensors

- low dose implantation through the BOX and through the electronics
  - Suppress the back gate effect.
  - Less electric field in the BOX which may improve radiation hardness.

MIP detection: thick vs thin sensor

- Ratio of Pulse height: 0.61 ± 0.01
- Ratio of estimated sensitive thicknesses: 0.62 ± 0.05

S. Mattiazzo, RESMDD
In **HV-CMOS** a deep n-well surrounds the electronics of every pixel. The deep n-wells isolate the pixel electronics from the p-type substrate. The substrate can be reverse biased with no influence on the transistors. A depletion zone in the volume around the n-wells is formed. The n-wells collect electrons mainly by drift (a small contribution comes from diffusion from the substrate). Example AMS 350nm HV-CMOS: reverse bias voltage is 60-100 V, depleted region depth $\sim 15 \mu m$, 20 $\Omega$cm substrate resistance, E-field: 100V/15$\mu m$. 

![Diagram of drift field in Monolithic Pixels](image-url)
HC-CMOS

Many configuration possible:
Simple charge integrating pixels with pulsed reset and rolling shutter RO.
(Possible applications: ILC, transmission electron microscopy, etc.)
2) Pixels with complex CMOS-based pixel electronics that detect particle signals.
(Possible applications: CLIC, LHC, CBM, etc.)
3) Capacitively coupled pixel detectors (CCPDs) based on a pixel sensor implemented as a smart diode array.

Also other ideas for deep depletion MAPS, e.g. LePix collaboration, using deep submicron (90 nm) and medium resistivity substrates (see next talk by P. Giubilato).
Internal amplification: DEPFET

The DEPFET (depleted FET) detector is a detector with internal amplification. The n-bulk is fully depleted with a potential minimum below the strips and the structure of a field effect transistor. The electrons created by a charged particle accumulate in the potential minimum. The field configuration is such that the electrons drift underneath the gate of the transistor modifying the source drain current. An active clear is necessary to remove the electrons. (J. Kemmer and G. Lutz Nucl. Instr. and Meth. A 253 (1987), p. 365)

Change in threshold voltage shift of Clear Gate due to certain Gate voltages

DEPFET Arrays

Read-out:
Row-wise read-out (Rolling shutter mode)
20 μs frame time (100 ns per row)

1. Select row with gate
2. Sample drain current (column wise)
3. Clear internal gate
4. Sample drain current again (Correlated double sampling CDS, for faster read-out, i.e. Belle II, single sampling with stored (empty) currents)

Measurement on DEPFET equivalent test structures (CLG, 20 nm Si₃N₄)
Voltage range up to +2.5V is in flat region
→ reducing of drift voltage was possible (formerly -8 V)

Auxiliary Chips:
Switcher (switches on/off gate and clear)
DCD (Drain current digitizer)
DHP (data handling processor)
Combining technologies: ISIS, In-situ Storage Image Sensor (ILC)

- Signal charge collected under an array of photogates into a buried channel (next to pixel)
- Charge is transferred to an ‘in-pixel’ register, 20 times during the 1 ms-long train
- Readout in the 200 ms-long quiet period after the train; excellent noise performance and immunity to RF pickup during the bunch train
- 1 MHz column-parallel readout at end of ladder is sufficient, with on-chip edge logic for
  - cluster finding, centroid determination and data sparsification
- Important additional ISIS feature: easy to drive because of the low clock frequencies:
  - 20 kHz during capture, 1 MHz during readout

ISIS combines

- CCDs
- active pixel and
- CMOS edge electronics

in one device.

Chris Damerell@ESSD Wildbad Kreuth 2009 & Z Zhang@Vertex 2009 Putten
Important aspect: interconnections

Wire and bump bonding are used to interconnect the sensors to the readout electronics and to the support electronics. It represents a significant part of the cost and the complexity of a detector system. It impacts on the coverage of the tracking volume.
Important aspect: interconnections

 Significant effort is taking place for improving connectivity and system aspects. These include R&D at ASIC level (vertical integration), at detector and hybrid electronics level (multi-metals, improvement on the filling factor of sensors, thin film hybrid circuits...). The various developments can be combined for producing detector systems optimised for a given application.
Vertical integration, a dram that can come true

Two or more layers (=“tiers”) of thinned semiconductor devices interconnected by vias to form a “monolithic” circuit.

- Different layers can be made in different technology (BiCMOS, deep sub-\(\mu\) CMOS, SiGe,……).
- 3D is driven by industry:

High Power consumption
- Long Connection
- Low Density
- Poor Heat Dissipation
- RC Delays
- High Impedance
- Large Area
- Challenging Interposers
- I/O Pitch limitations

Low Power consumption
- Short Connection
- High Density
- Good Heat Dissipation
- Reduced RC Delays
- Low Impedance
- Smallest Area
- Simple Interposers
- Less I/O Pitch limitations
TSVs (Through Silicon Vias) are the enabler for vertical integration

Two different concepts:

Via last: postprocess CMOS (and other) wafers with vias
- any technology can be used (in principle)
- via area has to be reserved designing the chip
- area for vias introduces dead area in CMOS chip
- complicated process flow
- only low temperature processes can be used for via processing

Via first: Vias etched before CMOS processing
- integrated part of the CMOS process
- vias don’t add much dead area
- high temperature processes for vias possible (e.g. poly-silicon)
- limited to few producers and technologies

H-G Moser, Vertex 2012
Examples of the two approaches:
Tezzaron, 2-tier readout ASIC
AIDA (WP3) heterogeneous sensor/ASIC assemblies

In late 2008 FERMILAB organized a consortium of 15 institutions to fabricate 3D integrated circuits using the Tezzaron/Chartered process.

- Chartered uses a via middle process to add vias to 130nm CMOS process
- Tezzaron performs 3D stacking using Cu-Cu thermo compression bonding
Examples of the two approaches:
AIDA (European supported project).

- Improve performance of CMOS sensors by 3D
- NMOS transistors in CMOS sensors act as parasitic charge collection nodes
  - Restricted circuitry
  - Inefficient charge collection
- Solution:
  - Place (most) of the complex circuitry in a second tier
- 20µm pitch monolithic sensor
- Digital tier with sparsification and time stamp
- Interleaved readout (matched to ILC beam structure)
- Fabricated by Tezzaron
- Successfully tested (Threshold scan)

H-G Moser, Vertex 2012
Other aspects of interconnections: beyond bump bonding
IZM SLID Process

Metallization SLID (Solid Liquid Interdiffusion)

• Alternative to bump bonding (less process steps “low cost” (IZM)).
• Small pitch possible (<< 20 μm, depending on pick & place precision).
• Stacking possible (next bonding process does not affect previous bond).
• Wafer to wafer and chip to wafer possible.
Other aspects of interconnections: thin film hybrids

- Manage ASIC IO
  - Vias in ASIC
  - Silicon MCMD
  - 3 layer stack
- Goal is to use a thin film technology “hybrid”
  - Option-i: Silicon hybrid (Interposer)
  - Option-ii: Post processing on the silicon sensor
  - Option-iii: Replace wire-bonding with flip-chip (2nd phase)

Direct Processing of Hybrid Circuit on Silicon Sensor
(Ultimate reduction in mass and assembly complexity.)
Thin films hybrids possible construction

- **Dielectric layers: Benzocyclobutene (BCB)**
  - Deposited in layers of 3-15 µm thickness
  - Dielectric constant of 2.65
- **Conducting layers: sputtered Cu/Ti**
  - Standard thickness 1-2 µm
- **Connecting vias: etched through BCB before curing**
  - To the sensor
  - Between metal layers
- **Feature sizes**
  - Lithographic resolution: 10 µm
  - Good yield at 30 µm track width/spacing
  - Minimal via size at 15 µm thickness: 65 µm
Thin films hybrids possible construction

The first processing was done to check that thin films do not alter basic electrical parameters before .......

$C_{IS} + C_{SG} + C_{SBP}$ is a good estimate of the total capacitance

$I/V$ graphs for w14 (temperature corrected)

$1/C^2 V$ graphs for w14 at 10kHz
Thin films hybrids possible construction

.... and after irradiation ........

- Measured by two different methods
  - Bias rail to GND plane capacitance (low frequency)
  - 3 strips + edge capacitance (high frequency)

- CCE measured with a $\beta$-source vs. bias voltage
  - Using analogue SCT128A chip
- Results as expected for 500 $\mu$m thick sensor
  - Compared to non-processed 300 and 140 $\mu$m sensors

- Depends on GND plane type
- Depends on dielectric thickness
- Unaffected by irradiation
  - Small increase at $10^{15}$

G. Casse, 13th VCI, Vienna 11-15 Feb 2013
• Design based on Atlas SCT upgrade kapton hybrid
  – Hosts 20 ABCDN chips
  – Layout adjusted to MCM-D design rules
• Processed on blank silicon wafers
  – Design portable to sensor wafers
Other aspects of interconnections: multi-metals

- Small R
  - RL width ~ 11um
  - Strip width ~ 11um
  - Strip pitch ~ 40um

- Large R
  - RL width ~ 10um
  - Strip width ~ 38um
  - Strip pitch ~ 101um

Allows to produce also strixels sensors......
Breakdown protection: Guard Rings

Typical distance between sensitive area and cut edge for high voltage devices ~ 1mm. Lot of interest for reducing this inactive region.
Improving the area coverage

There are three key steps of the process:
1) Scising on front-side
2) Cleaving, which leaves the surface with low defect density
3) Surface passivation to make the sidewall resistive. N- and p-type devices require different passivation technologies.

- For n-type devices one needs a passivation with positive interface charge. SiO2 layer works well.
- For p-type material a passivation with negative interface charge is necessary. We found that Al2O3 works in this case.

H. Sadrozinski et al., RD50 Workshop, Nov. 21-23, 2011
Further improving the area coverage:

**PLANAR**

GUARD RING
Sinks surface leakage current

Microcracks, chips etc..

**PLANAR-3D** =
PLANAR DETECTOR + DOPANT DIFFUSED IN
FROM DEEP ETCHED EDGE THEN FILLED
WITH POLYSILICON

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Active edges with planar n-in-p sensors

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n-in-p pixels at VTT: active edge process with back-side implantation extended to the edges

See J. Kalliopukska talk at Pixel 2012

“Results of a Multi Project Wafer Process of Edgeless Silicon Pixel Detectors”
Incidentally, a further dream:

One of the main feature of MAPS

Can be very thin (~25 µm of silicon in total) and still fully efficient!

Problem: how to handle, interconnect and at the end built a low mass ladder with such a thin device?
Silicon detectors for good timing resolution: the NA62 GigaTracKer (GTK)

- Beam spectrometer
  - provide precise momentum, time and angular measurements on all beam tracks
  - sustain high and non-uniform rate (~1.5 MHz/mm² in the center, 0.8-1.0 GHz total)
  - preserve beam divergence for precise momentum and angular downstream measurements and limit beam hadronic interactions

- $X/X_0 \approx 0.5\%$ per station
- $\sigma(p_K)/p_K \approx 0.2\%$
- $\sigma(\theta_K) \approx 16$ $\mu$rad
- pixel size $300$ $\mu$m $\times$ $300$ $\mu$m
- $\sigma(t) \approx 150$ ps (rms) on single track
Virtuous spiral

From physics to application, and back.

An example is the Medipix: the ASIC originated from HEP needs has been further developed for X-Ray imaging.

The ASIC has evolved and a new version for application in HEP (VeloPix) is now a candidate for the LHCb-VELO upgrade.

No surprise: HEP has a typical boom and bust cycle. Keeping the R&D going between HEP ‘booms’ has high return value.
Evolution of microelectronic technologies

No roadmap, room for new ideas: monolithic sensors, 3D integration

More than Moore: Diversification
- Analog/RF
- Passives
- HV Power
- Sensors
- Actuators
- Biochips

Interacting with people and environment
- Non-digital content
- System-in-package (SiP)

Combining SoC and SiP: Higher Value Systems

Digital content
- System-on-chip (SoC)

Information Processing

Evolutionary roadmap:
- More Moore: Miniaturization

Nanoscale CMOS

Baseline CMOS: CPU, Memory, Logic
- 130nm
- 90nm
- 65nm
- 45nm
- 40nm
- 22nm
- 16nm

Beyond CMOS

around 2015

Valerio Re - RESMDD12, Firenze, October 10-12, 2012

G. Casse, 13th VCI, Vienna 11-15 Feb 2013
SUMMARY

Silicon detectors for HEP are operating with spectacular success at the current LHC!! The immediate next challenge, the HL-LHC is generating an intense R&D effort, with results that show that state of the art devices are well on track for facing the new radiation levels, speed requirements and granularity (but watch out for system aspects, powering and cooling...). ILC and SuperB’s, and other possible high intensity machines are supporting a wide range of extremely creative R&D, and material budget reduction combined with adequate radiation tolerance have been achieved or are in touching distance of many prototypes.

Special effects like Vertical Integration and interconnectivity are pursued.
SUMMARY

Besides the more glamorous development, the technology of sensor allows more sophisticated solutions (and, little by little, more affordable) for tracking at any radii (long and short strips, strixels, ...).

The role of R&D is essential, and sustaining the research also between the HEP ‘cycles’ is a high return enterprise:

"The success of particle physics experiments, such as those required for the high-luminosity LHC, relies on innovative instrumentation, state-of-the-art infrastructures and large-scale data-intensive computing. Detector R&D programmes should be supported strongly at CERN, national institutes, laboratories and universities. Infrastructure and engineering capabilities for the R&D programme and construction of large detectors, as well as infrastructures for data analysis, data preservation and distributed data-intensive computing should be maintained and further developed". (From the Draft of the Update of the European Strategy for Particle Physics).

Concerning of the future of silicon detectors, it looks bright for a number of years! Will there be a paradigm change when the size of CMOS will reach the ‘minimum feature size limit’?
HL-LHC Performance Goals

Leveled peak luminosity:
\[ L = 5 \times 10^{34} \text{ cm}^{-2} \text{ sec}^{-1} \]

Virtual peak luminosity:
\[ L = 10 \times 10^{34} \text{ cm}^{-2} \text{ sec}^{-1} \]

Integrated luminosity:
200 fb\(^{-1}\) to 300 fb\(^{-1}\) per year

Total integrated luminosity:
ca. 3000 fb\(^{-1}\)

Finally look to double the energy (HE-LHC)
16.5+16.5 TeV proton collider in the LHC tunnel
Plan for occupancy numbers based on this (see $\mu$ values below)

Plan integrated dose figures based on this

$\mu$ values going with the peak luminosity figure if achieved with 25ns beam crossing

When we calculate the dose figures which are used to specify the radiation hardness of components which can be reliably tested for post-irradiation performance (eg ASICs, silicon sensors, diamond, ...) apply this safety factor to the dose calculations in setting the radiation survival specification (Still under discussion)
Results with proton irradiated 300 μm n-in-p Micron sensors (up to $1 \times 10^{16} n_{\text{eq}} \text{ cm}^{-2}$)

Irradiated with reactor neutrons

RED: irradiated with 24GeV/c protons
Other: 26MeV protons