Monolithic pixel detectors with 0.2 μm FD-SOI pixel process technology

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on behalf of SOIPIX collaboration
High Energy Accelerator Research Organization (KEK)

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2/11-2/15 2013
@Vienna University of Technology
Electronics session
2/14 14:50-15:15
Outline

Introduction of SOI detectors
Brief review of our activities: measurement of X-rays/charged particles
- INTPIX4, INTPIX5, XRPIX1b, FPIX1, INTPIX3e
Main topics:
(1) CZn/FZn sensors study
(2) Double SOI circuit/sensor study
Summary
SOI Wafer Production

Smart cut™ by Soitec
Specify wafer resistivity: High resistivity (High R) wafer --- Sensor
Low resistivity (Low R) wafer --- CMOS

Development of the SOI monolithic pixel detector has been started since 2005 as a project of the KEK Detector Technology Project (KEK DTP)
Use Lapis Semiconductor Co Ltd. 0.2 μm FD-SOI pixel process
The features of SOI monolithic pixel detector

- No mechanical bump bonding. Fabricated with semiconductor process only → high reliability and low cost
- Fully depleted (thick & thin) sensing region with low sense node capacitance (~10fF@17μm pixel) → high sensor gain
- Wide temperature range (4-570K)
- Low single event cross section
- Technology based on industry standards
## Process

| Process          | 0.2 µm Low-Leakage Fully-Depleted (FD) SOI CMOS  
| (Lapis Semiconductor Co. Ltd.) | 1 Poly, 5 Metal layers (MIM Capacitor and DMOS option)  
|                  | → Total thickness above top Si (SOI layer) ~ 9 µm  
|                  | Core (I/O) voltage : 1.8 (3.3) V  
| SOI wafer (200 mm φ =8 inch) | Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick  
|                  | Buried Oxide: 200 nm thick  
|                  | Handle wafer thickness: 725 µm → thinned up to 300 µm (Lapis)  
|                  | or commercial process → ~50 µm (then, backside process…)  
|                  | Handle wafer: CZn ~ 700 Ω-cm (Default)  
|                  | FZn > 3 k Ω-cm (2009-)  
|                  | FZp ~ 25 kΩ-cm (2010-)  
|                  | Double SOI (CZn) (2012-)  
| Backside process | Mechanical Grind → Chemical Etching → Back side Implant → Laser Annealing → Al plating  


Multi Project Wafer (MPW) run

- KEK organizes MPW runs twice a year
- Mask is shared to reduce cost of a design
- Including pixel detector chip and SOI-CMOS circuit chip
- University & institution
  KEK, FNAL, LBNL, AIST, CNS, Kyoto Univ., Tohoku Univ., Univ. of Tsukuba, RIKEN-XFEL, JAXA, Krakow, Hawaii, IHEP, and more…

Supporting companies
Lapis Semiconductor Co. Ltd.,
Lapis Semiconductor Miyagi Co. Ltd.,
T-Micro Co. Ltd., Rigaku Co. Ltd
## Development history: SOI Integration type pixel detector

KEK is working on integration-type and counting-type / digital (binary) pixel detectors

<table>
<thead>
<tr>
<th>Year</th>
<th>Process</th>
<th>Pixel size</th>
<th>Technology</th>
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<tbody>
<tr>
<td>FY05</td>
<td>KEK MPW</td>
<td>0.15 µm</td>
<td>SOI Integration type</td>
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<td>FY06</td>
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<td>FY08</td>
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* Only integration-type detectors are shown

Pixel size

20 µm
Measurement of X-rays

X-ray imaging (INTPIX4), 3 images are combined

Compton electron detection (INTPIX4)

Dried fish

X-ray spectrum (XRPIX1b)

Kyoto Univ. & KEK

* CZn sensor

For astronomical mission

Sensor gain 6μV/e-

188 eV (FWHM)

noise=18 e- rms
FPIX1 – The smallest pixel in KEK sensors

Pixel size 8µm, 512x512, effective area 4.096 x 4.096 mm
No STORE, no storage capacitor

JIMA RT RC-05 (1µm-Au absorber)
3 slits/group, 2x2mm area, 3-50µm
2000 event accumulation
Cr target 30kV-60mA(1.8kW MAX)
FPIX1 (CZn-260um)
Vdet=70V (partially depleted)
Temperature 15deg.

8µm lines can be seen

X-ray image

CTF>20%
Measurement of charged particles

α particles from Am-241

INTPIX5 with high-gain mode

Pixel size 12μm

Carbon beam

Measured at Research Center for Charged Particle Therapy, NIRS, Chiba, Japan
INTPIX5 low-gain mode, 64x64 pixels are used

* CZn sensor
INTPIX3e – general purpose integration-type pixel detector

It was used for high-energy particle beam test in 2011

CERN SPS NORTH H4-H6
π+ 55%, p 39%, K 5%
120 GeV

4 layers of INTPIX3e
(pixel size = 16 x 16 μm)

From master thesis by Katsurayama
(Tohoku Univ.)
260μm-thick CZn INTPIX3e

An example of residual distribution
Residual 1-4 layers is 2-4μm in σ

From master thesis by Shinsho
(Univ. of Tsukuba)

MIP spectrum
The chip was thinned by Nihon Exceed
CZn-INTPIX3e
50μm-thick
S/N ~ 15
Main topics (1)

**CZn/FZn sensor study**

INTPIX5 (FY11)
- 1408 x 896 pixels
- Pixel size 12 x 12 μm
- Effective area: 16.896 x 10.752 mm

No breakdown up to 400V
Leakage current is higher for CZn-INTPIX5

Leakage current of FZn sensor became lower thanks to Lapis back processing

![Pixel layout](image195x66.png)

![Pixel circuit](image74x400.png)
Spatial resolution study @ KEK-PF

KEK-PF BL-14B monochromatic X-ray E=16.1 keV
Use NTT-AT test chart
Front and back illumination
CZn 260μm-thick INTPIX5 (100V, partial depletion)
FZn 500μm-thick INTPIX5 (170V, full depletion)
Spatial resolution of CZn & FZn INTPIX5

KEK-PF BL14A monochromatic X-ray Energy ~ 16 keV

16 μm slits can be seen for all the images.
Main topics (2)  

Double SOI circuit/sensor study

Current issues

- The back gate effect --- BPW/BNW process is a solution
- Charge trap at BOX --- TID effect
- Cross talk (Under testing. I don’t show any results today)

A suggestion

Utilization of Double SOI (D-SOI) wafer

Y. Arai et al., NIM A Vol. 636, Issue 1, Supplement, 21 April 2011, Pages S31–S36
Double SOI Wafer Production

The parameters are not optimized. The 1st TEG/sensor chips were received on Oct. 2012.
Double SOI sensor test status (2012.10 ~)

Issue 1 Lower breakdown voltage

Double SOI INTPIX3g bare chip I-V Curve (T=23deg)

- Breakdown
- Remove SOI2 between them
- Improvement
- The 2\textsuperscript{nd} process (MX1501, MX1542)

Issue 2 charge collection inefficiency

Charge collection efficiency reduction between pixels → BNW between pixels (INTPIX3g, PIXOR), remove DSOI between pixels, or use p-wafer

Fixed (-2V)

Pixel(n) BNW Pixel(n+1) BPW +45V(Vdet)

X-ray image (0.4x0.4 mm beam spot)
12keV monochromatic X-ray @KEK-PF BL 14A

The 2\textsuperscript{nd} test chip will be received in FY2013
Co-60 gamma-ray TID test @ JAERI/Takasaki

Double SOI Test Element Group (TEG) chip (AIST & KEK)
During irradiation, all the contacts are set to GND.

```
Vth[V]
0.5
0
-0.5
-1
-1.5
```

NMOS is ON at more than ~ 400 krad with Vsoi2=0V
NMOS works at 10 Mrad with Vsoi2=-2V
PMOS works at 10 Mrad

Preliminary

Univ. of Tsukuba
Hara, Honda, Ishibashi
X-ray irradiation test

Experimental setup

X-ray irradiation
Every 10/20/60 sec

Single SOI:
10 sec x 6 times
Double SOI:
10 sec x 20 times
20 sec x 5 times
60 sec x 10 times

Measurement
beam-on/off ADC output
in a pixel

Intensity
Measured by 300um-thick
Silicon PIN PD
@30kV-60mA
Current 885nA (Error 3%)

In double SOI, \( V(\text{middle SOI}) = -2V \)
Preliminary results of high dose X-ray irradiation test

Single SOI CZn (HR1, 3JA) Total dose 54 krad
Signals disappeared

D-SOI CZn (6JA) Total dose 810 krad
Signals still appear (Dynamic range changed narrower)

Caution!: INTPIX3g design has problem and has very low dynamic range!

* Middle SOI voltage = -2V
Preliminary results of radiation tolerance study

Signals disappeared!

Dynamic range became narrower, but signals still appeared.

Reference channel = (50,50)
Preliminary results of radiation tolerance study

Double SOI sensor worked after 800 krad irradiation. Dynamic range (eventually transistor parameters) was changed.

One solution: reduce reset voltage because the SF transistor VTH was shifted.
Summary

SOI monolithic detector has many attractive features.
MPW runs twice a year
Process was improved and several wafers are available.
Integration type pixel detectors
- High gain with smaller pixel size w/o CSA
- Good energy resolution
- Good spatial resolution (CZn/FZn)
- Charged particles were detected by thin CZn sensors
- Thick FZn wafer is suit for hard-X-ray detection
Current issues
- The back-gate effect \(\rightarrow\) BPW/BNW process, double SOI
- Crosstalk \(\rightarrow\) double SOI, under testing
- Radiation hardness
  \(\rightarrow\) Transistors and sensors on double SOI wafer
  had radiation tolerance with middle SOI potential control.

FY2013
Test of several types of wafers
Optimization of pixel layout with double SOI
Application experiment
SOIPIX Collaboration

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Lapis Semiconductor Miyagi Co. Ltd.: H. Kasai

Thank you for your attention!
Supplements
Back gate effect is suppressed by the BPW.
Double SOI effectiveness study

"SOI2" = Floating or 0V

Middle SOI layer blocks the back-gate effect.
We expect the middle SOI blocks sensor cross-talk.

AIST double SOI TEG
NMOS #1 Tr IdVg, Vds=1.8V

Middle SOI layer blocks the back-gate effect.
We expect the middle SOI blocks sensor cross-talk.
IdVgs curve with dose

Honda (Univ. of Tsukuba)

Vsoi2=0[V]  Vsoi2=-1[V]  Vsoi2=-2[V]

N33_IONVT_ST2_L0.4_w5