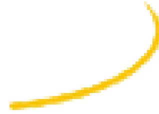

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Monolithic pixel detectors with 0.2 um FD-SOI pixel process technology

Thursday, 14 February 2013 14:50 (20 minutes)

Truly monolithic pixel detectors were fabricated with 0.2 um SOI pixel process technology by collaborating with LAPIS Semiconductor Co., Ltd. for particle tracking experiment, X-ray imaging and medical application. CMOS circuits were fabricated on a thin SOI layer and connected to diodes formed on the silicon handle wafer through the buried oxide layer. We can choose the handle wafer and therefore high-resistivity silicons are also available. When Float Zone (FZ-) SOI wafers in which the thickness is about 500 um are used as the handle wafer, it can be fully-depleted with back-bias voltages of about 100 V. Double SOI (D-SOI) wafers fabricated from Czochralski(CZ)-SOI wafers were newly obtained and successfully processed in 2012. The top SOI layers are used as electric circuits and the middle SOI layers used as a shield layer against the back-gating effect, the cross-talk between sensors and CMOS circuits, and the total ionizing dose (TID) effect. KEK organizes Multi Project Wafer (MPW) runs in every year, in which many designs provided by Universities and institutions over the world are put together. In 2012, we developed several types of pixel detectors and some transistor test chips. Characteristics of the transistors and sensors fabricated with D-SOI were compared with that with single SOI. In presentation, the up-to-date test results will be shown.

quote your primary experiment

SOI

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