The first fully functional 3D CMOS chip with Deep N-well active pixel sensors for the ILC vertex detector

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OUTLINE

- Vertical Integration (3D) CMOS Technologies
  - Why are they so attractive for HEP applications?
  - Tezzaron/GlobalFoundries 3D process
- DNW MAPS in 3D technology
  - Design features
  - Characterization results
- Conclusions and future plans

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Vertex Detectors in future HEP Experiments

✓ The experiments at the future high luminosity colliders need fast, highly granular (=> small pixel pitch), low material budget (=> low mass cooling, thin silicon wafers) particle trackers

✓ Significant progress has been made in the last decade to address these issues by integrating sensors and front-end electronics within the pixel cell

✓ Monolithic Active Pixel Sensors (MAPS) are a promising solution for low-mass, high granularity pixel trackers. After several years of R&D, MAPS are reaching a good maturity level, but there is still room for substantial improvements

✓ SOI Pixel Sensors

✓ 3D circuits offer improved performance over other approaches for HEP

✓ The move to 3D is being driven entirely by industry needs (reduce R, L, C for higher speed, provide increased functionality, reduce cross-talk, ...)

✓ A 3D chip (different from a 3D detector) is comprised of 2 or more layers of semiconductor devices which have been thinned, bonded and interconnected to form a monolithic circuit

✓ Processing of each layer can be optimized
Several groups from US and Europe have been involved in the first 3D MPW for HEP (pixel and strip readout chips for ATLAS, CMS, B-factory, ILC) and photon science applications (X-ray imaging).

Single set of masks used for both tiers to save money
- identical wafers produced by Chartered (now GlobalFoundries) and face-to-face bonded by Tezzaron
- backside metallization by Tezzaron

Top layer flipped over
Bottom layer
Tezzaron uses a “via middle” approach for the fabrication of 3D chip

Step 1: On all wafer to be stacked complete transistor fabrication, form TSV, passivation and fill TSV at same time connections are made to transistors

Step 2: Complete back end of line (BEOL) process by adding Al metal layers and top Cu metal (0.7um)

Step 3: bond wafer 2 to wafer 1 (Cu-Cu thermo-compression bond)

Step 4: thin the wafer 2 to about 12um to expose TSV. Add Cu to back of wafer 2 to bond wafer 2 to wafer 3 OR add metallization on back of wafer 2 for bump bonding or wire bonding

Step 5: stack wafer 3, thin wafer 3 to expose TSV, add final passivation and metal for bond pads.
A novel approach, based on triple well structures, has been proposed to enable the design of MAPS sensors (deep N-well, or DNW MAPS) with capabilities for pixel level sparsification and time stamping.

In triple-well CMOS processes a deep N-well is used to isolate N-channel MOSFETs from substrate noise.

These features were exploited in the development of deep N-well (DNW) MAPS devices.

DNW is used to collect the charge released in the substrate.

A classical readout channel for capacitive detectors is used for Q-V conversion → gain decoupled from electrode capacitance.

NMOS devices of the analog section are built in the deep N-well.

Using a large detector area, PMOS devices may be included in the front-end design → charge collection inefficiency depending on the ratio of the DNW area to the area of all the N-wells (deep and standard).
What can be gained from going 3D

- Sensor and analog front-end can be integrated in a different layer from the digital blocks
- Less PMOS in the sensor layer \(\rightarrow\) improved collection efficiency
- More room for both analog and digital power and signal routing

Tier 1: collecting electrode (deep N-well/P-substrate junction) and analog front-end and discriminator

Tier 2: digital front-end (2 latches for hit storage, pixel-level digital blocks for sparsification, 2 time stamp registers, kill mask) and digital back-end (X and Y registers, time stamp line drivers, serializer)

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Analog front-end and discriminator

Only preamplifier PMOS devices are kept in the analog layer (TIER 1)

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**Digital front-end**

The digital tier includes a number of digital blocks (double hit detection and double 5-bit time stamp, data sparsification and pixel masking)

- **Chip operation tailored on the ILC beam structure**
  - detection phase, corresponding to the bunch train interval
  - readout phase, corresponding to the intertrain interval
  - During the detection phase, the SR FF (FFSRK) is set, and the relevant time stamp register gets frozen, when the pixel is hit for the first time
  - Upon a second hit, the D FF (FFDR) is set and the relevant time stamp register gets frozen

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Token passing readout architecture
SDR1 prototype elementary cell: bottom and top tiers

DNW sensor and preamplifier NMOS

Competitive N-well

Discriminator NMOS

Inter-tier connections

Inter-tier connections

Discriminator PMOS

Digital front-end

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Moving most of the PMOS transistors to the top (digital) tier may significantly improve the detector collection efficiency.

The DNW covers about 35% of the cell area in the SDR0 chip, more than 50% in its 3D release.

SDR1 cell (3D)
(bottom/sensor tier)

SDR0 cell (2D)
Prototype chip layouts

240x256 DNW MAPS for ILC (20 μm pitch)

8x8 and 16x16 DNW MAPS for ILC (20 μm pitch)

32x8 DNW MAPS matrix for SuperB (40 μm pitch)

5 test structures of DNW MAPS for ILC (3x3, single channels with different C₀, 20 μm pitch)

Test structures of DNW MAPS for SuperB (2 3x3 one with ELT input device, 40 μm pitch)
Prototype chip layouts

1st wafer

metal + oxide + 2nd wafer substrate

5.5 mm

6.3 mm
SDR1 experimental results

Tests on the analog section with injection of external calibration signals (3x3 pixel matrix)

No crosstalk between pixels, no correlated noise

Preamplifier response of the 3x3 matrix central pixel to an external calibration signal

Pixel output signal vs injected charge

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SDR1 characterization with laser scan

Laser measurements for characterization of gain uniformity, identification of dead pixels, ...

- collected charge (expressed as percentage of the peak value) as a function of the laser beam position
- obtained by retro-illumination with an infrared laser (1060 nm wavelength)
- 2.5 um step in X and Y
- the layout of the Deep N-well layers and competitive N-wells has been superimposed (exact position unknown)
- intensity profile of the laser beam has a Gaussian shape with $\sigma_{xy} \approx 1.3$ um
- measurement results show the relative charge collection versus position (the amount of charge that is deposited has not been calibrated) and the impact of the standard N-wells on the charge collection
SDR1 characterization with laser scan

- Peak amplitude of pixel 13, 23, 33 measured at the same time for each laser spot position.
- Adjacent pixels collect slightly less than 50% of the charge when the laser spot is above the competitive N-well.
- 2 µm step in X.
Digital readout test

Signals from an 8x8 matrix at 50 MHz readout clock

Vth < PA output DC level -> all the pixels are read out

Cell clock

N_pix x N_bit x T_clk 64 x 24 x 20 ns \approx 30.7 \text{ us}
Digital readout test

Signals from an 8x8 matrix (details of the first and last read out cells, $f_{ck}=5\text{ MHz}$)

$V_{th} < \text{PA output DC level}$ -> all the pixels are read out
Conclusions and future plans

A DNW monolithic pixel sensor for applications to the ILC VTX detector has been successfully fabricated in a 130 nm 3D CMOS technology

- analog and digital front-end works fine
- readout architecture tested up to 50MHz on small matrices
- characterization of the charge collection properties by means of laser scans → limited charge spreading among neighbor pixels

Characterization activity is still in progress

- Tests of SDR1 with radioactive sources are needed
- Test of the readout architecture on large (240x256) matrix
- Thorough evaluation of the cross-talk phenomena between digital and sensor layers
- Conclude the radiation hardness evaluation
- Test beam of the 240x256 matrix

The design of new 3D DNW MAPS and of a 3D front-end chip for hybrid pixels is in the final stage