A bump-bondable DSSC Pixel Readout ASIC for DEPFET Sensor Matrices

J. Soldat[1], P. Fischer[1], L. Bombelli[2], D. Comotti[3], F. Erdinger[1], S. Facchinetti[2], K. Hansen[4], P. Kalavakuru[4], M. Kirchgessner[1], M. Manghisoni[3], M. Porro[5], E. Quartieri[3], C. Reckleben[4]

[1]Heidelberg University, Germany; [2]Politecnico di Milano, Italy; [3]Univ. di Bergamo, Italy; [4]DESY, Germany; [5]MPI Munich, Germany

Introduction

The aim of the DSSC (DEPFET Sensor with Signal Compression) development project is to deliver a high speed focal plane detector system for the new European XFEL in Hamburg. The XFEL will deliver a bunch train rate of 10 Hz, each train containing 2880 pulses at a frequency of 4.5 MHz.

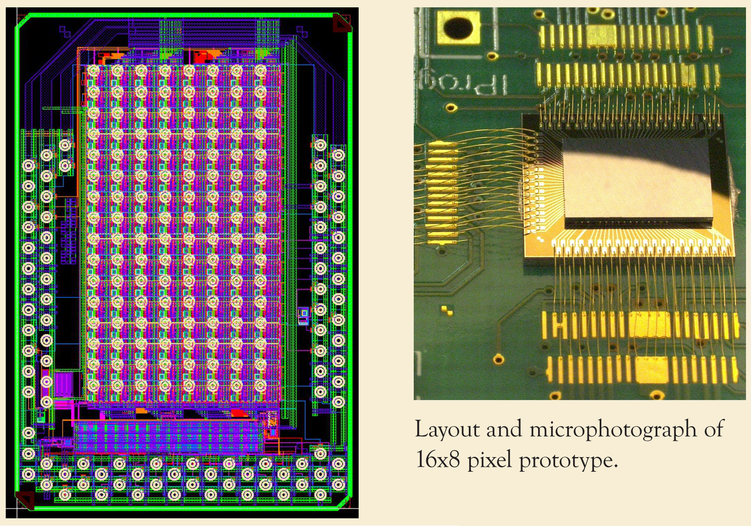
Key requirements for the DSSC system:

- Detection of single low energy X-rays (>0.5 keV)
- Detection of up to 10^4 X-rays with resolution better than Poisson limit
- Variable bunch rate 4.5 MHz ... 1 MHz
- Processing of >500 subsequent pulses in each burst
- Data reatout in 99.4 ms burst gaps

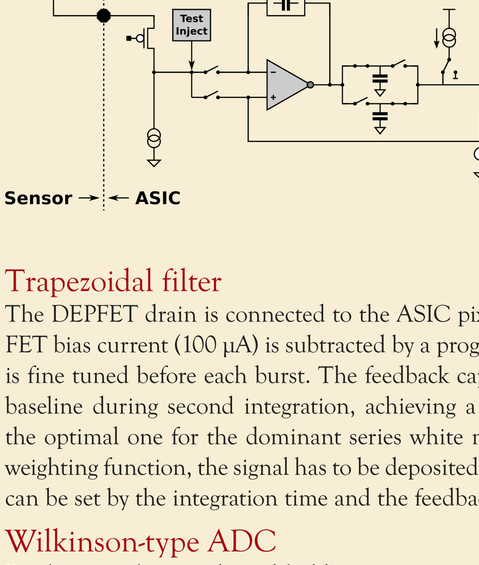
ASIC Architecture

The ASIC has been designed in IBM 130nm technology. Each (final) ASIC contains a digital block for control and readout of the 64x64 pixel matrix, organized in 64 pixel columns. The power and timestamps for the ADCs are distributed along these columns.

The prototype presented here is a 16x8 pixel matrix. Power and timestamps are routed in a snake pattern to mimic 2 final columns. One column is using a global gray code counter approach, while the second column is used for testing a new in-pixel counting approach.



Layout and microphotograph of 16x8 pixel prototype.



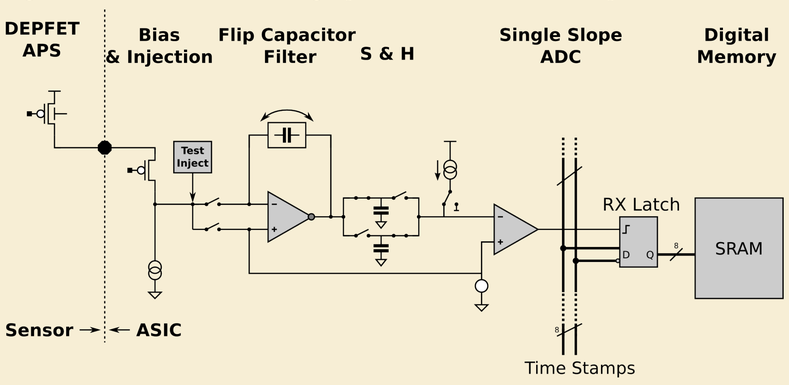
The prototype already has a close-to-final ASIC control interface with very few digital control lines necessary for operation. After one redesign, the on-chip global digital control block is working as expected.

Pixel Architecture

Each ASIC pixel reads out one DEPFET pixel using:

- Optimized analog shaping
- Immediate digitization by 8-bit ADC
- In-pixel SRAM

The aim is to set the gain and offset of the filter and ADC, such that in the linear region of the DEPFET, each single photon is attributed to a separate ADC bin.



Trapezoidal filter

The DEPFET drain is connected to the ASIC pixel by bump bonding. The DEPFET bias current (100 µA) is subtracted by a programmable current source, which is fine tuned before each burst. The feedback capacitor is flipped to subtract the baseline during second integration, achieving a trapezoidal weighting function, the optimal one for the dominant series white noise. During the flat top of the weighting function, the signal has to be deposited in the DEPFET. The filter's gain can be set by the integration time and the feedback capacitor's size.

Wilkinson-type ADC

By charging the sample and hold capacitor up to the comparator's reference voltage, a voltage-to-time conversion is achieved. The ADC's gain can be set by the trimmable current source, the offset can be set with a delay between the ramp start and the counter start. The global time stamps with a granularity of 719 ps are distributed along 13mm-long Coplanar Waveguides for a 64 pixel column.

Digital memory

The in-pixel static memory is using IBM Dense SRAM cells violating normal design rules and is able to save 640 words (9 bit) in just 229x64 µm² with only 15% of the space needed for control.

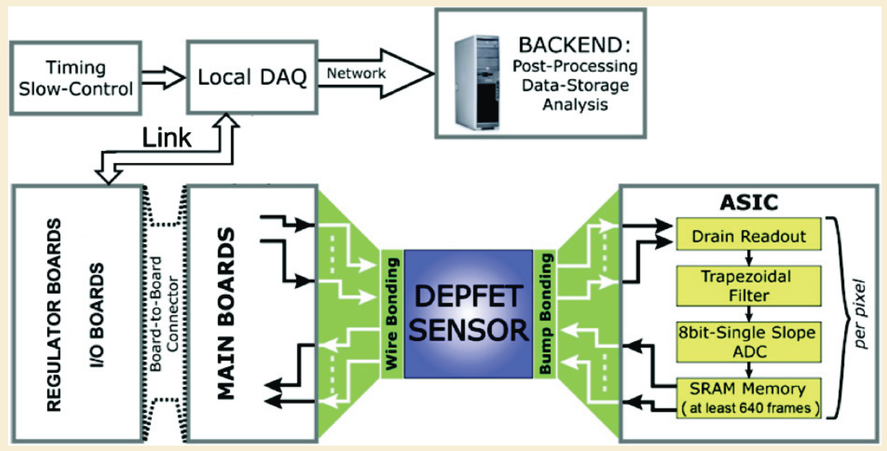
Other

Not shown in the schematic are decoupling capacitors with fault detection logic, static control registers, and the circuit necessary to generate precise and temperature-compensated currents and reference voltages.

DSSC Detector System

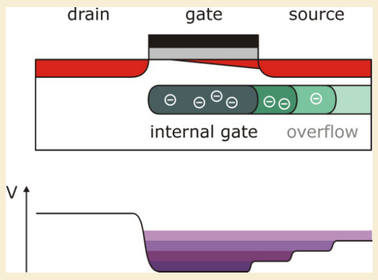
Detector Architecture

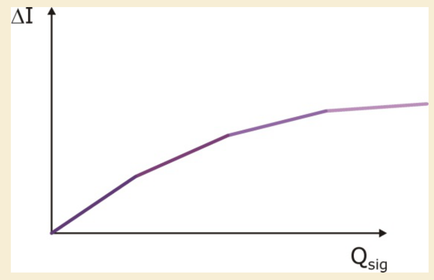
- Hybrid pixel detector approach to achieve full parallel processing
- Based on a pixelated silicon sensor with a DEPFET as a central amplifier structure
- 1024x1024 hexagonal pixels of 229x204 µm² pitch
- Low noise (<50 e^-) due to DEPFET properties
- Signal compression on sensor level, dynamic range of >10^4 photons
- Digital in-pixel storage
- Veto mechanism for discarding uninteresting events
- Power cycling of the sensor and analog frontend, exploiting the low XFEL duty cycle



DEPFET sensor

- Deep potential minimum for electrons under the external gate, causing an effect on FET current
- DSSC-type DEPFET has an additional overflow region for electrons underneath the source
- Signal charges at high levels are also stored under source, therefore less/no effect on FET current



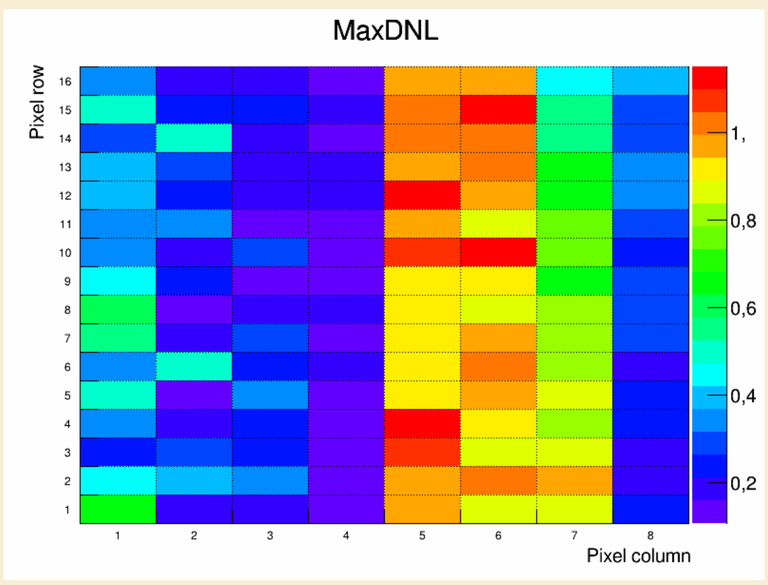


Chip Testing

Each ASIC building block has been characterized in great detail and issues in the first versions have been addressed.

ADC

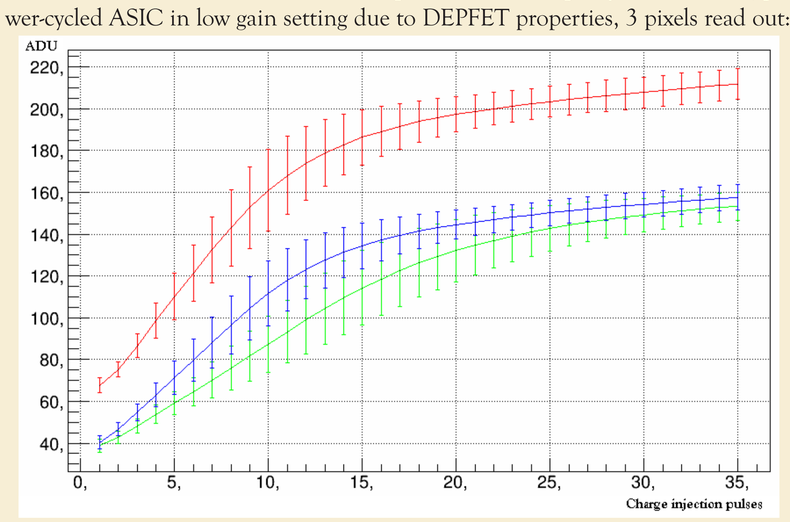
The ADC's bin width variations are expressed as differential nonlinearity. The map below shows the prototype's maximum DNL as a function of pixel position. The global counting ADCs (right) show a DNL of less than 0.4 LSB in the first column, while the in-pixel counting version is below 0.2 LSB. Both ADC types' performance degrade due to bends and layer changes of the time stamp/clock transmission lines.



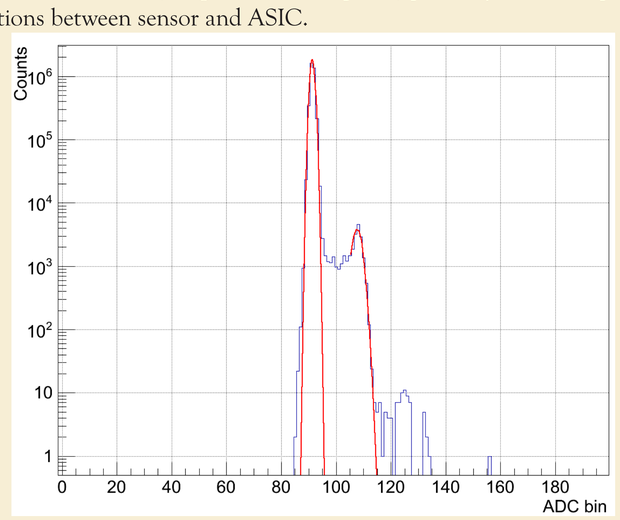
Complete readout chain

The functionality of the complete signal processing chain has been verified by measurements with DEPFET prototypes.

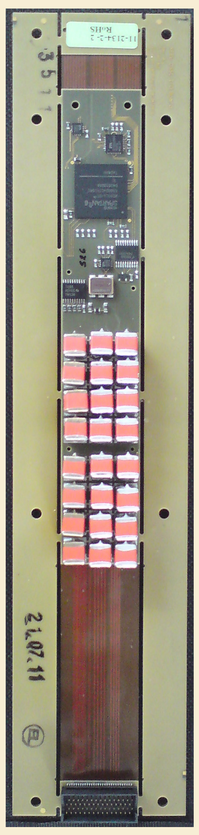
Scan of the nonlinear characteristic using an internal charge injection contact, power-cycled ASIC in low gain setting due to DEPFET properties, 3 pixels read out:

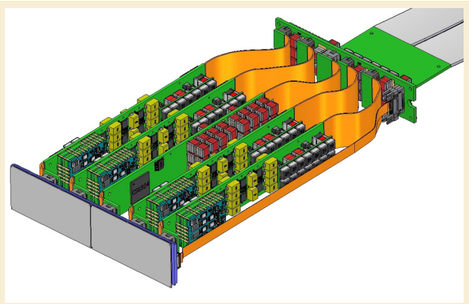


Measurements of an earlier matrix and DEPFET prototype with a ^{55}Fe source showed a noise of 78 e-, larger than anticipated, probably due to imperfect wire connections between sensor and ASIC.



System Control and Readout





Focal plane hardware

Two types of PCBs are placed perpendicular to the focal plane: the I/O Board and the Power Regulator Board. Prototypes are already available and have been tested successfully with ASIC prototypes.

The I/O Board (left) is an FPGA board designed for controlling and reading data from 4 ASICs. Slow Control is done via JTAG, data taking and readout is done by control telegrams. The telegrams order the ASIC's master FSM to initiate a burst synchronous to the XFEL machine, discard an event during a burst or start sending the captured data. The Veto telegram for a specific event is sent with a fixed (but programmable) latency, simplifying the necessary logic to simple shift registers. Data readout from the focal plane is done in the burst gaps on a single 350 MHz link per ASIC. Each I/O Board collects the data from 4 64x64 pixel ASICs.

The Power Regulator Board has been designed to create the analog system's 10 Hz power cycling with 2.9 A peak currents and precise 60 ns-long clear pulses for the DEPFETs.

Connection to XFEL DAQ system

The system's connection to the XFEL is maintained by the Patch Panel Transceiver, a Kintex-7 FPGA-based module, which accepts XFEL clock and control information and converts it to the appropriate DSSC commands and timings. It also concentrates the data read out from the focal plane I/O Boards and sends it to the XFEL data acquisition system on a QSFP+ optical interface.

Outlook: Large 64x64 matrix chip

The full-size matrix ASIC will have a size of 14x15 mm² and a power consumption of 1.5 mW per pixel. The layout outlook below gives an idea of the proportions of the pixel matrix and the global control block (bottom). The first production run is scheduled for spring 2013.