LePix – High Ω monolithic pixels

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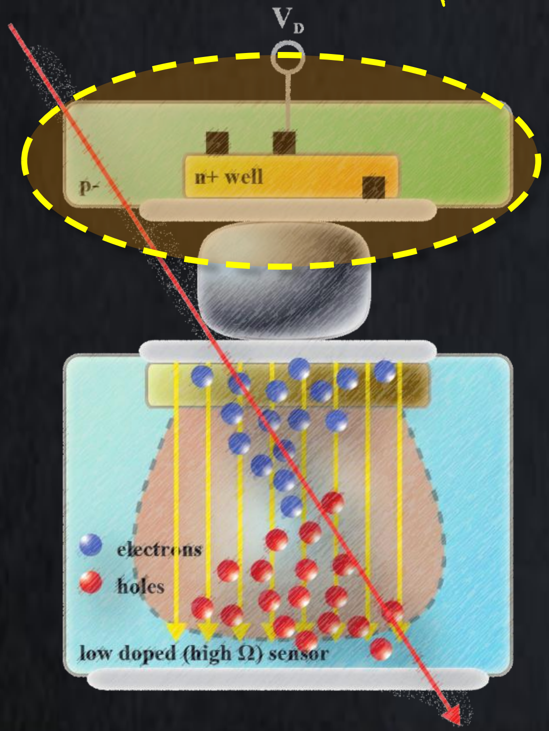
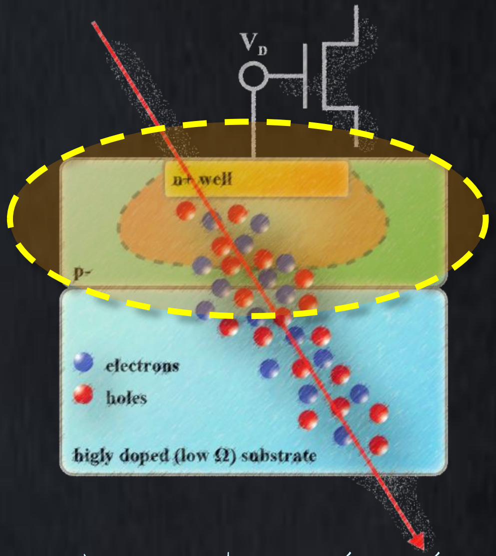
Hybrid versus monolithic approach

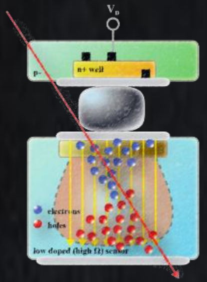
Both uses CMOS for front-end and readout



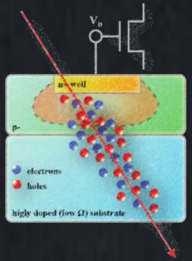


Integrate the readout circuitry – or at least the front end – together with the detector in one piece of silicon

Hybrid and monolithic approach: pro and cons

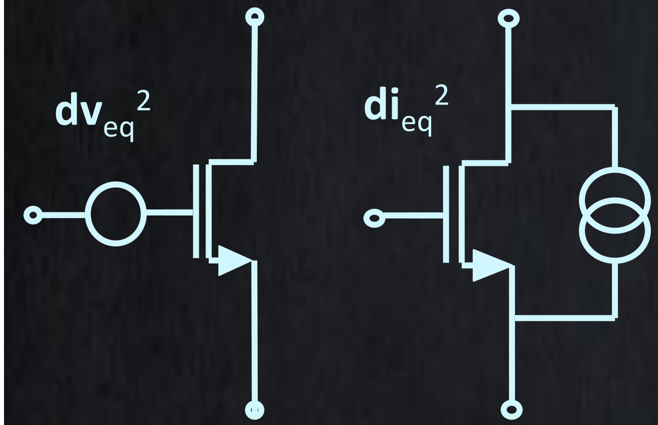


- Established, proven, effective technology
- Unique possibility to use the **best sensor** depending on the radiation to track
- Plenty of room for extremely advanced in-pixel electronic
- **Cost, complexity, mid power consumption, material budget**
- Producing **small (< 20 um) pixels** still a challenge for bump bonding



- **Young** technology
- **Sensing material** limited to substrate silicon
- **Not so much room in pixel** for advanced signal processing
- **Radiation tolerance** could still be an issue for high doses applications
- **Cost effective**, simple, low power and low material budget
- **High resolution** (pixels < 5μm)

Reminder: noise sources in a single MOS stage



$$di_{eq} = g_m \cdot dv_{eq}$$

Noise, Weak inversion

flicker ($^1/_f$)

$$dv_{eq}^{\ 2} = \left(\frac{K_F}{WLC_{ox}^{\ 2} f^{\alpha}} + \frac{4kT\gamma}{g_m} \right) df \qquad g_m \sim I$$

thermal

Noise, strong inversion

$$dv_{eq}^{\ 2} = \left(\frac{K_F}{WLC_{ox}^{\ 2} f^{\alpha}} + \frac{2kT\gamma}{g_m} \right) df \qquad g_m \sim \sqrt{I}$$

Transconductance g_m is related to power consumption:

First pixel stage: higher current (power)-> better performances and lower noise

Power depends on Q/C

signal (S), noise (N); $2 \le m \le 4$

$$\frac{S}{N} \sim \frac{Q/_C}{\sqrt{g_m}} \sim \frac{Q}{C}\sqrt[m]{I} \sim \frac{Q}{C}\sqrt[m]{P} \Rightarrow P \sim \left(\frac{S/_N}{Q/_C}\right)^m$$

$2 \le m \le 4$

Assuming $\frac{S}{N} = cost \Rightarrow P \sim \left(\frac{Q}{C}\right)^{-m}$

$\frac{S}{N}$: Good detection Parameter, say 25

P: Power to meet S/N goal

Analog power is very strongly dependent on Q/C => Wants low C

Power depends on Q/C visualized!

Assuming input noise $v_{eq} = 0.16\ mV$

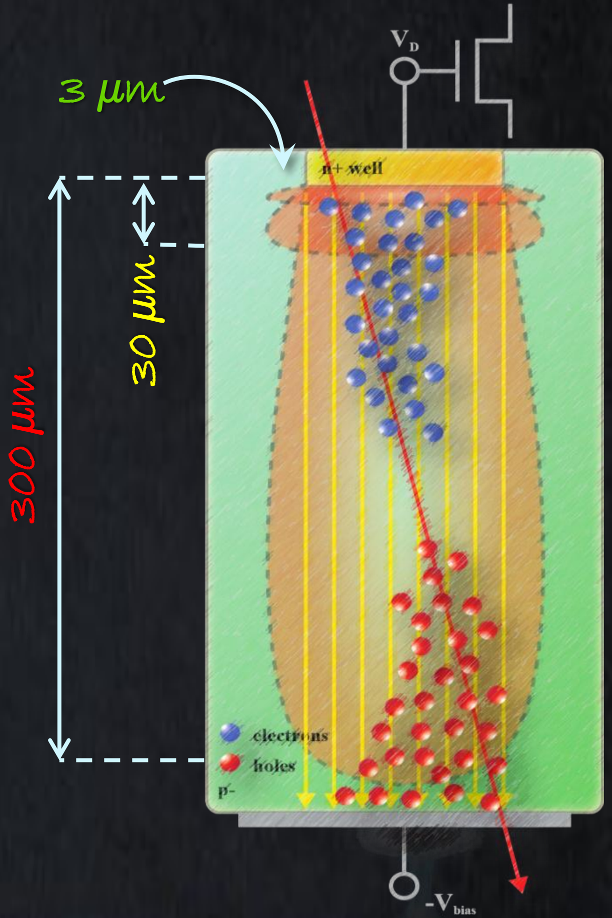
(Transistor noise at 40 MHz BW for 1 µA
(1 µA/100x100 µm pixel = 10 mW/cm²))

$$\Downarrow$$

$$\frac{S}{N} \geq 25 \rightarrow \frac{Q}{C} \geq 4\ mV$$

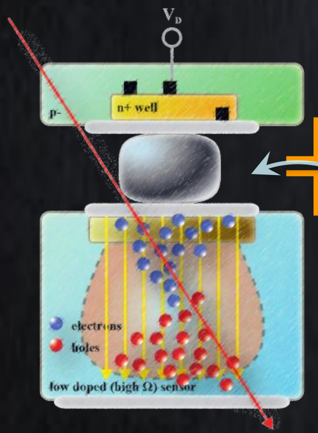
$$\Downarrow$$

25000 e⁻		2500 e⁻		250 e⁻
$\frac{4\ fC}{1\ pF}$	$\equiv$	$\frac{0.4\ fC}{100\ fF}$	$\equiv$	$\frac{0.04\ fC}{10\ fF}$
300 µm		30 µm		3 µm



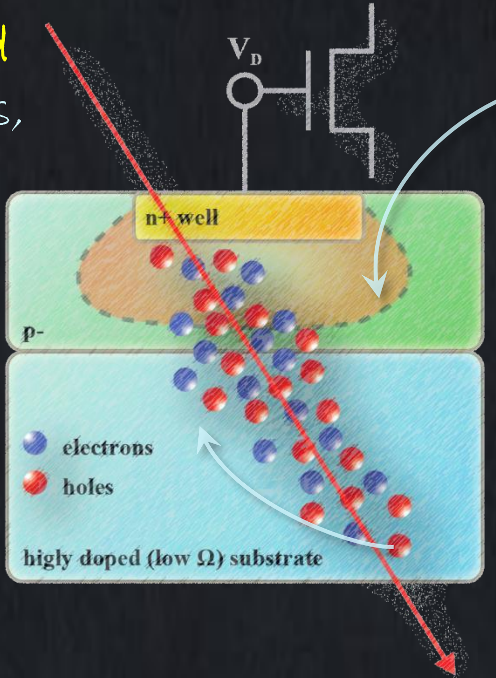
Monolithic approach – standard M.A.P.S.

Usually a **standard** (opto) CMOS process, **low Ω** substrate



Fast, deep collection volume

<u>capacitance</u>, **cost, complexity**



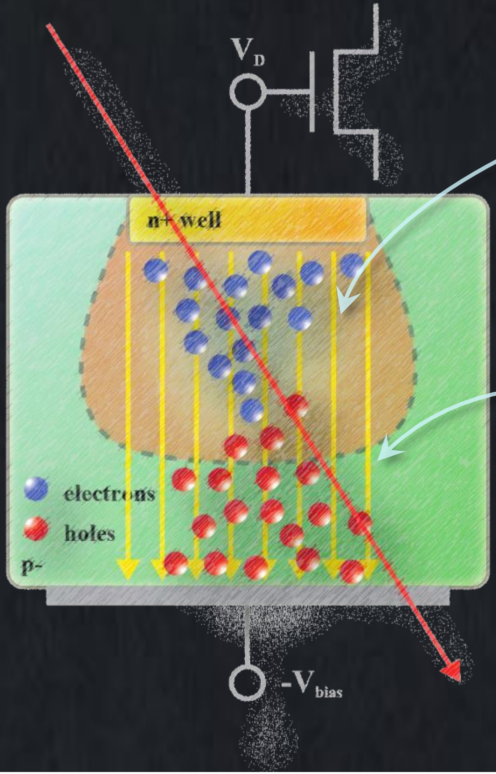
Charge collection by **diffusion**. Collection time of tens of ns.

Effective **collection depth limited** to the epitaxial layer (~10µm)

Sensor, front-end and read-out are embedded in the very same silicon detector. No external circuitry, no bump bonding.

Monolithic approach – high Ω substrate

Low doping, high Ω (>~100 Ω/cm) substrate



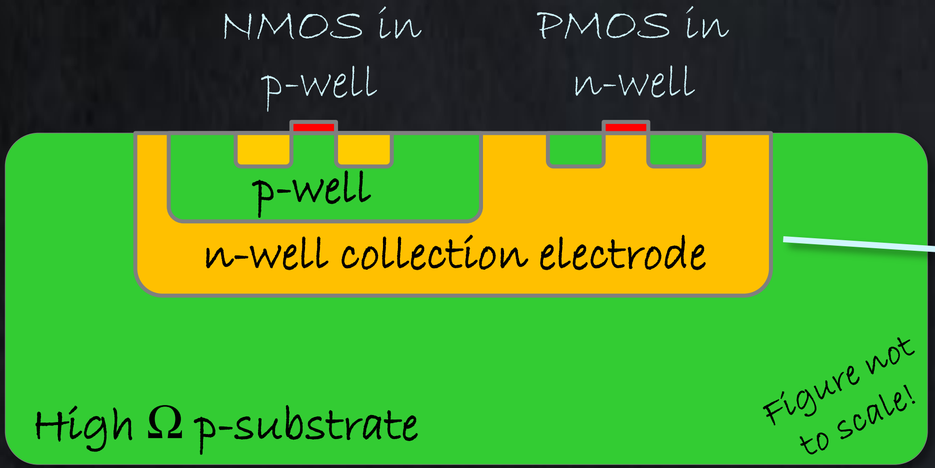
Charge collection by drift: faster, less recombination, higher radiation tolerance, faster collection (ns)

Effective collection depth depends (also) on the applied substrate bias

Monolithic integration -> low capacitance -> low power -> <u>key to low mass</u>

Higher signal, faster response, better radiation hardness (> 10 MRad), same simplicity, higher price (currently) than traditional M.A.P.S.

LePix: high Ω substrate monolithic in IBM 90 nm



High resistivity substrate (~ 400 Ω cm)

90 nm IBM process

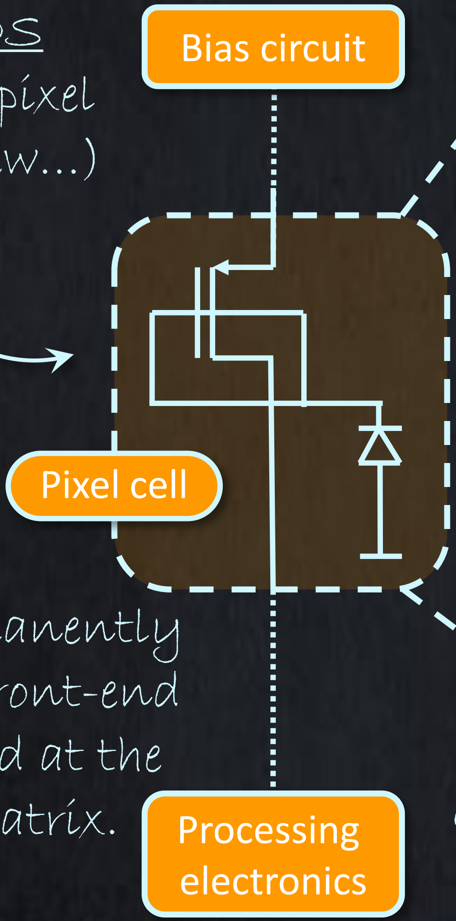
Only few transistors in the (small) collection electrode for low C (hence low power)

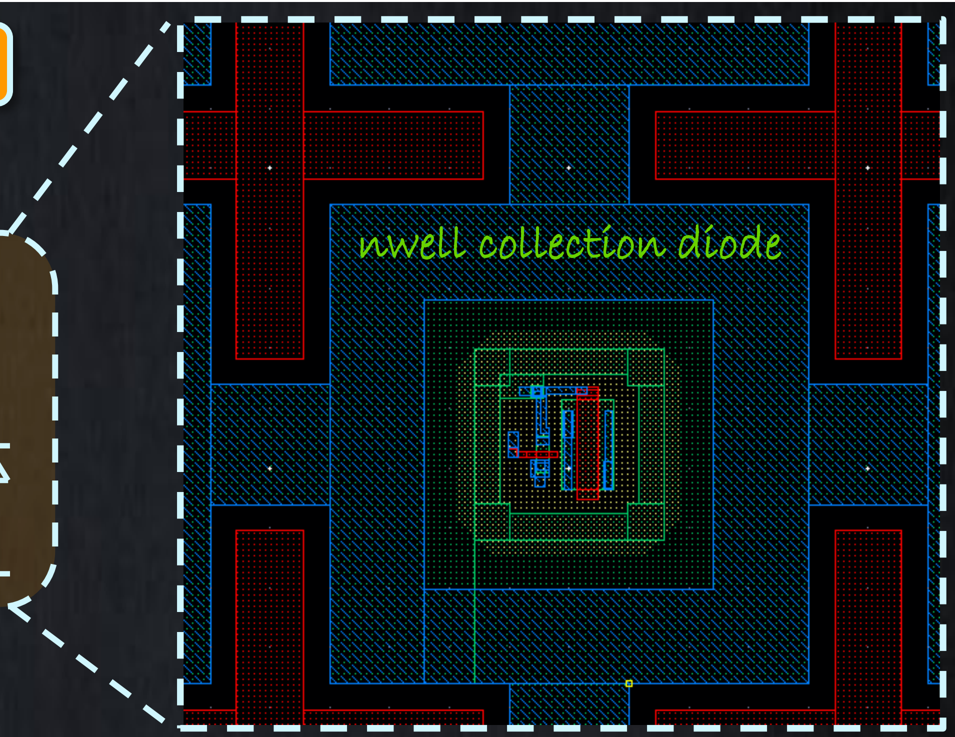
$$\frac{10\ fF}{px}, 50\mu m\ px \rightarrow \left.\frac{16\ mW}{cm^2}\right|_{1V@40MHz}$$

- Pixel clock costs significant **power**: move all the electronic at the periphery, lines from every pixel. Exploit 90 nm **low K dielectrics** in the metal.
- Need for uniform depletion layer (collection by drift, better radiation tolerance) makes **large pixel difficult** (50 µm seems already being a limit).
- Possibility of large area detector by **stitching**.

LePix pixel cell layout (top view)

Only one PMOS transistor in the pixel (or maybe very few...)

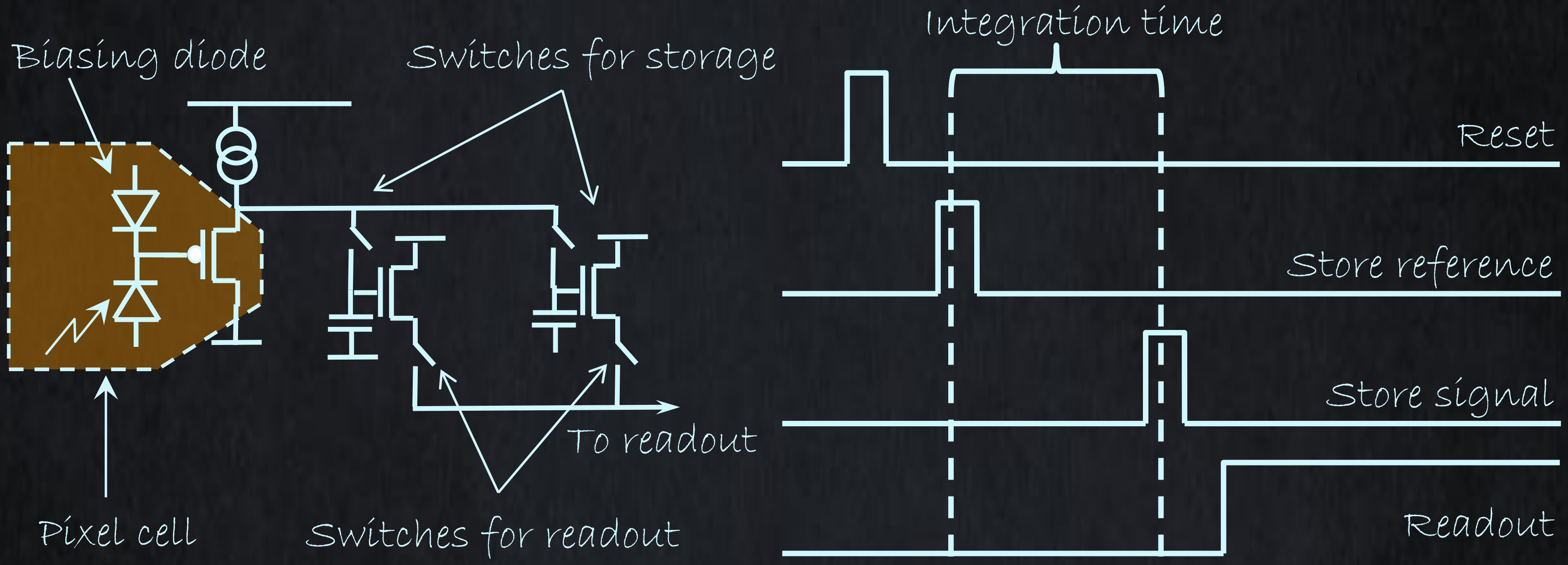




Each pixel is permanently connected to its front-end electronics located at the border of the matrix.

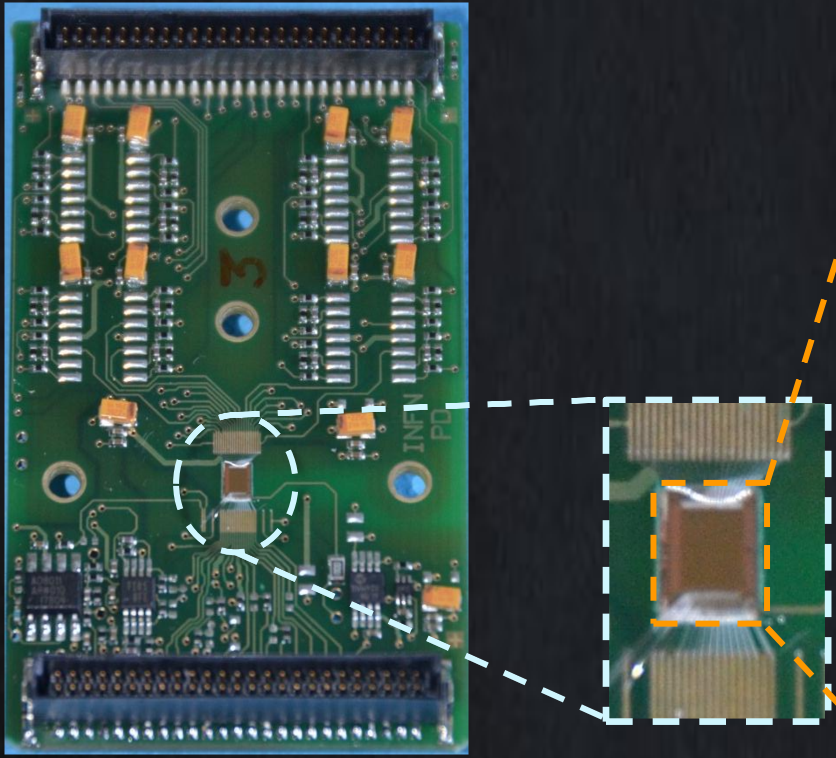
One or two dedicated lines per pixel: fine pitch lithography => 90 nm CMOS

LePix analog shutter logic

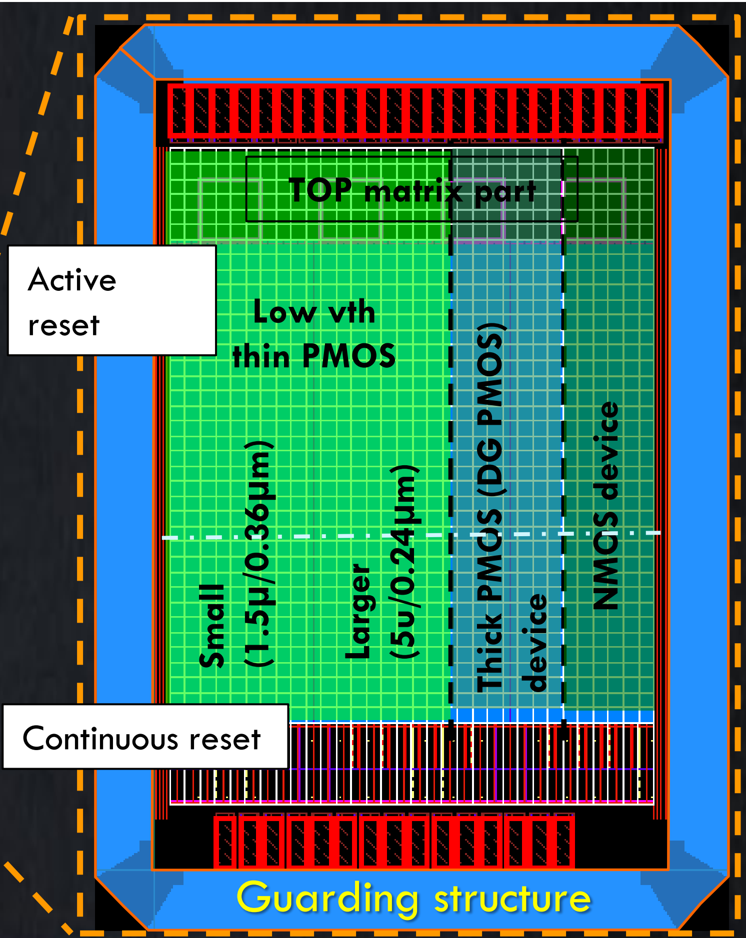


On periphery CDS. Parallel storage for all pixels: no rolling shutter, synchronous integration time independent from readout time.

The device

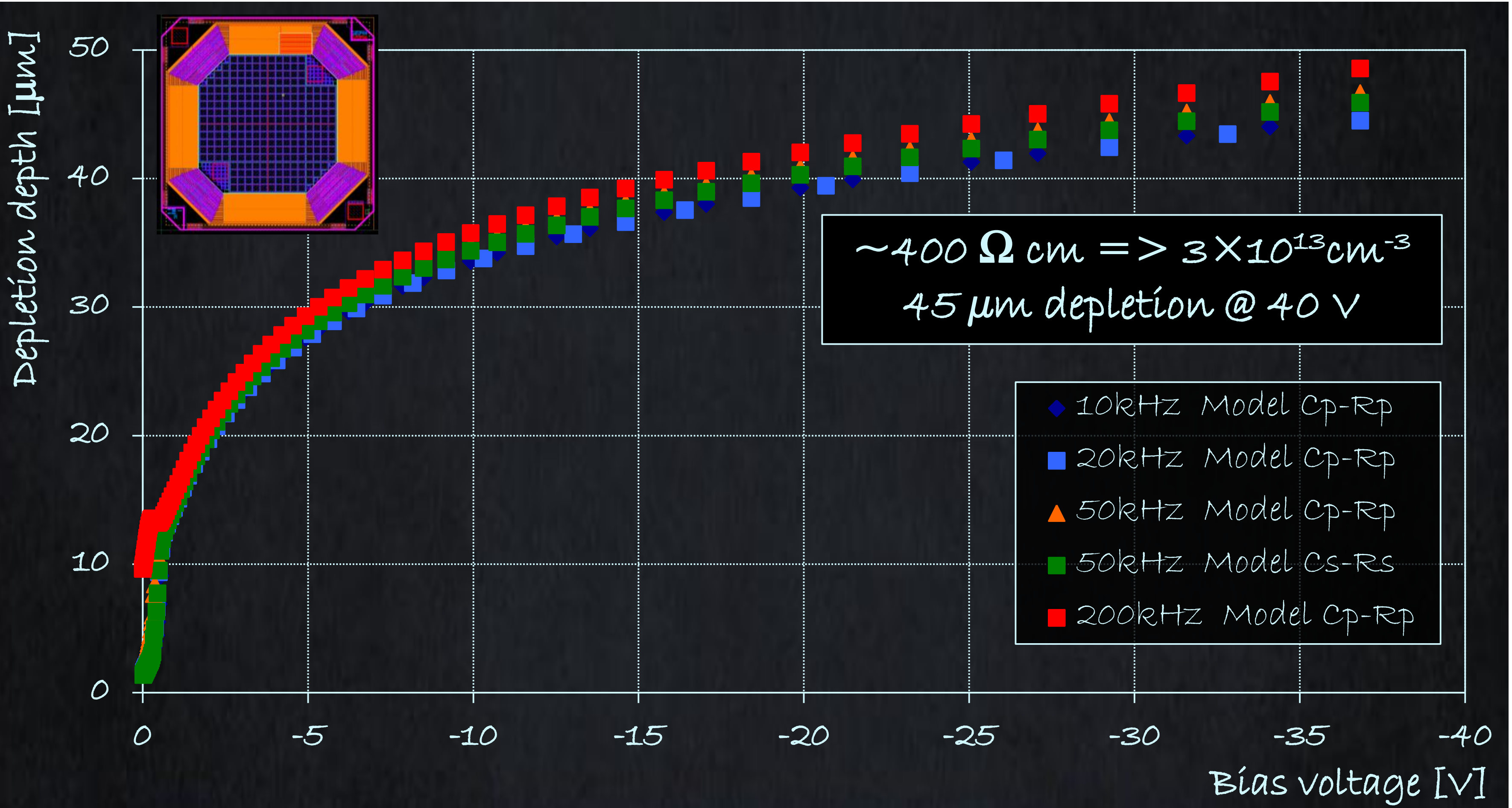


INFN
PD

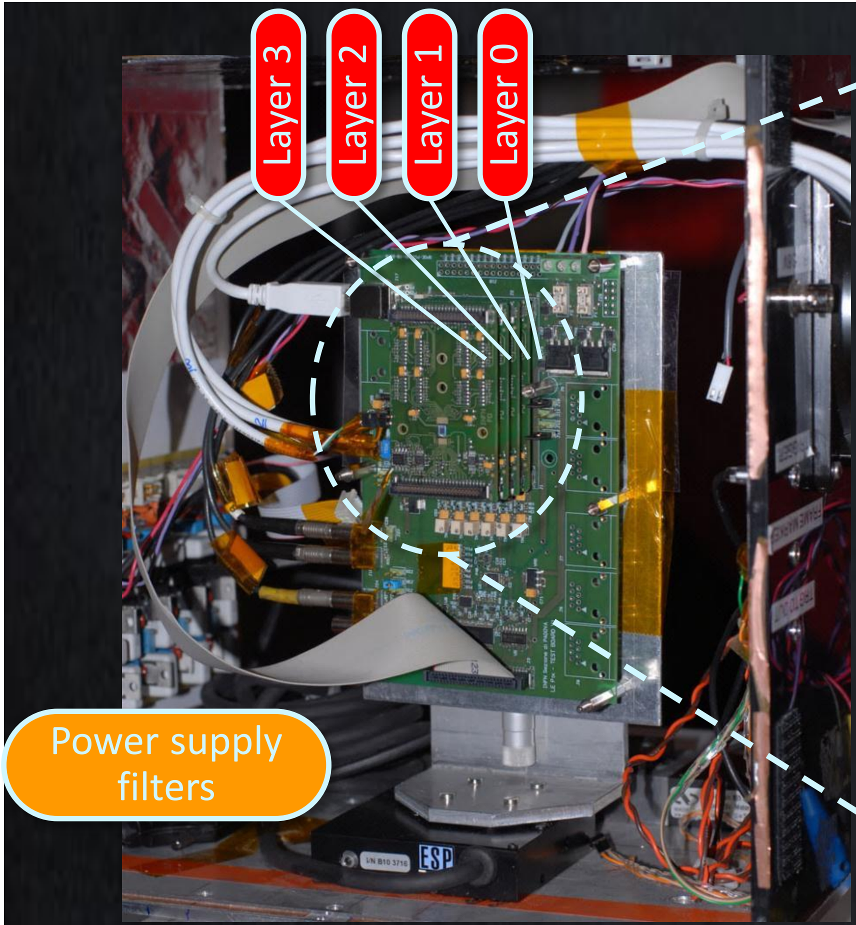


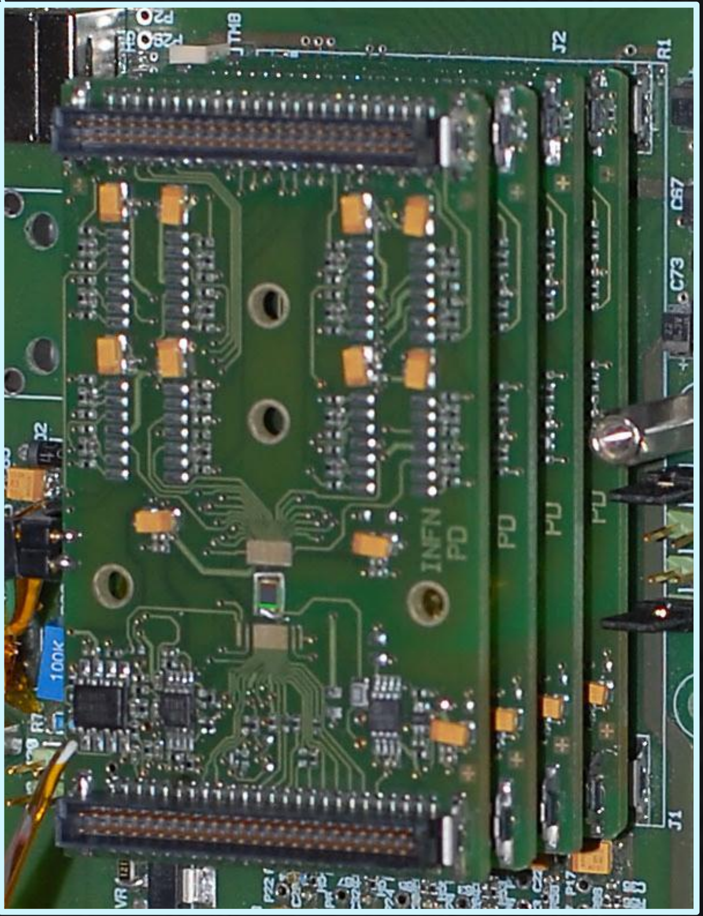
Active reset
TOP matrix part
Low vth thin PMOS
Small (1.5μ/0.36μm)
Larger (5u/0.24μm)
Thick PMOS (DG PMOS) device
NMOS device
Continuous reset
Guarding structure

LePix depletion depth measurements

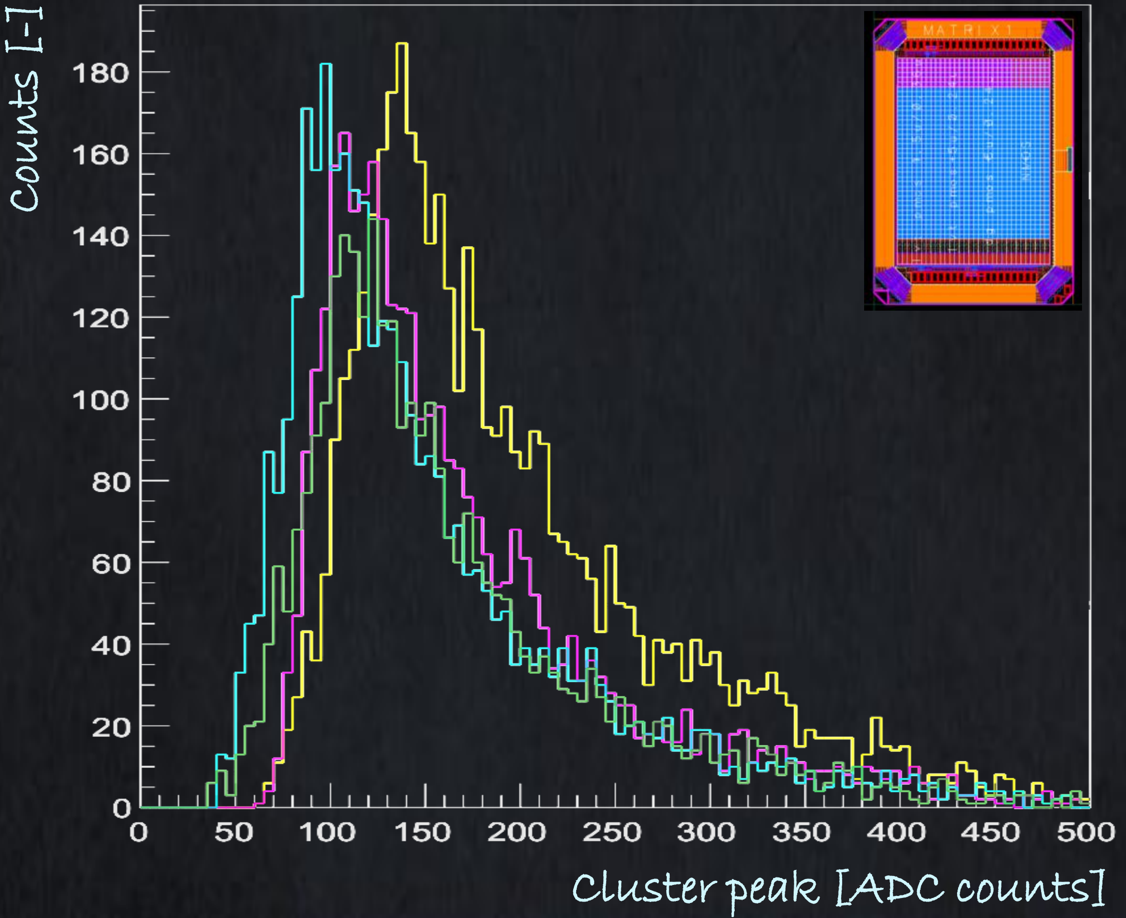


Test beam setup (both CERN SPS and PSI cyclotron)

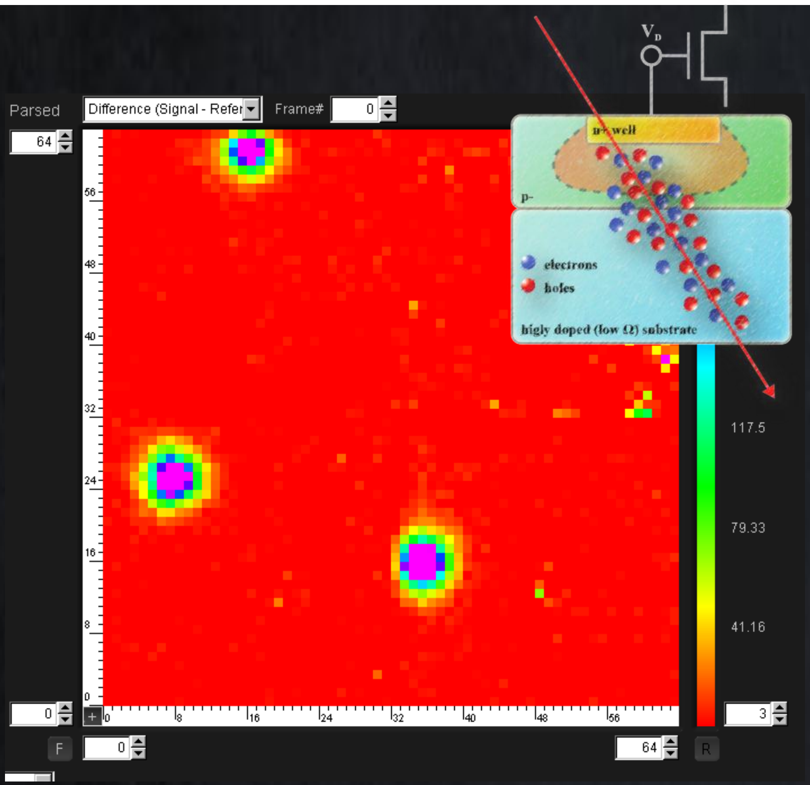




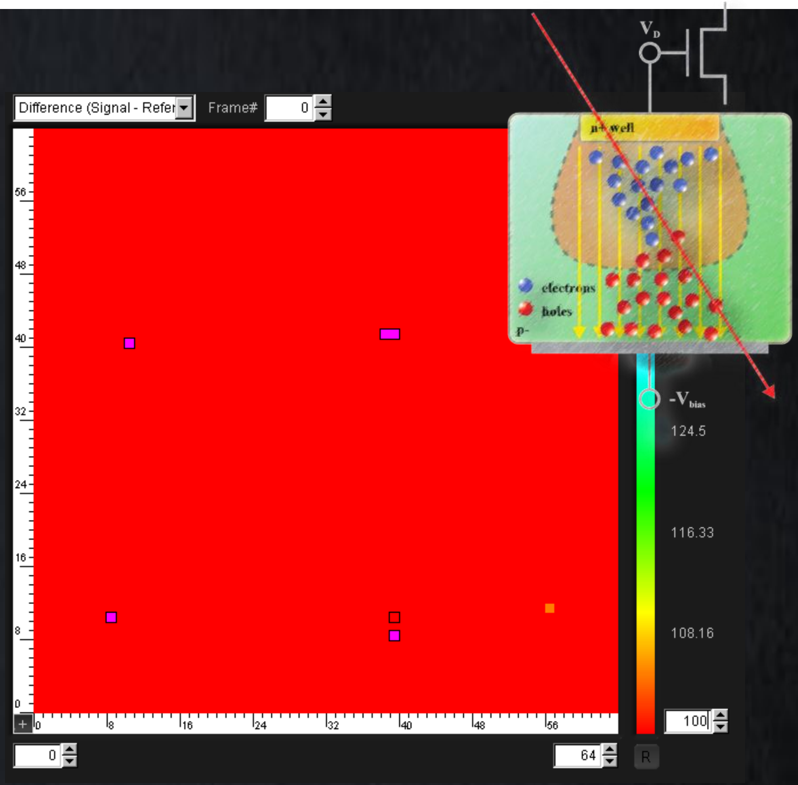
LePix with 300 GeV π at CERN SPS



LePix with 300 MeV p at PSI cyclotron

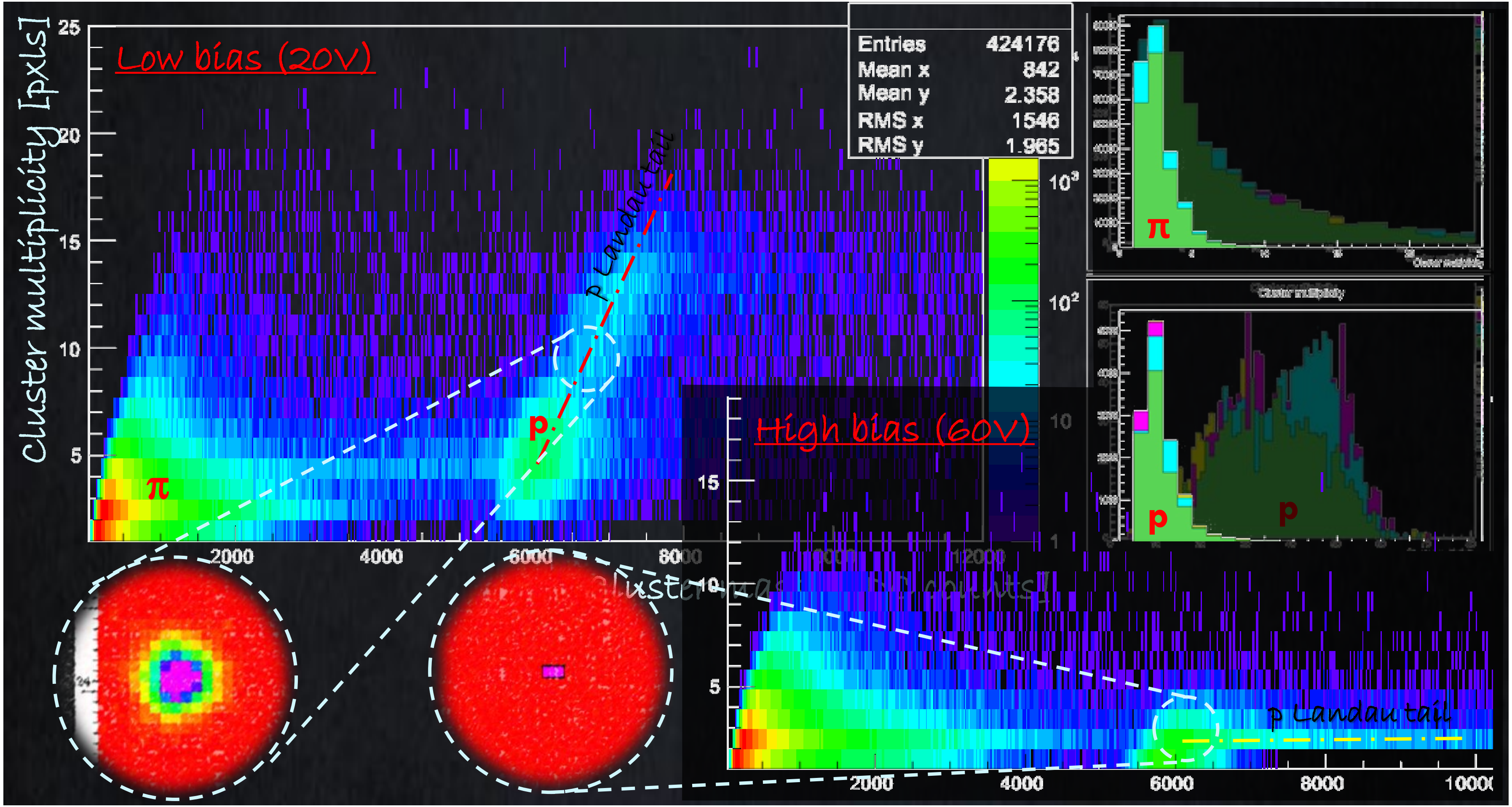


0 Volts bias



60 Volts bias

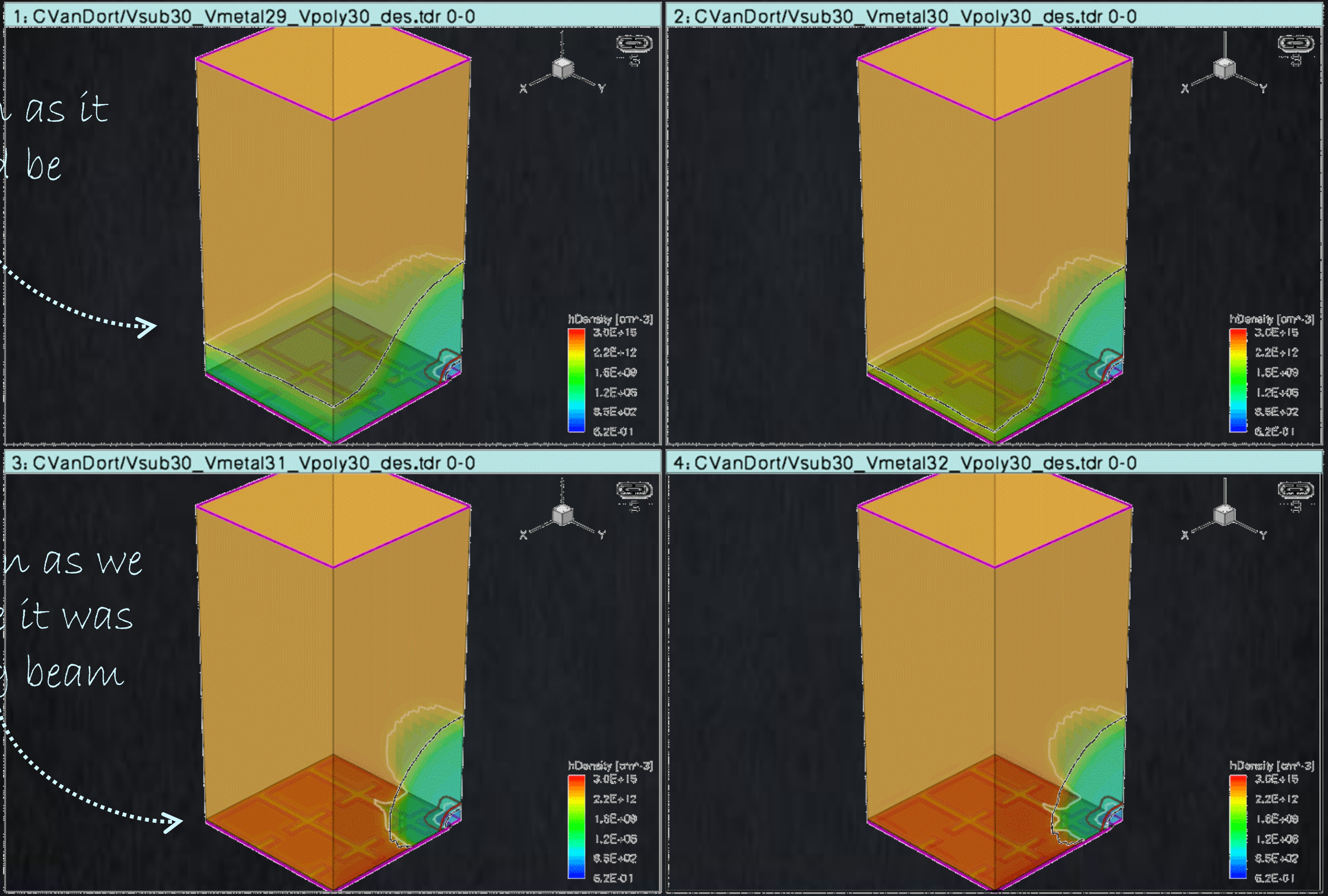
LePix with 300 MeV π⁻ and p at PSI cyclotron



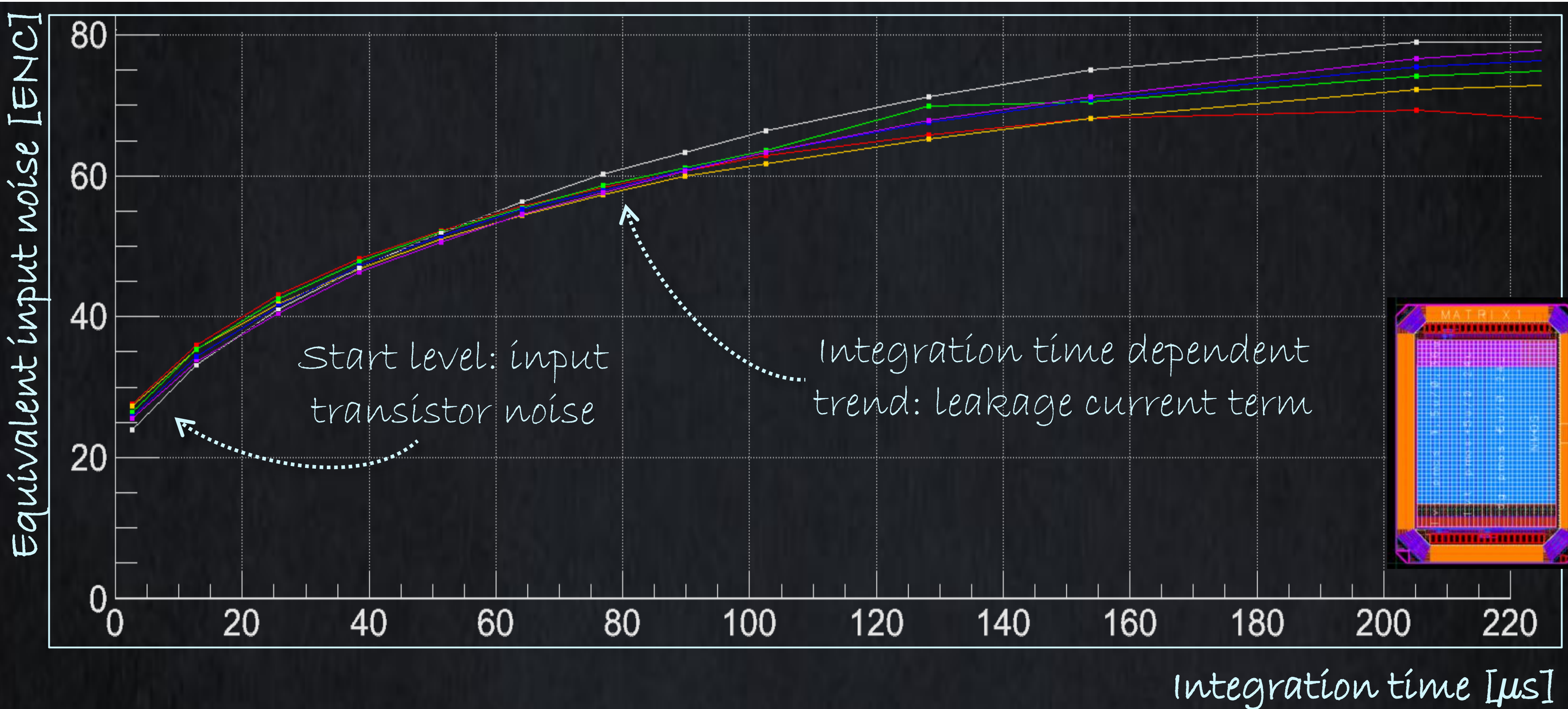
Efficiency problem (~70%) : depletion forms "bubbles"

Depletion as it should be

Depletion as we suppose it was during beam

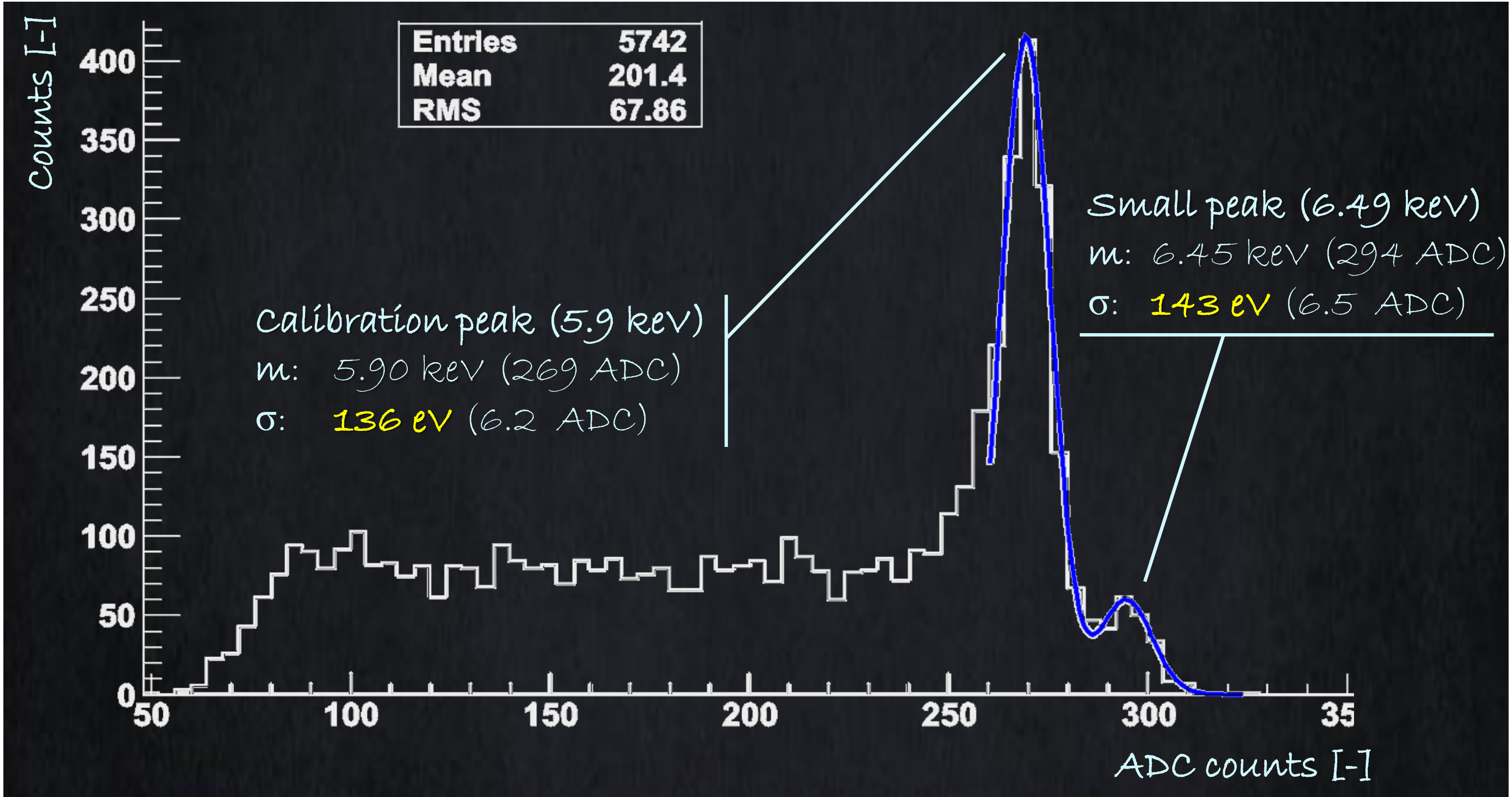


LePix noise (@ room temperature)



Equivalent input noise (all system inclusive) at room temperature is about 25 e^-, accordingly to what expected for the input capacitance measured value.

LePix with ^{55}Fe @ room temperature

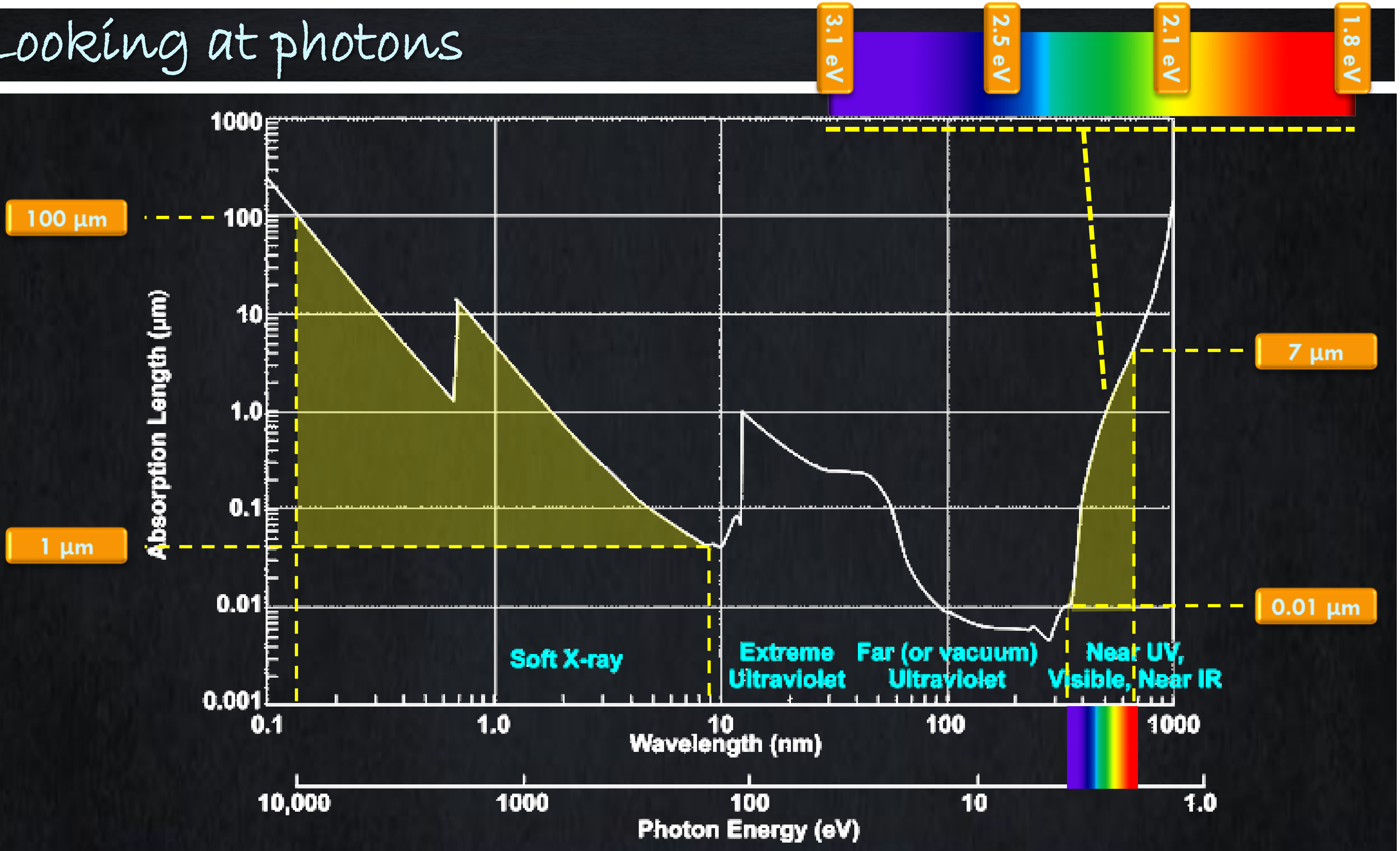


Looking at photons

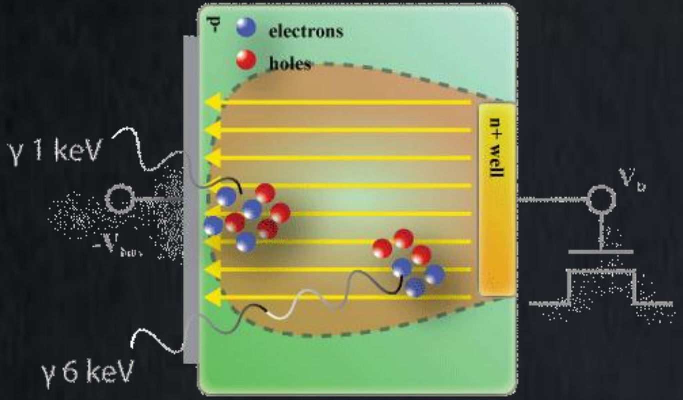
Even if LePix was designed as High Energy Physic detector with extremely low power consumption and material budget...

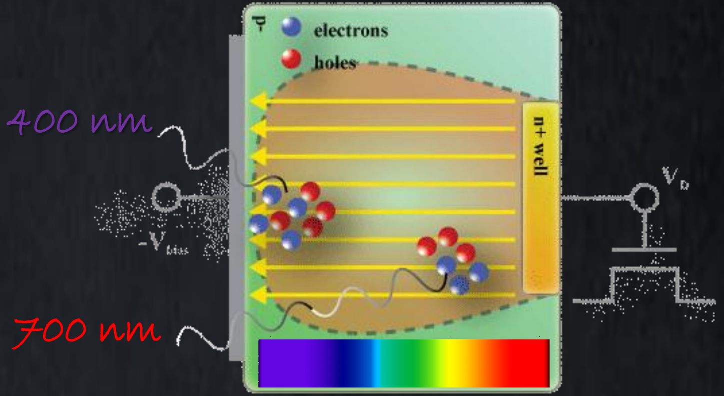
...it proved effective as (far lower energy) photons detector prototype.

Looking at photons



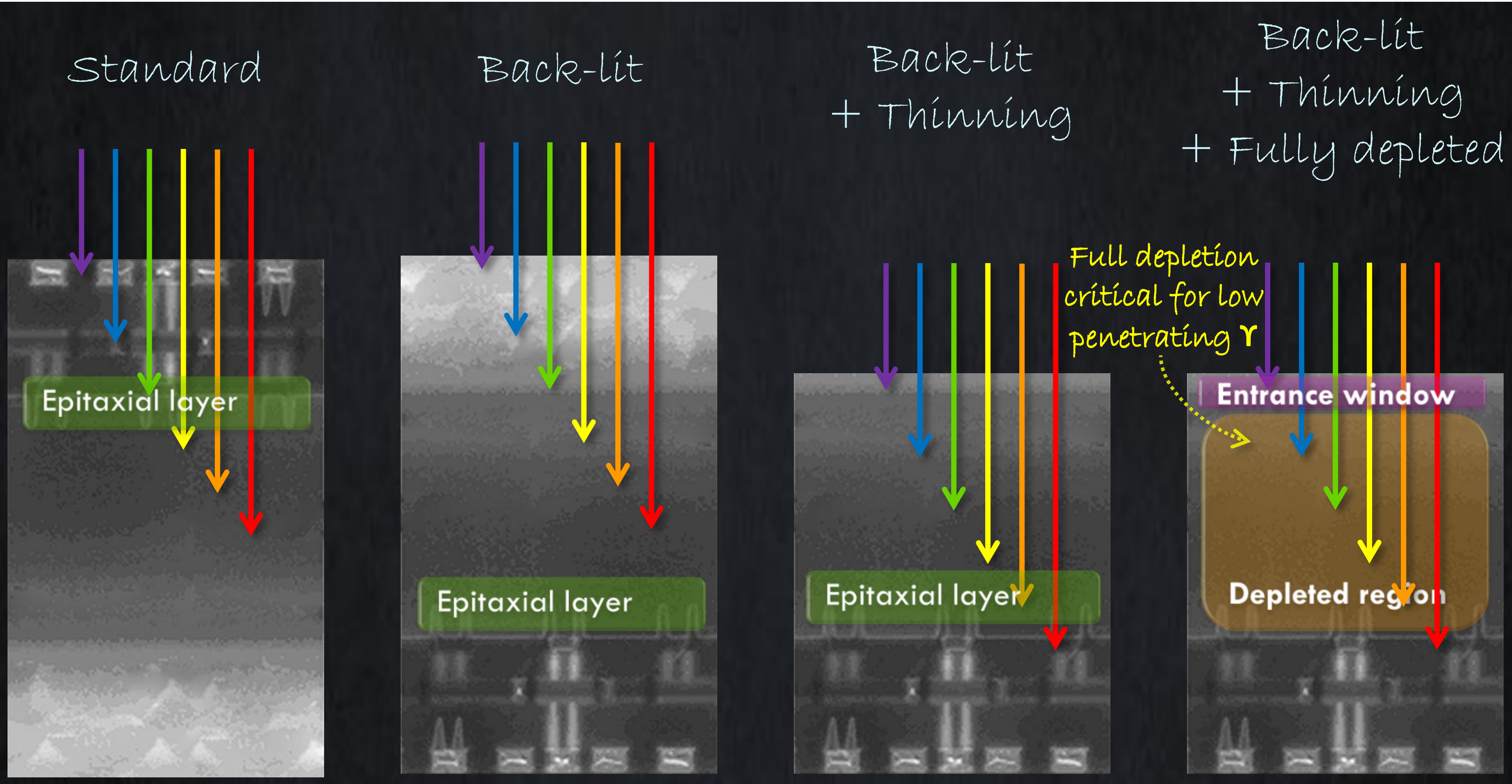
Back-illumination + thinning + full depletion





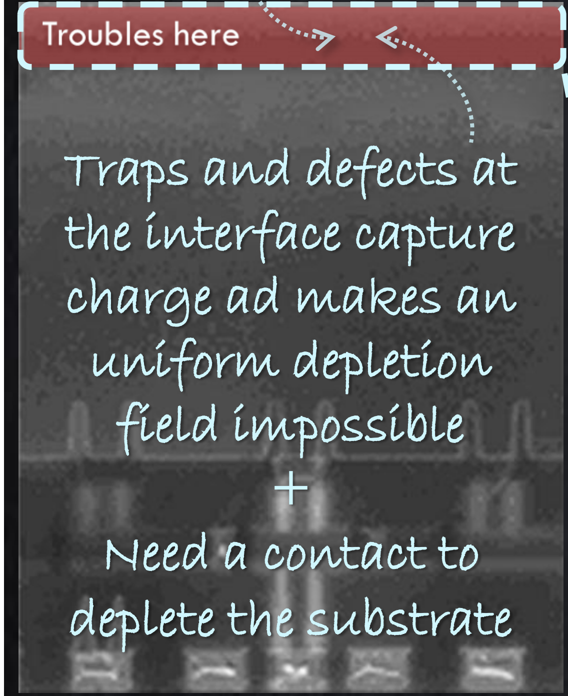
- Back-illuminated, fully depleted device could see the whole spectrum.
- Spectroscopic capabilities over full detection range thanks low noise.
- Soft X-Rays (0.5 keV – 10 keV) absorption length 1 µm – 100 µm.
- Visible range 0.05 µm – 7 µm color imaging without filters.
- Large area (up to 20 x 20 cm^2) and small pixel pitch (down to 1 µm) are key characteristics for Synchrotron Light Sources and Free Electrons Lasers.

Back-illumination + thinning + full depletion



Entrance window processing is critical

Thinning produces stress on the material



Traps and defects at the interface capture charge ad makes an uniform depletion field impossible
+
Need a contact to deplete the substrate

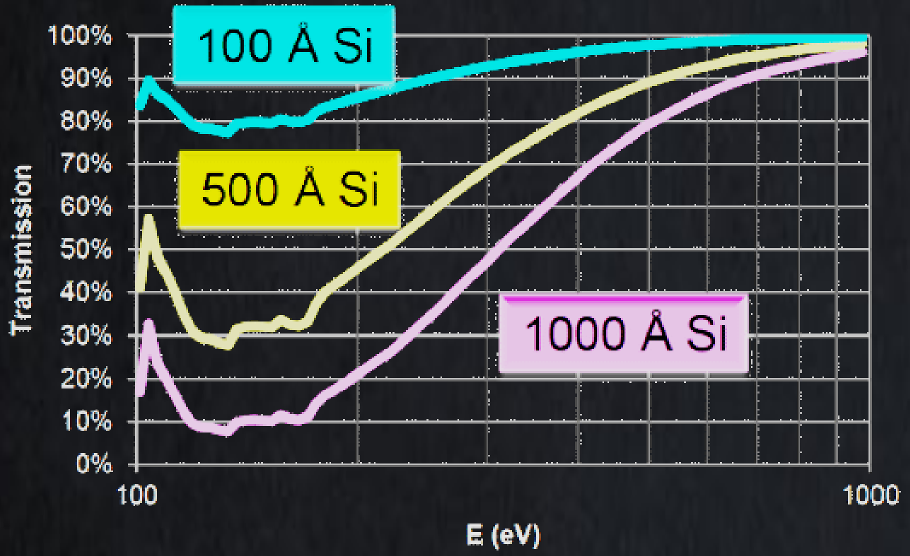
Thin window processes (LBNL)

Process	Window thickness	Status
Low energy implant + 500 C annealing	1000 – 2000 Å	Process dependent, SOI, LePix functional
Low energy implant + laser annealing	400 – 700 Å	Several SOI prototypes functional
A-Si contact deposition by sputtering	300 Å	Prototypes functional, high leakage
In-situ doped poly (ISDP)	100 – 200 Å	Standard MSL process
Molecular Beam Epitaxy	50 - 75 Å	Developing in-house capability

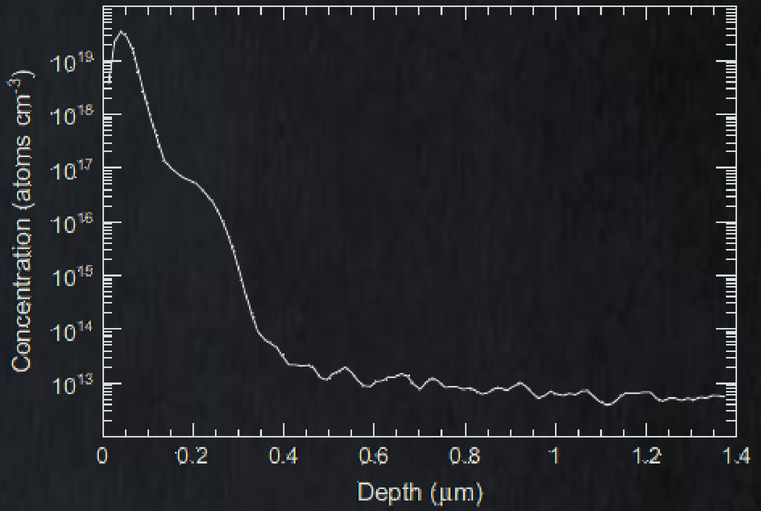
[From Craig Tindall, LBNL]

LBNL thin window for increased transmission

Entrance window transmission



Deposition profile



LBNL low temperature process: cold P implant at 33keV, -160°C to create amorphous layer, annealing @ 500°C (10 min Nitrogen atmosphere).

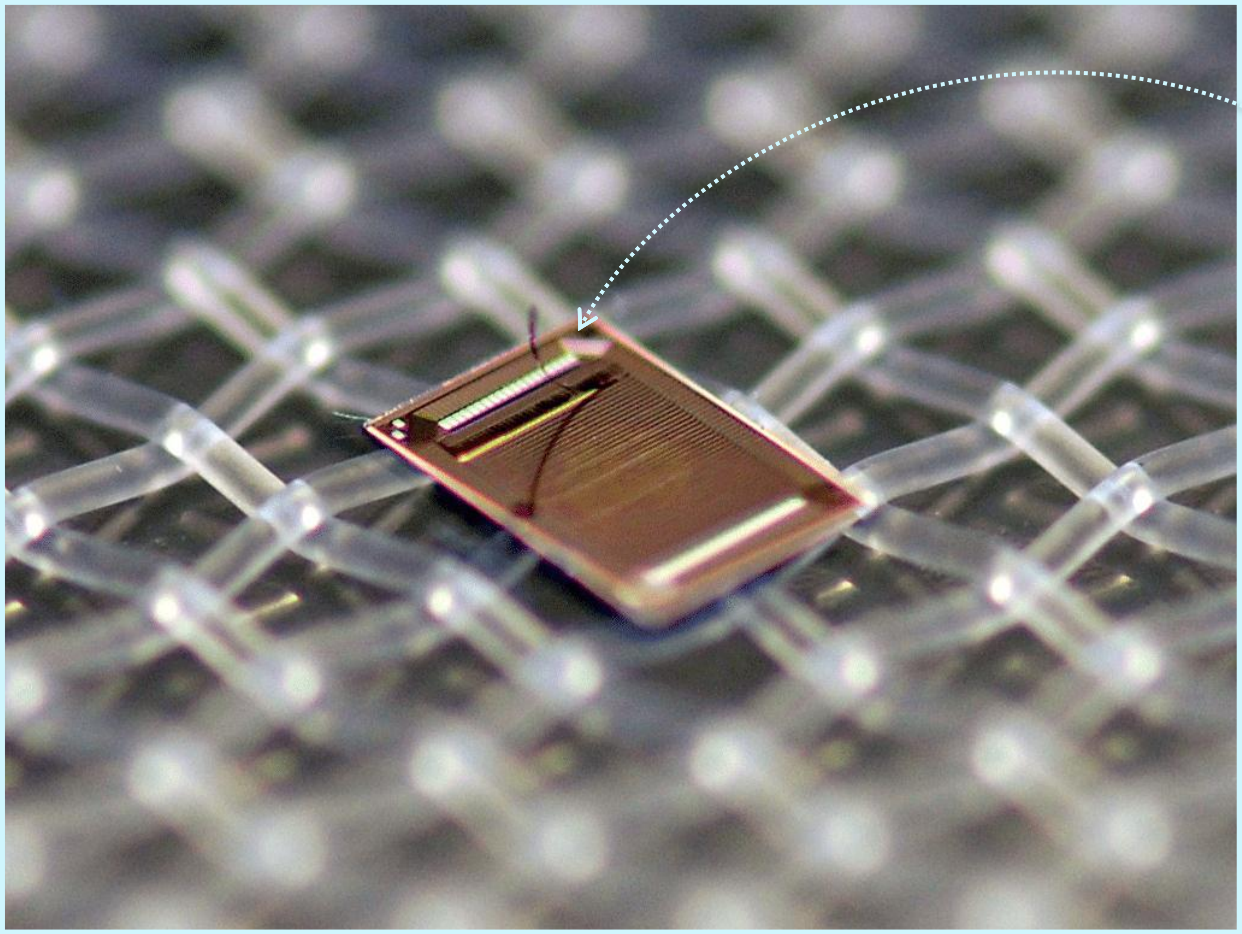
Spreading Resistance Analysis (SRA) measurements show P contact extending to 0.3 - 0.4 µm depth.

[From Craig Tindall, LBNL]

First processed LePix prototype

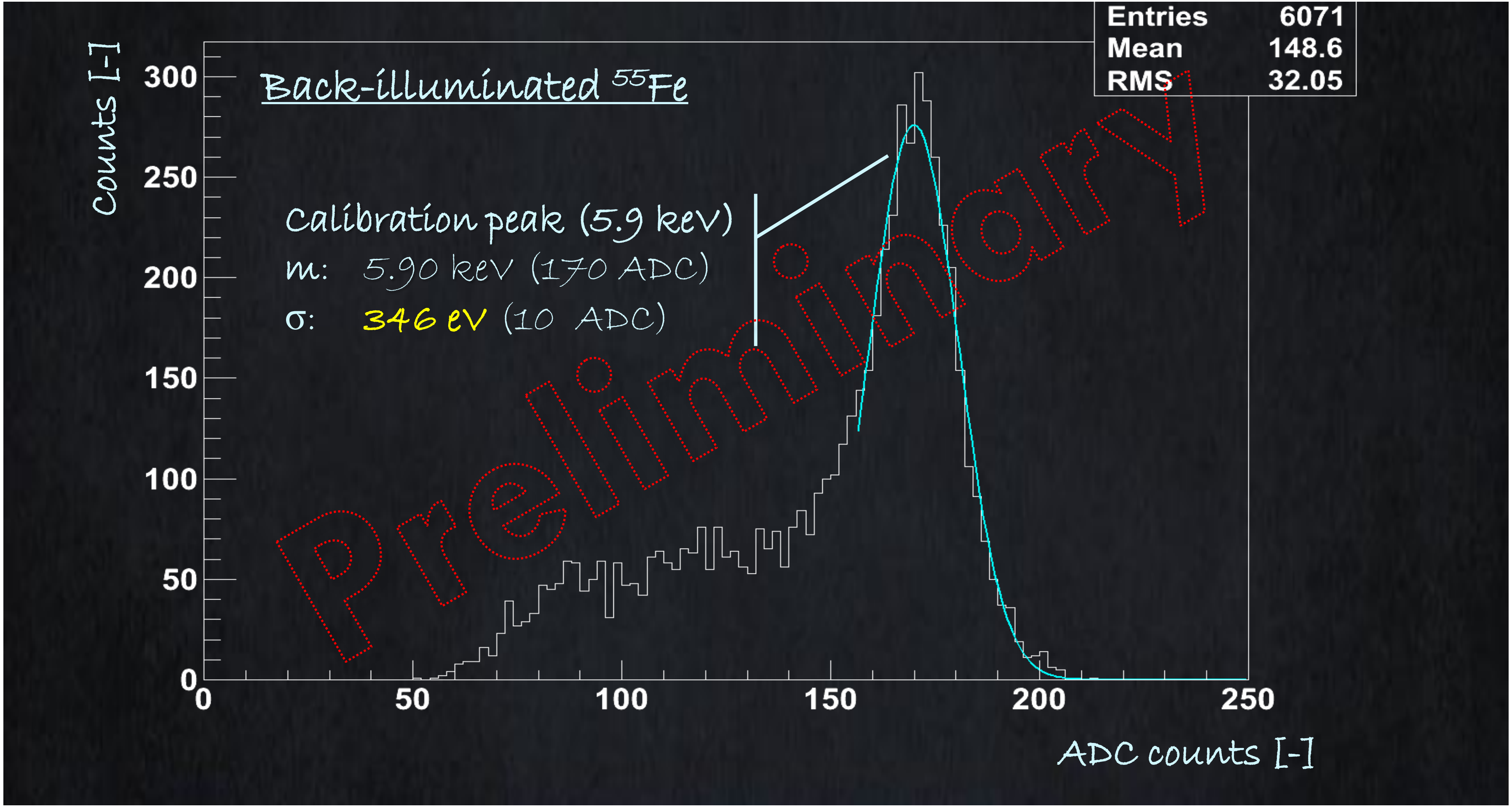
- Few LePIX matrices have been thinned down to about **50µm** and back-processed at LBNL.
- Back-process consisted of two steps: **ion implantation** and **annealing**.
- The **annealing** step **is critical** (temperature issue) so that:
  - We lost two chips annealed at the highest temperature.
  - Two chips annealed at 50°C below the standard temperature are dead as well. One lost after the first tests (working at the beginning, even though we could not see any signal from any source, and then lost) and one dead since the very beginning.
  - One chip annealed at 100°C below the standard temperature is alive and working.

Processing is NOT such an easy step....



Thinned (50 µm) chips do not like thermal stress!

...but we have a first working device!



Conclusions

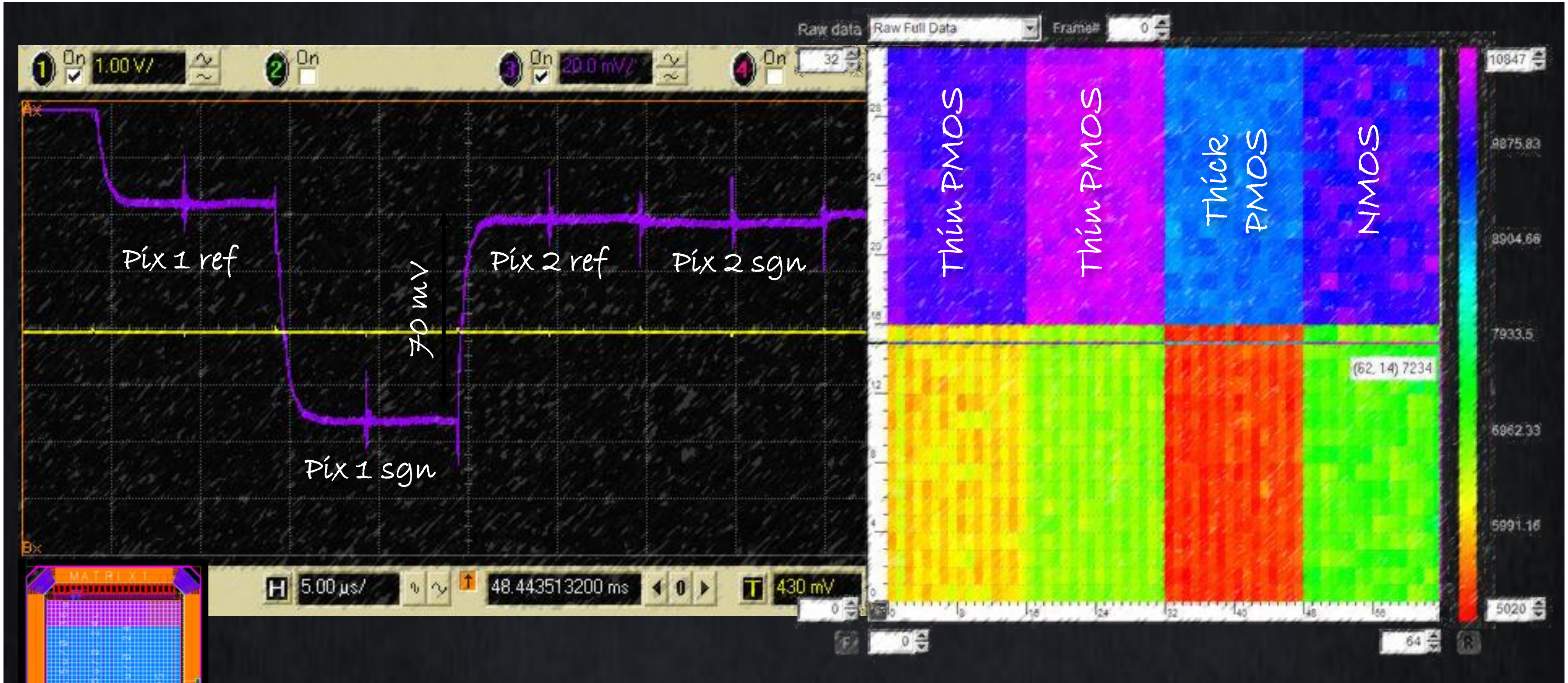
- Near-commercial CMOS process, low cost in case of large production runs (engineering runs still expensive, but other foundries claim do the same).
- Reasonable radiation tolerance (10 MRad / 10^{14} Neq) from scratch.
- High spatial resolution (1 um pixel pitch) possible, large area though stitching, now commercially available.
- Large edgeless detectors through stitching.
- Low power consumption (10 mW/cm^2), hence low material budget.
- Full spectrum in a monolithic device is possible, yet many processing parameters to be investigated/optimized.
- Soft X-ray (10 keV) seems a feasible goal for a 50 – 100 µm depleted device.

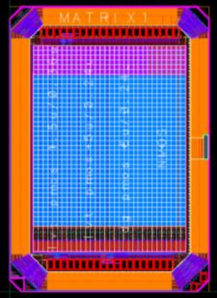
Backup

Backup slides…

LePix matrix test pulse measurements

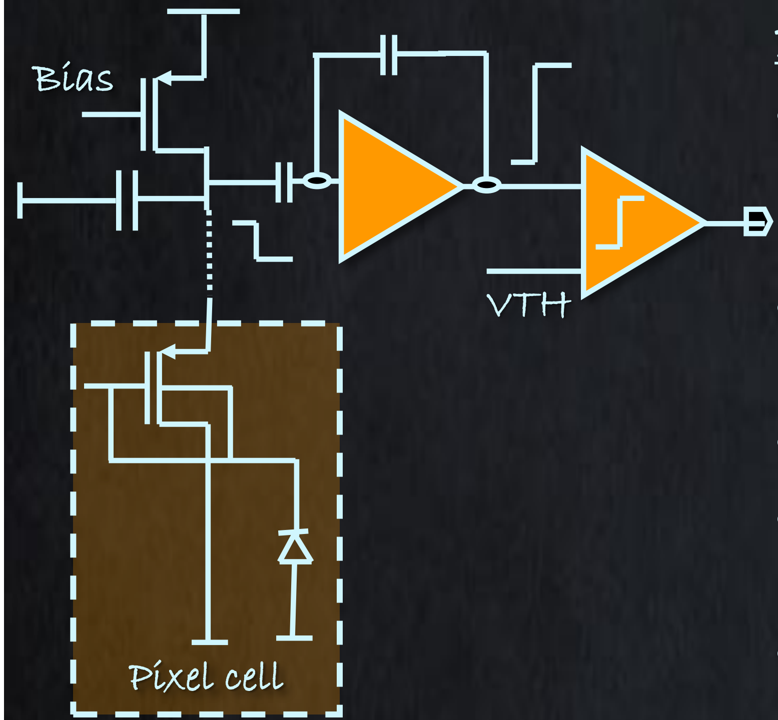
Piero Giubilato – VCI 2013 – Vienna, 11 Feb 2013





Low C is key to reach low power, pulse measurement illustrates very low capacitance, around **4 fF** for small collection node pixels.

LePix also sports "digital" pixels

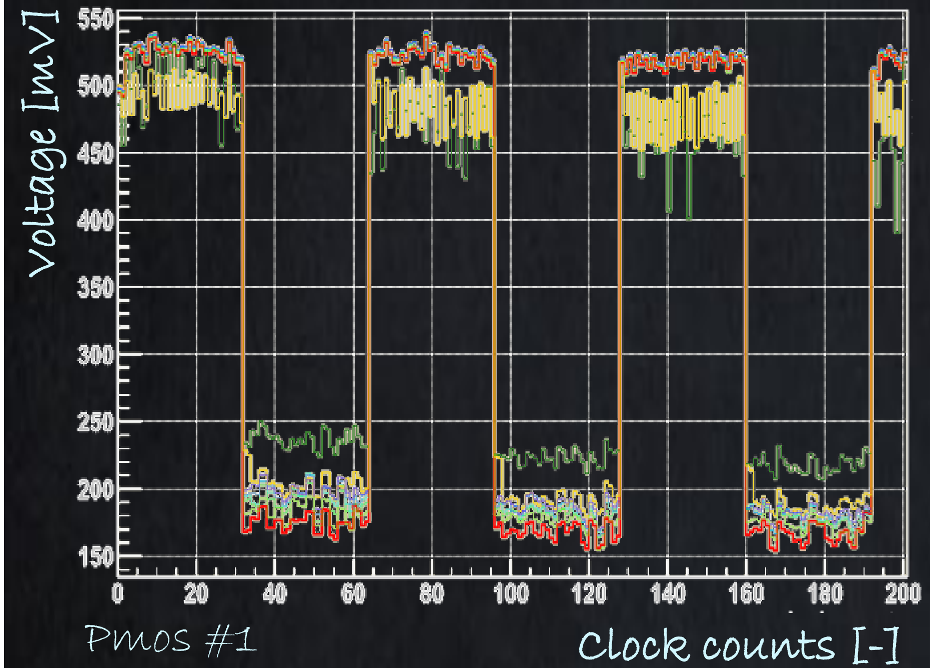


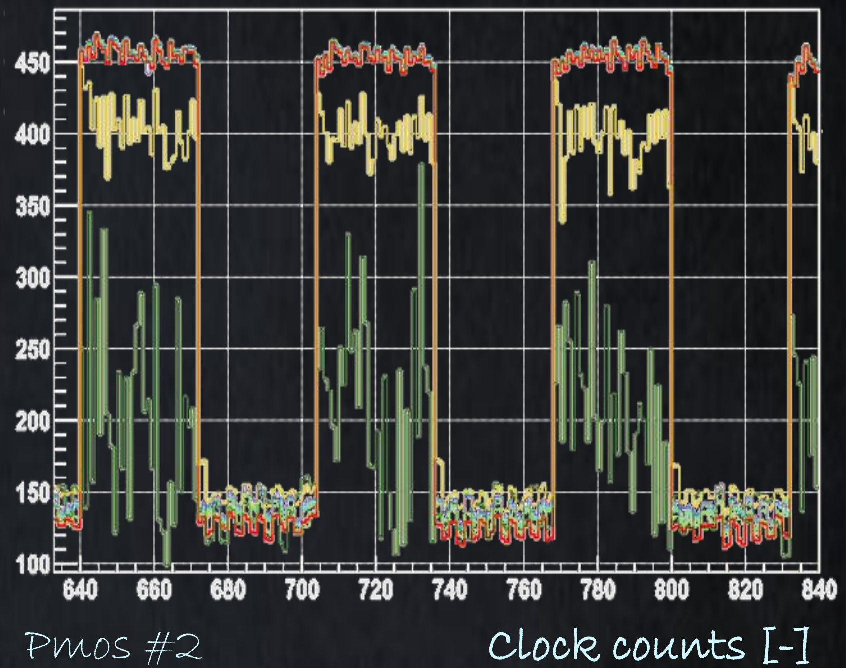
Digital readout

- The current signal is converted to a voltage step by integration on the input parasitic capacitance (~ 10 fF).
- Voltage step sensed at the source and fed to a preamplifier-shaper-discriminator chain.
- Stack of only two transistors.
- Margin to operate the sensor at low power supply (0.6 V).
- Enough headroom for leakage induced DC variations.

Only one external line per pixel. The rise time of the signal, but not its final amplitude sensitive to the parasitic capacitance of the line.

LePix irradiation (10 MRad X-Ray)





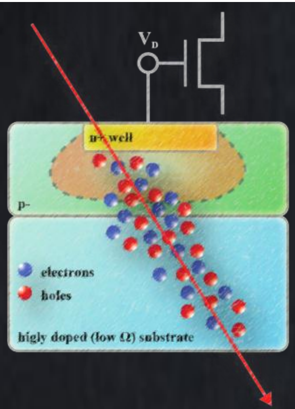
(4.8 kRad/min, biased) pre (red) and post (green) rad, one week at room T (yellow)

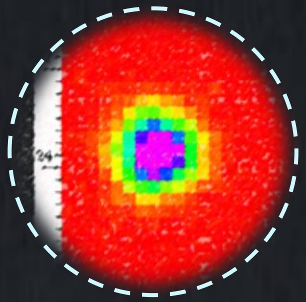
Some sectors more affected than others immediately after irradiation, reasonable recovery after one week.

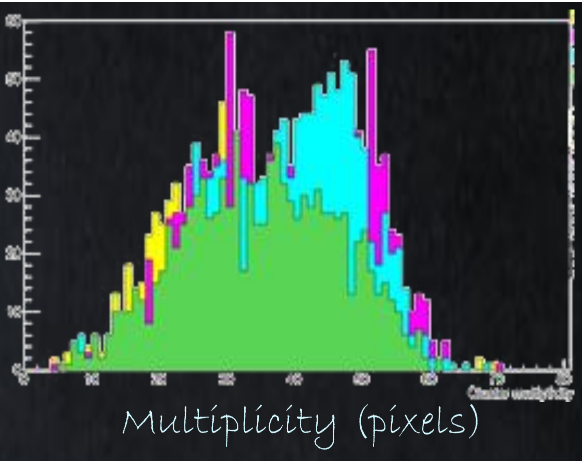
LePix: clusters multiplicity summary

300 MeV protons beam
50 um pixel (LePix detector)

No bias







60V bias