Contribution ID: **225** Type: **Talk**

A Low Mass On-chip Readout Scheme for Double-sided Silicon Strip Detectors

Wednesday, 13 February 2013 09:50 (20 minutes)

B-factories like the KEK-B in Tsukuba, Japan, operate at relatively low energies and thus require detectors with very low material budget in order to minimize multiple scattering. On the other hand, front-end chips with short shaping time like the APV25 have to be placed as close to the sensor strips as possible to reduce the capacitive load, which mainly determines the noise figure.
In order to achieve both - minimal material budget and low noise - we developed a readout scheme for double-sided silicon detectors, where the APV25 chips are placed on a flexible circuit, which is glued onto the top side of the sensor. The bottom-side strips are connected by two flexible circuits, which are bent around the edge of the sensor.
This so-called "Origami"design will be utilized to build the Silicon Vertex Detector of the Belle II experiment, which will consist of 4 layers made from ladders with up to five double-sided silicon strip sensors in a row. Each ladder will be supported by two ribs made of a carbon fiber and Airex foam core sandwich. The heat dissipated by the front-end chips will be removed by a highly efficient two-phase CO2 system. Thanks to the Origami concept, all APV chips are aligned in a row and thus can be cooled by a single thin cooling pipe per ladder.
We will present the concept and the assembly procedure of the Origami chip-on-sensor modules, and show results of beam tests which were performed at CERN on prototype modules.

quote your primary experiment

Belle II

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Session Classification: Semiconductor Detectors 2