3-Dimensional ASIC Development at Fermilab

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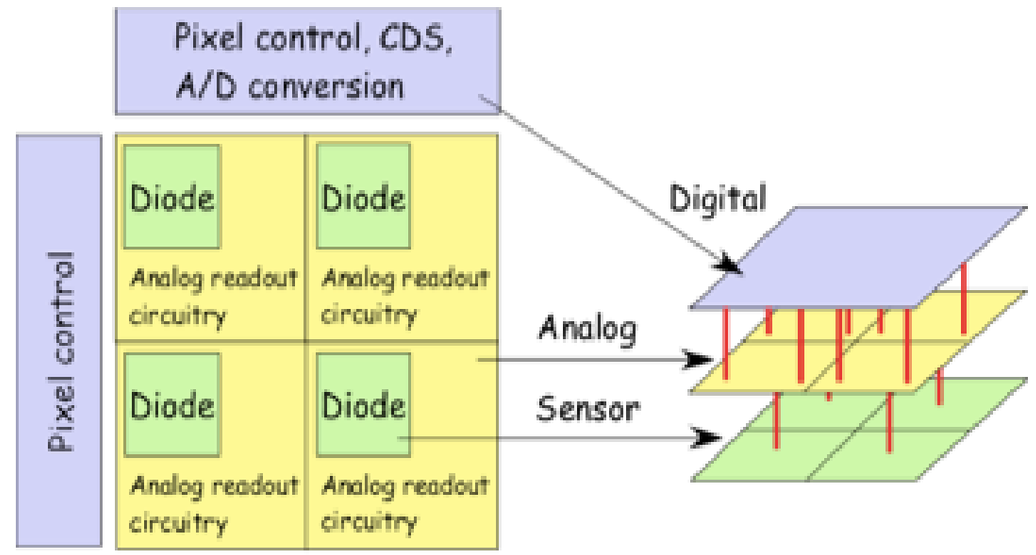
Performing the fastest signal processing possible means we have to leave the 2 dimensional world behind

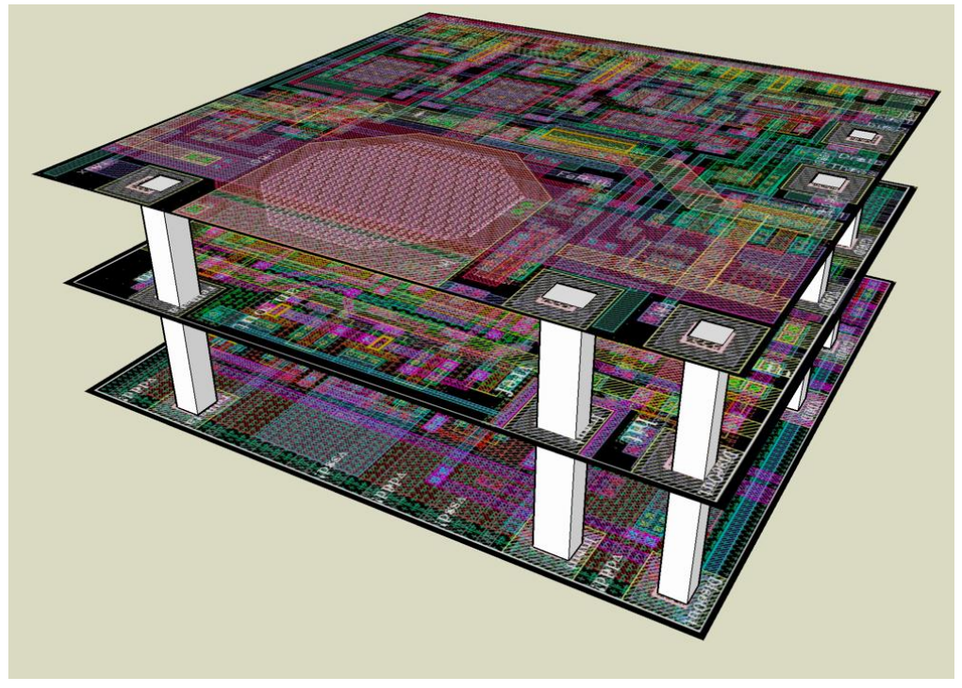
- Industry and government initiated development of vertical integration, since Moore's law would not extend beyond ~ 2020

- What is 3D vertical integration?:
  2 or more layers ("tiers") of active semiconductor devices that have been thinned, bonded and vertically interconnected to form a monolithic circuit



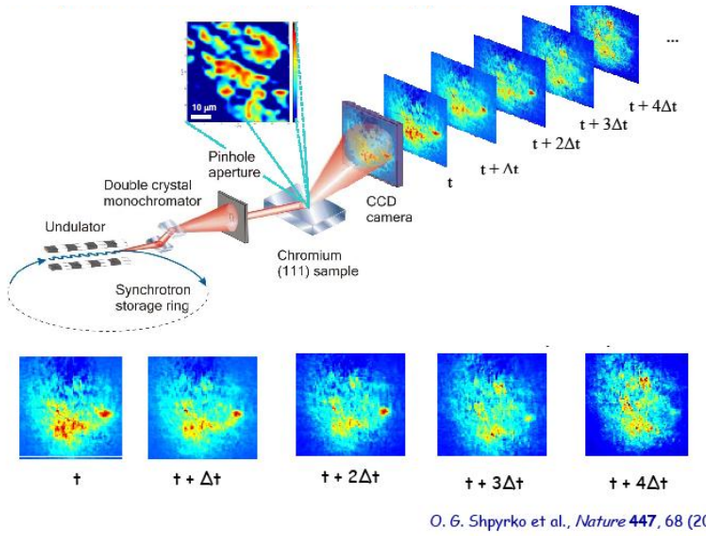
- This type of integration improves circuit performance:
  - No fine pitch bump bonds
  - Reduces R, L, C for higher speed
  - Reduces chip I/O pads (less dead area)
  - Technology of each layer can be separately optimized
  - Reduces interconnect power and crosstalk
  - Can give more transistors per cm^2

- Processes now available commercially



3D ASIC Applications

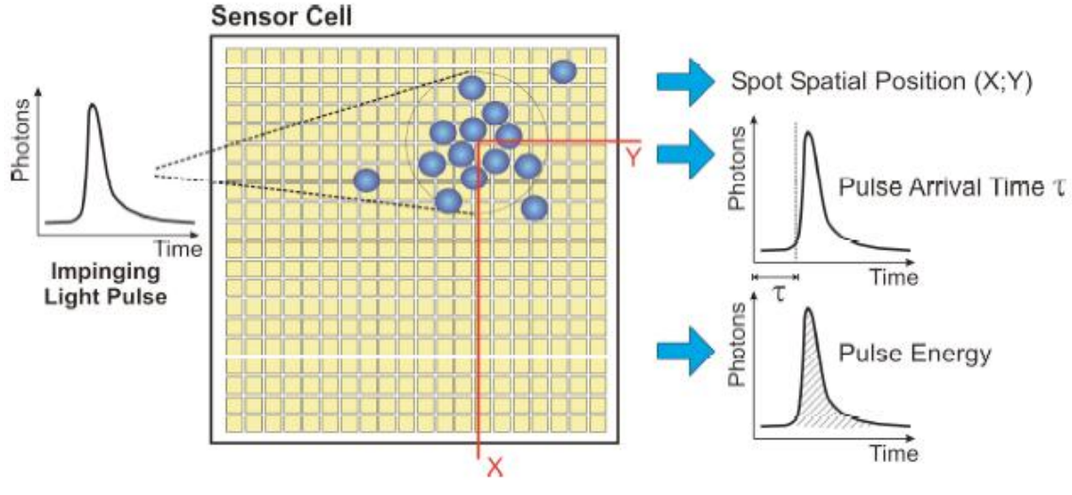
- We are just at the beginning of exploring 3D ASICS.
- Directions to pursue include:
  - 3D sensors
  - High density pixel (ILC type)
  - LHC track trigger
  - X-ray imaging with time tag
  - Pixel chip size reduction
  - B factory Vertex
  - CMOS/CCD integration
  - SiPM with per pixel digital readout
  - 3D associative memories for triggering



O. G. Shpyrko et al., *Nature* **447**, 68 (2007)

Time correlated X-ray counting

Silicon Photomultiplier with individual diode addressing



ASIC Resources at Fermilab

- ASIC Group is part of Particle Physics Division Electronic Engineering Department
- 6 ASIC designers (3 PhDs)
  - 2 senior – project leader level
  - 1 engineering physicist
  - 1 test engineer
  - 2 technicians

  + PCB drafter depending on needs
  + occasional support from other resources within PPD/EED, Computing Division and other departments at Fermilab

- Design Software:
  - Cadence – main frame
    + Mentor Graphics – Silvaco (and Magma + Tanner)
  - Shifting from Cadence IC5.1X to IC6.1X (all new designs under IC6.1X OA) – (underway),
  - Migration from Eldo (Mentor Graphics) to Analog-Mixed-Mode Simulation (AMS) with Spectre (Cadence) – (2011),
  - Solicitation for: ASSURA PVS, VSR and VDI (budget dependent) – to be capable of 65nm flow - (2012),

- ASIC test lab spaces
  + “clean room” (probe stations /one capable 8”/ and measurement instruments)
- + 2 labs (FlexRIO National Instruments systems and test equipment + lab. radioactive sources)
- + robotic chip testing station (upgrade)
- + manual bonding station
- + PCB components mounting lab

History of Fermilab Initiatives in 3D

- 2006: FNAL participates in 2 multi-project-wafer runs organized by MIT-LL and submitted the VIP (vertically integrated pixel) chip, driven by ILC specs for vertex pixels.
  - MIT-LL: 3 tier fully depleted SOI process
  - Tiers communicate with Through Silicon Via's (TSV)
  - Proof of 3D principle

- In 2009, FNAL initiated and organized 3D-IC MPW for HEP and related fields
  - Standard CMOS foundry process (0.13 μm), wafers fabricated by Global Foundries
  - 3D processing and stacking done by Tezzaron
  - VICTR chip (vertically integrated CMS tracker for sLHC)
  - VIP2b (ILC pixels, 8-bit digital time stamp)
  - VIPIC (x-ray spectroscopy)

- In 2011, 3D design kit built by CMP and adopted by MOSIS, based on Global Foundries 130 nm process, using data from Tezzaron, NCSU, Fermilab and others

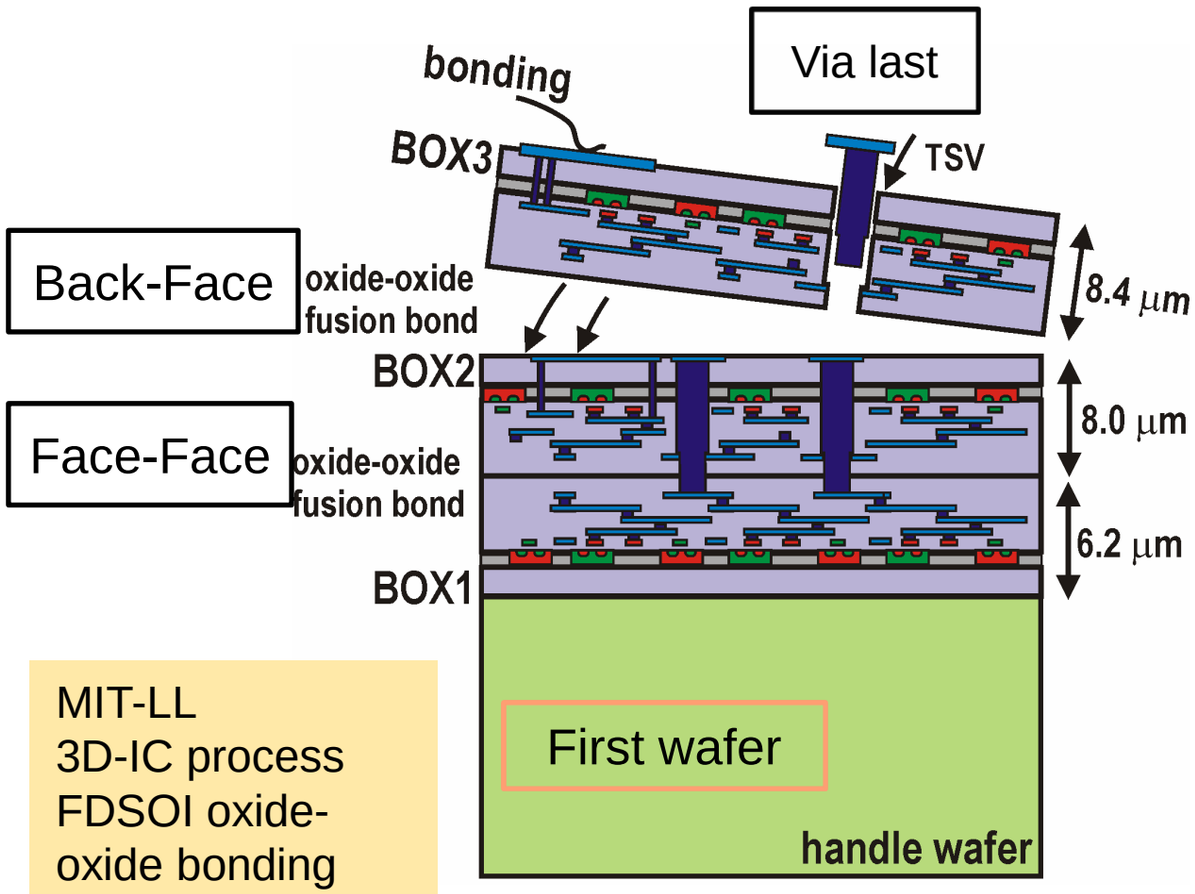
- Helped develop new handling techniques
  - Thinned detectors
  - Laser annealing of the backside contact (with Cornell)
  - Tested interconnections
    - Cu-Cu thermo-compression
    - Cu-Sn interconnects
    - Ziptronix Oxide Direct Bond Interconnect (DBI)

- Other projects that use 3D paradigm:
  - Silicon on Insulator (SOI) Mambo imaging chip with KEK/OKI
  - Large area arrays with active tiles
  - 3D version of Silicon Photomultiplier
  - VIPRAM Stacked Associative Memory for fast triggering

→Significant difficulties encountered at every step

3D-IC Techniques

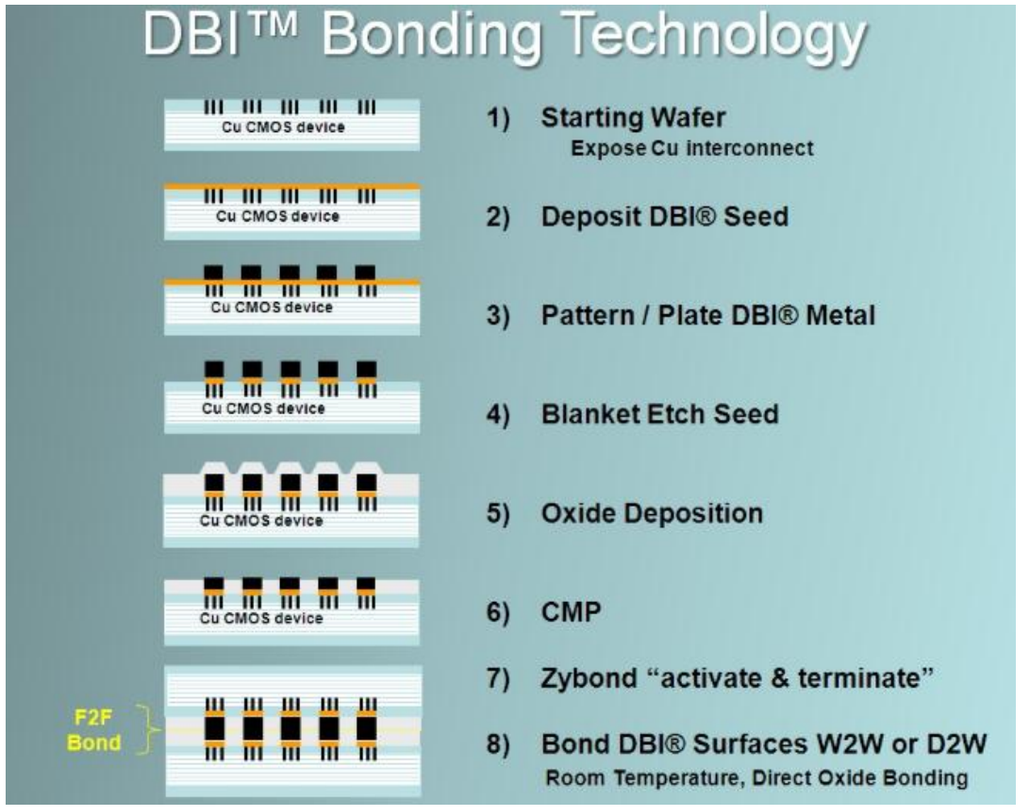
- Technology first explored at MIT-LL
- Not only good for electronic ROCs but also for attaching detectors to readouts
- Through Silicon Vias (TSV) for vertical wafer/chip connectivity - Vias at micron level
- Bonding: Oxide, polymer, metal, or adhesive strengthened (Wafer-Wafer, Chip-Wafer, Chip-Chip)
- Wafer thinning: aggressive and precise
- Back-side metallization and patterning

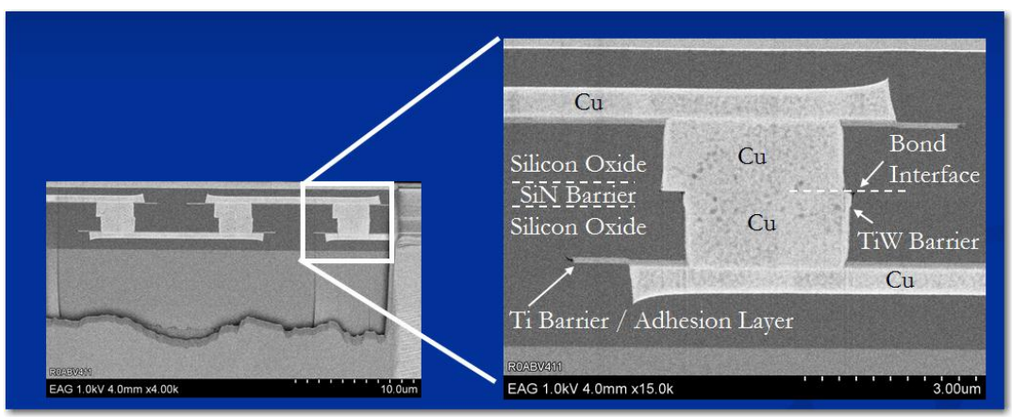


MIT-LL
3D-IC process
FDSOI oxide-oxide bonding

Oxide Bonding of Sensors and Chips

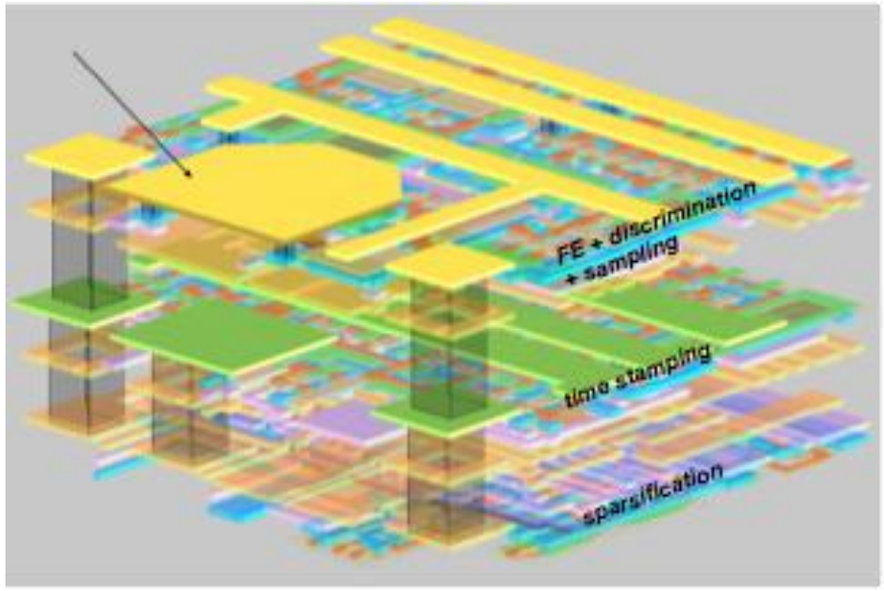
- Ziptronix Direct Bond Interconnect (DBI) is based on formation of oxide bonds between activated SiO_2 surfaces with integrated metal:
  - Silicon oxide/oxide initial bond at room temp. (strengthens with 350 deg cure)
  - Replaces bump bonding
  - Uses standard IC processes – chemical-mechanical polish and metalization
  - Chip to wafer or wafer to wafer process
  - Creates a solid piece of material that allows bonded wafers to be aggressively thinned
  - ROICs can be placed onto sensor wafers with <10 µm gaps - full coverage detector planes
  - ROICs can be placed with automated pick and place machines before thermal processing - much simpler than the thermal cycle needed by solder bumps

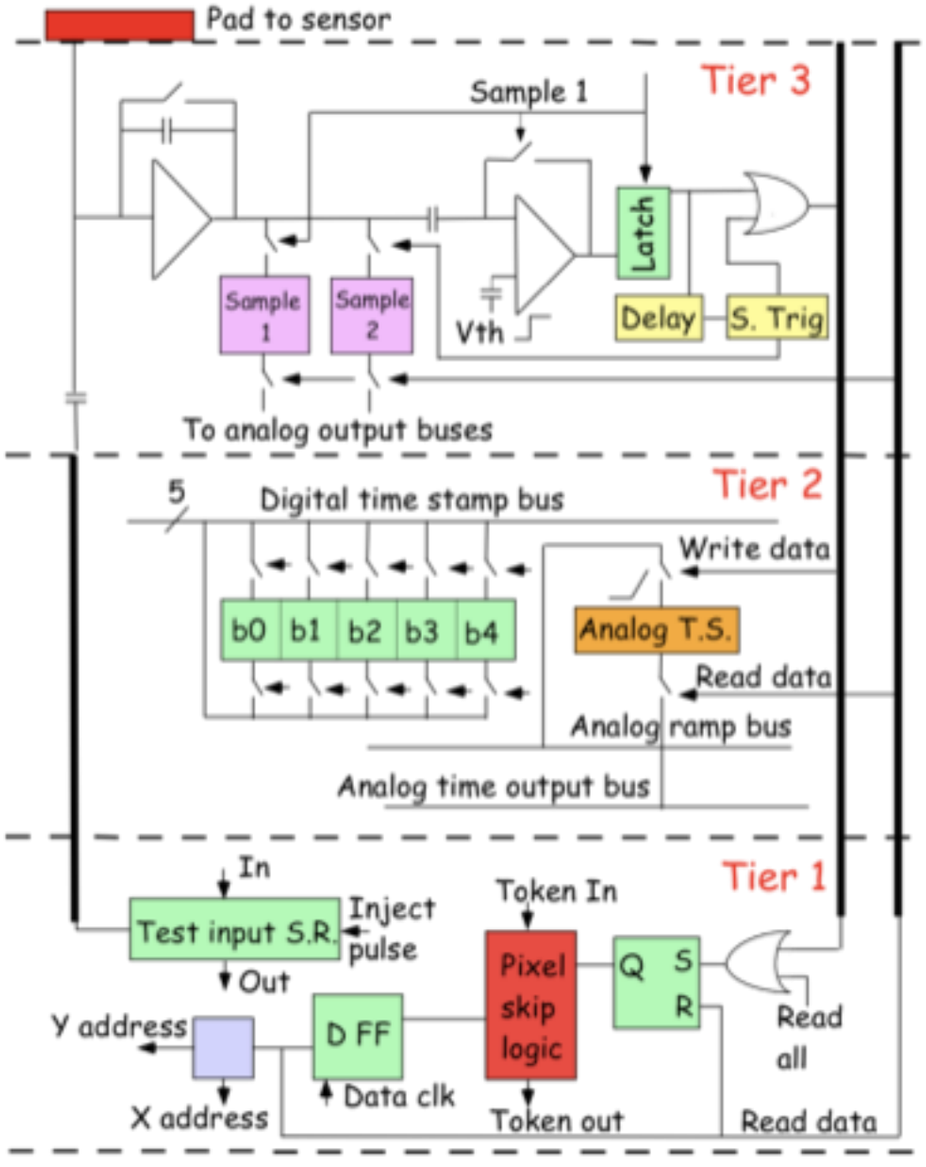




“VIP” = Vertically Integrated Pixels - 3D Chip for ILC Vertex

- Goal - demonstrate ability to implement a complex pixel design with all required ILC properties in a 20 micron square pixel
- Previous technologies limited to very simple circuitry or large pixels
- 3D chip design in MIT Lincoln Labs 0.18 um SOI process.
- Chip designed for ILC Vertex
  - Low power front end
  - Digital and and analog time stamp
  - Sparse scan readout
  - 24 micron pitch or better
- Initial submission had low yield and marginal functionality due to MIT-LL process issues.
- Second submission with a more conservative design worked well. Converted to 0.13 micron CMOS for 3D Tezzaron run VIP2b

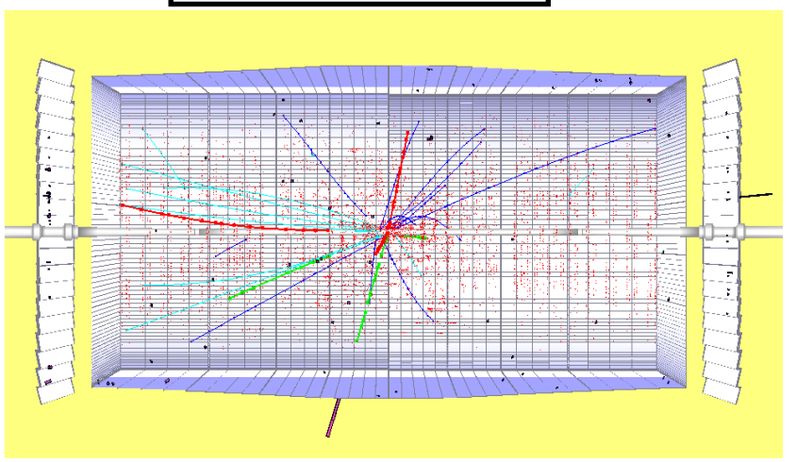




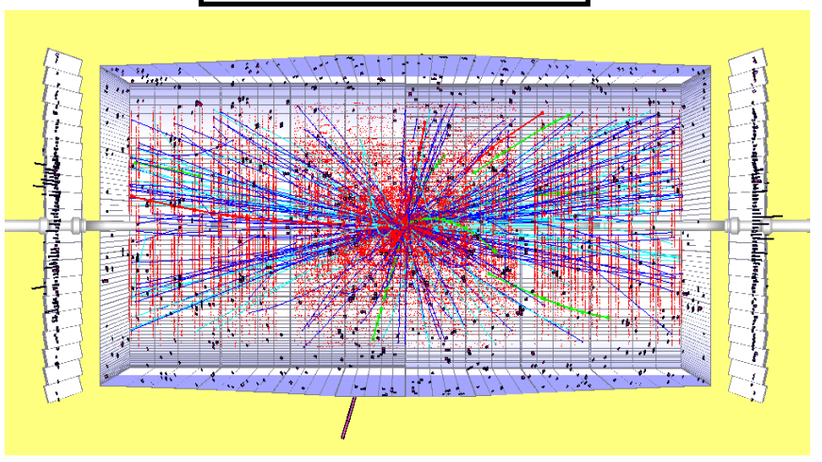
Another Application of 3D ASIC Circuits – High Luminosity LHC

H→ZZ → μμee for different luminosities in CMS:

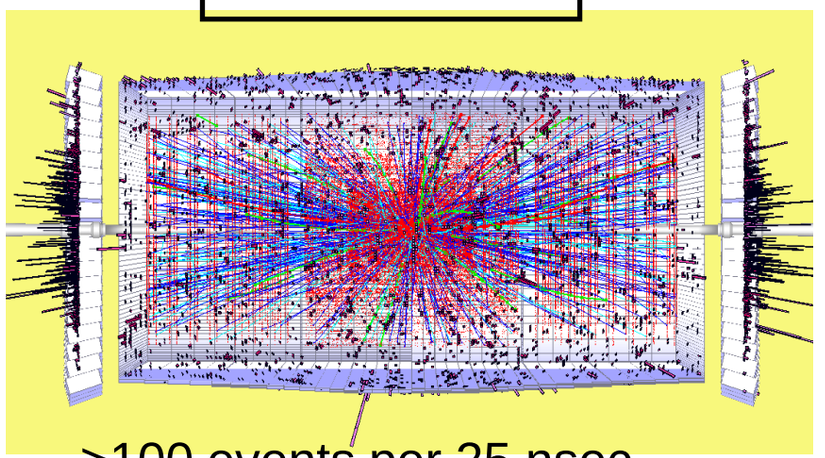
10^{33} cm^{-2}s^{-1}



10^{34} cm^{-2}s^{-1}



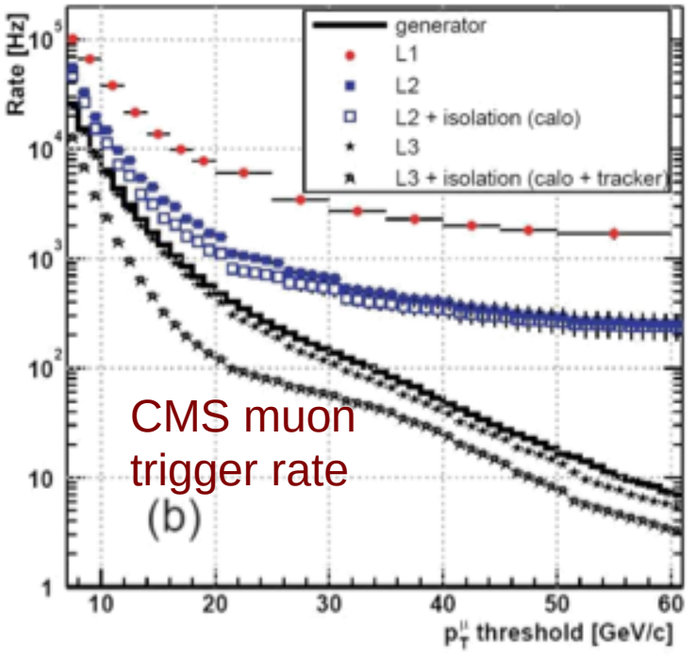
10^{35} cm^{-2}s^{-1}



>100 events per 25 nsec beam crossing !

Complexity is handled at higher (and slower) trigger levels with software on CPUs. This works with low luminosity, but will be compromised at the HL-LHC. Raising threshold does not significantly help.

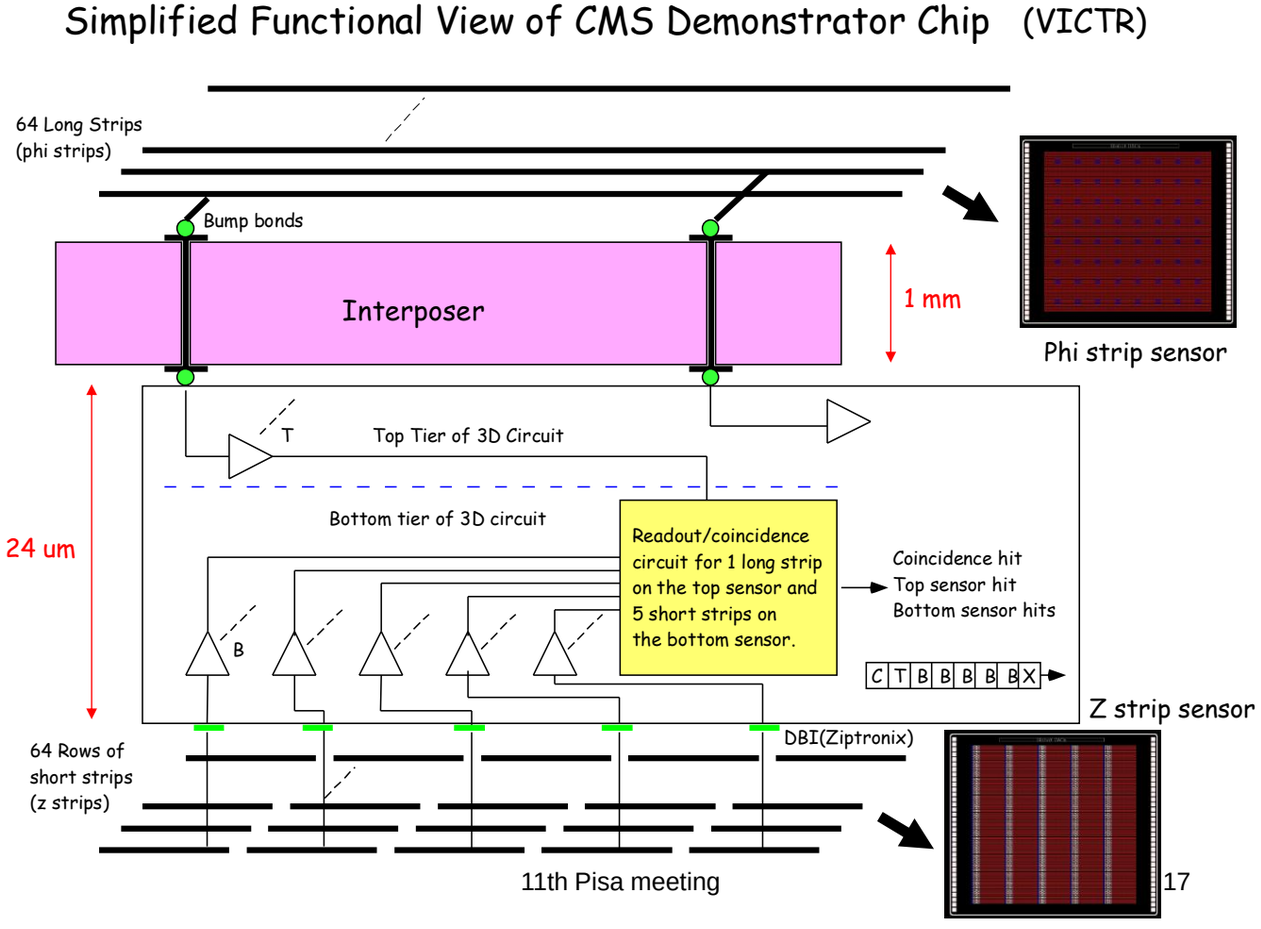
Several avenues for solving this (and other high speed) problems are being worked on in the 3D ASIC group at Fermilab



“VICTR” = Vertically Integrated Chip Tracker - an LHC track trigger at Level 1

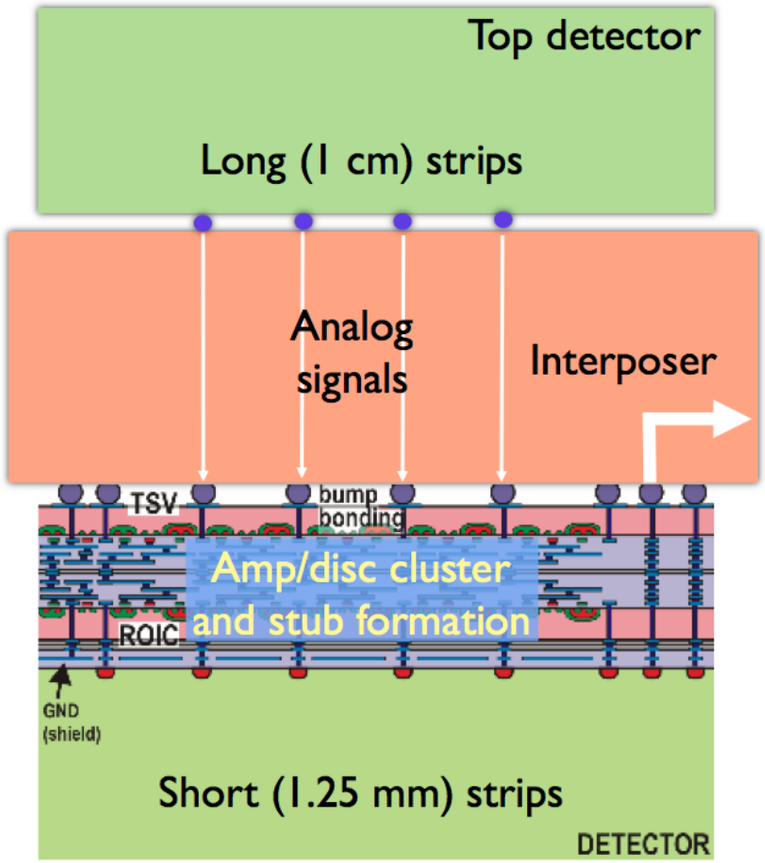
- Must be much faster than a L2 trigger. This is especially hard for a silicon-based tracker with potentially huge data volumes

  Principles:
  - The trigger must be designed into the tracker geometry from the start
  - Good Z resolution to reduce background event candidates. Minimize the tracks used for isolation.
  - Design the system geometry so all operations are “local” - minimize data transmission. Use hierarchical design to limit overall data flow
  - Limit rate at the front end by using correlated layers (x20 rate reduction)



- Serial RO of all top & bottom strips in coincidence, feeding into a 3D type of ASIC in the middle.
- Uses slightly modified front-end from FEI4 (ATLAS) with a custom serial RO architecture
- Low-power, with in-situ processing.

3D Module Data Flow in VICTR



Top sensor analog information flows through interposer to IC mounted on bottom

Long strips on top provide r-phi to minimize number of interposer connections

Short strips on the bottom provide Z resolution

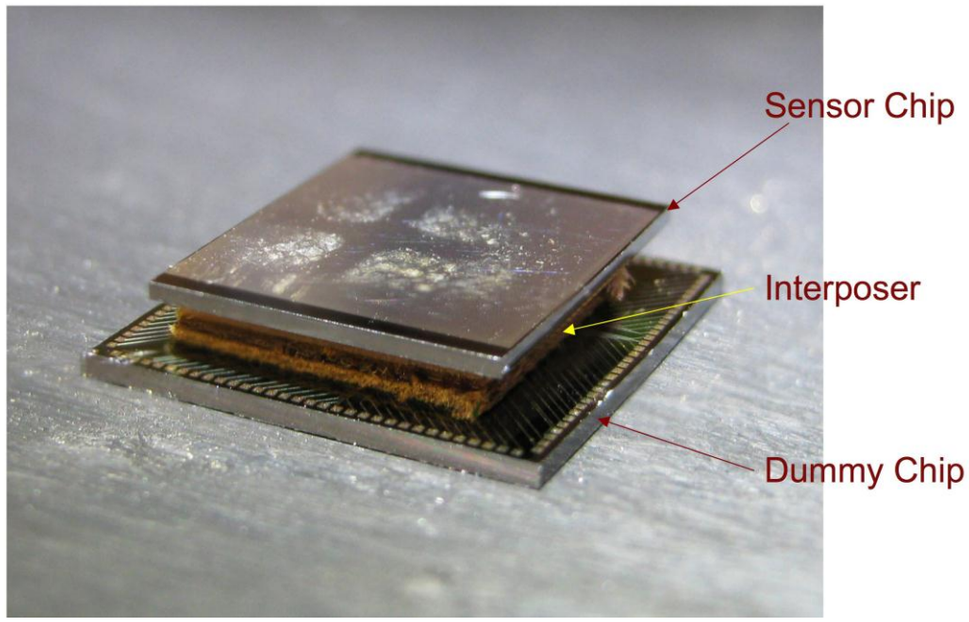
ROIC amplifies, discriminates. forms stubs and manages pipeline

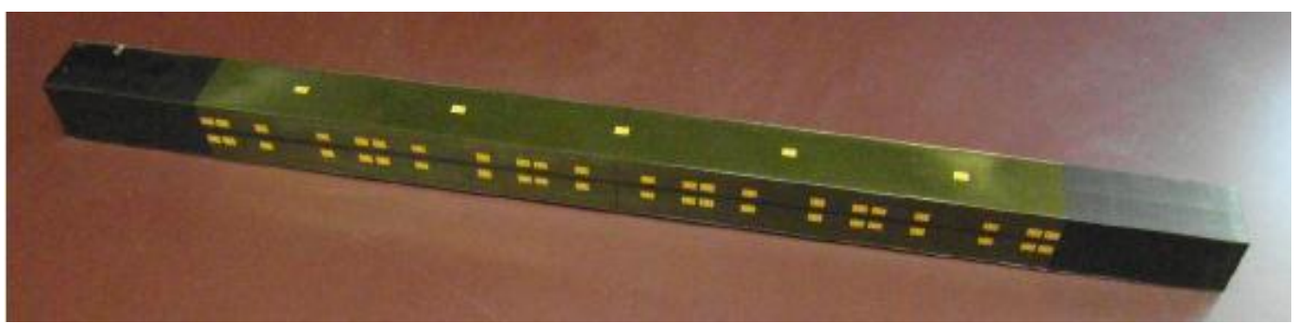
ROC sees signals from top and bottom sensors - all correlations are local

Collaborating with: LBNL, BNL, UC Davis, Cornell, AllVia, Tezzaron, Ziptronix, VTT

Double Stack Bonding

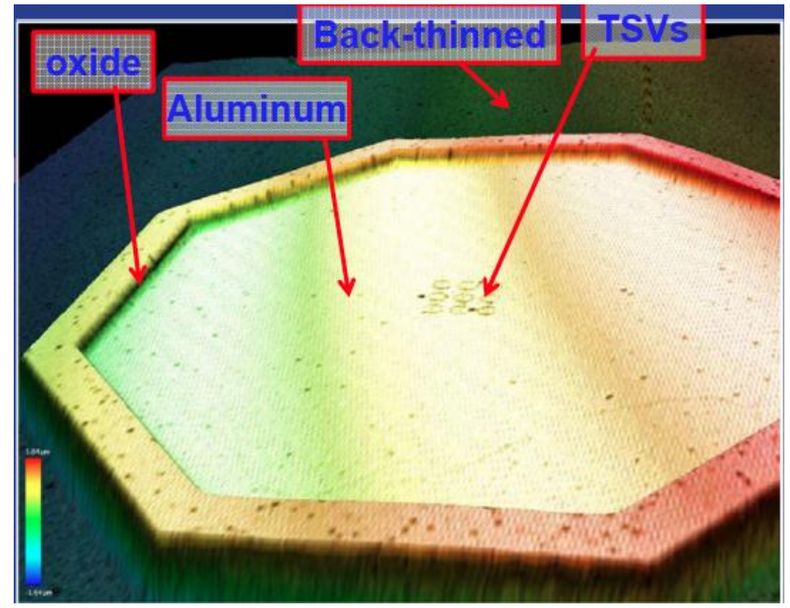
Bonded to sensor chips from BNL

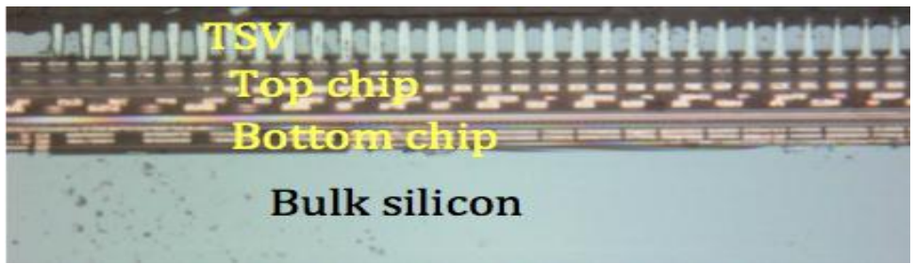


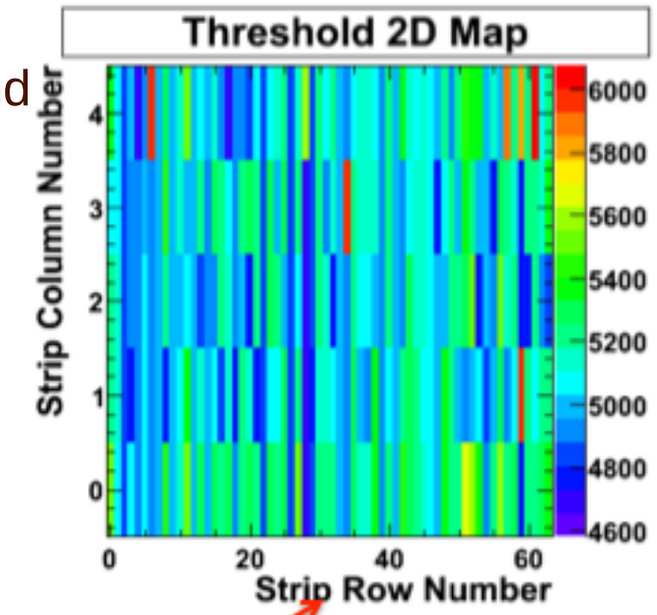


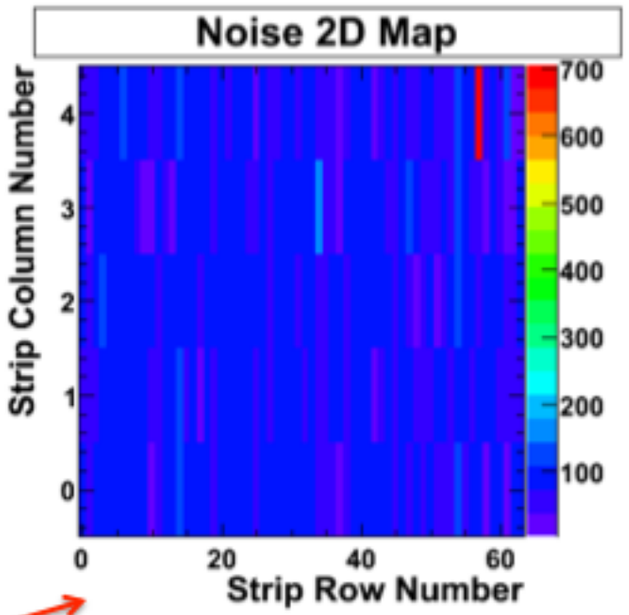
VICTR Test Results

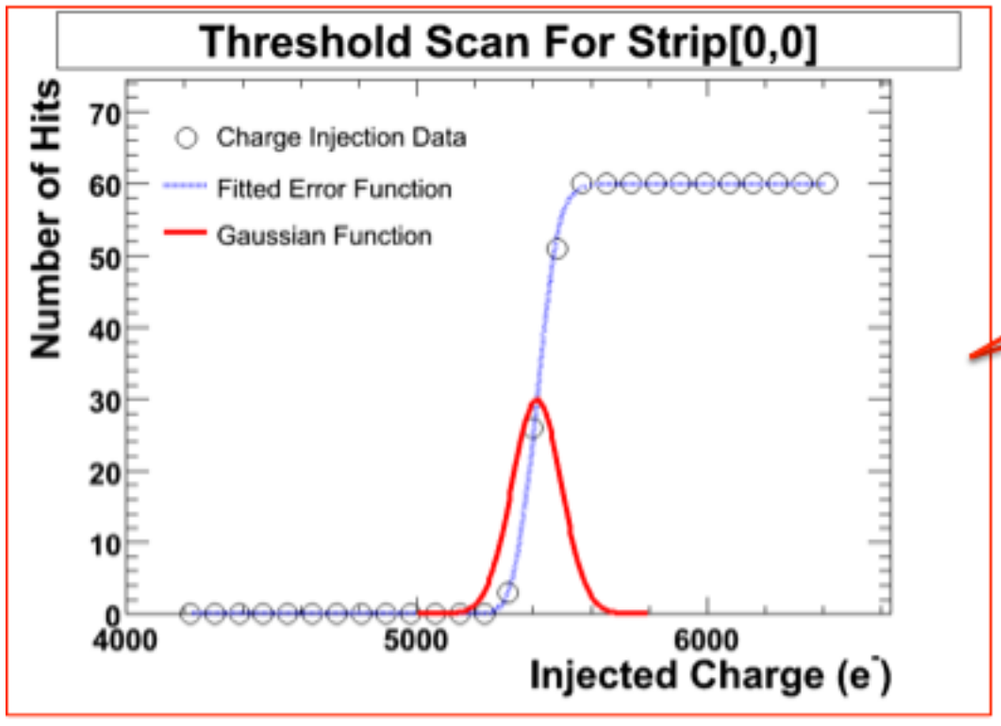
- Initial alignment problems in fabrication
- We now have well-aligned functioning chips from wafers delivered in June
- Good thinning and TSV contact and backside metalization
- Tests using NI flex rio systems give good threshold tuning and noise performance and show communication between layers

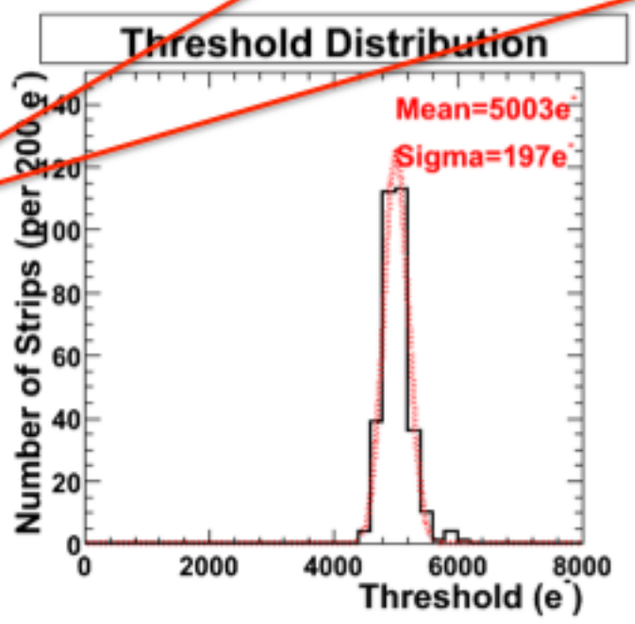


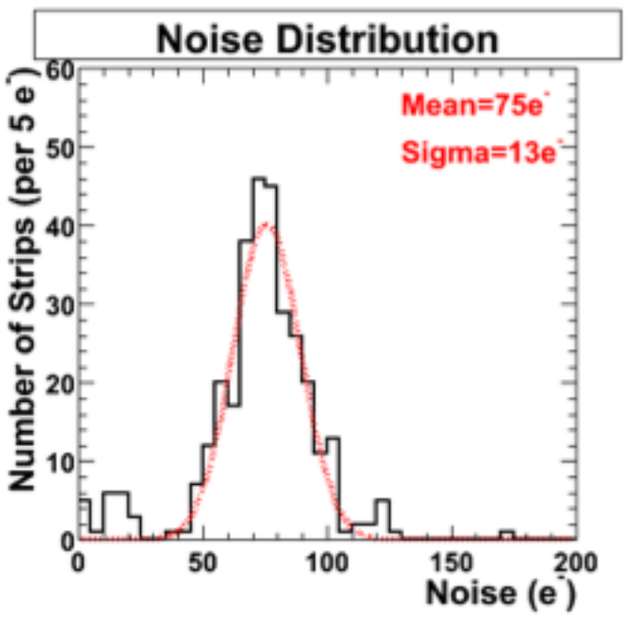






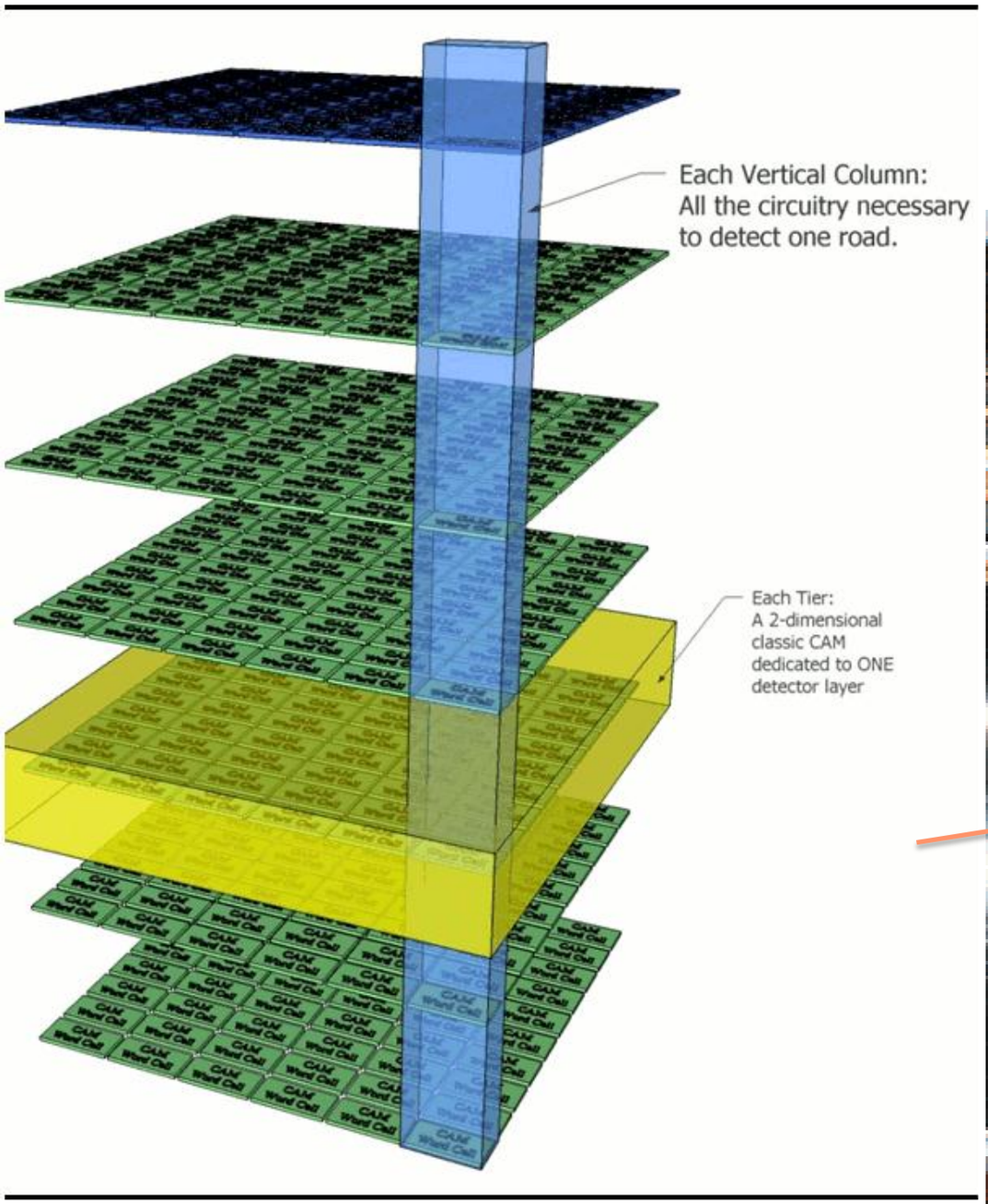




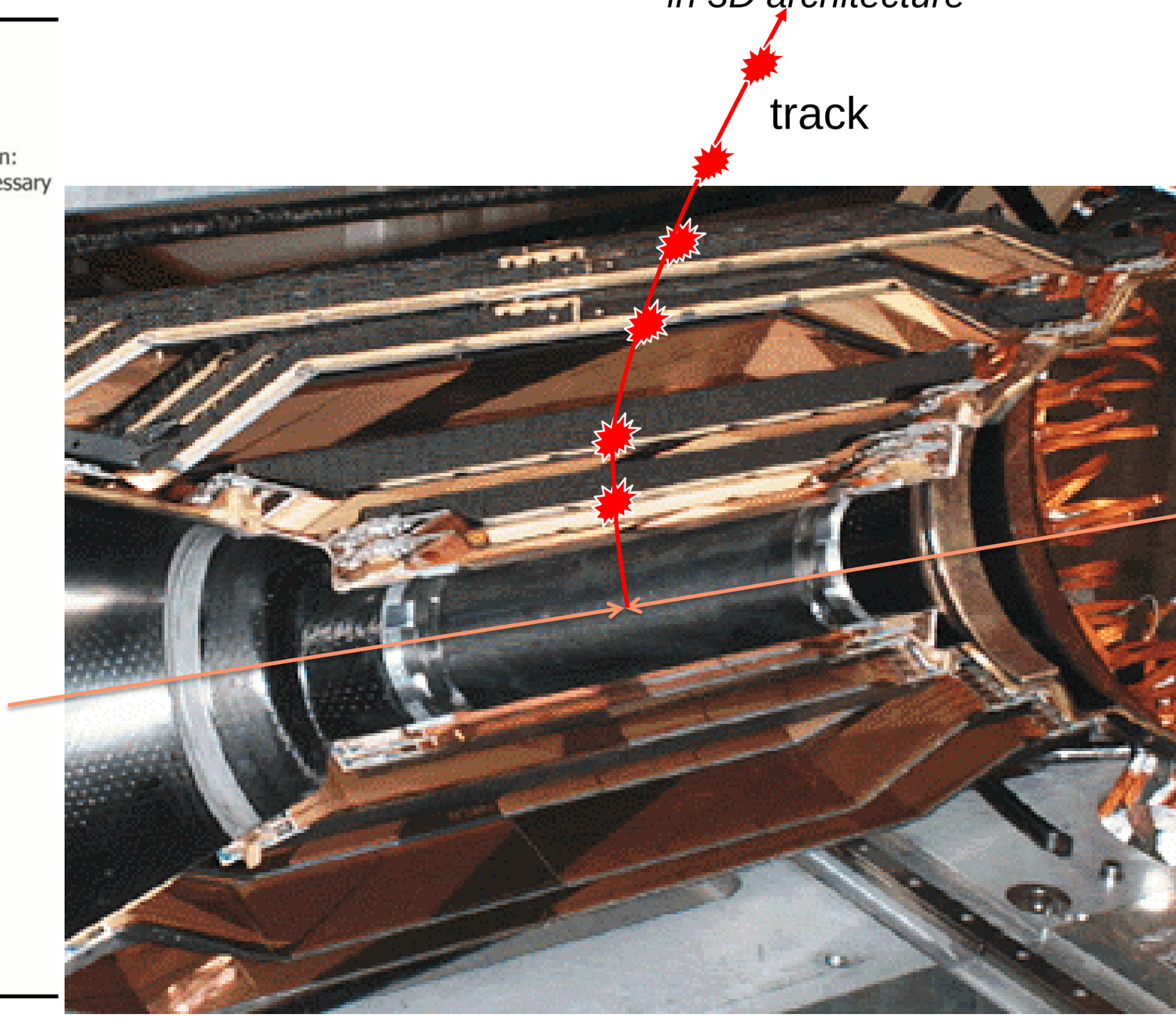


"VIPRAM" = Vertically Integrated Pattern Recognition Associative Memory

Using 'Content Adressable Memory' (CAM) technology for use in collider detector triggering



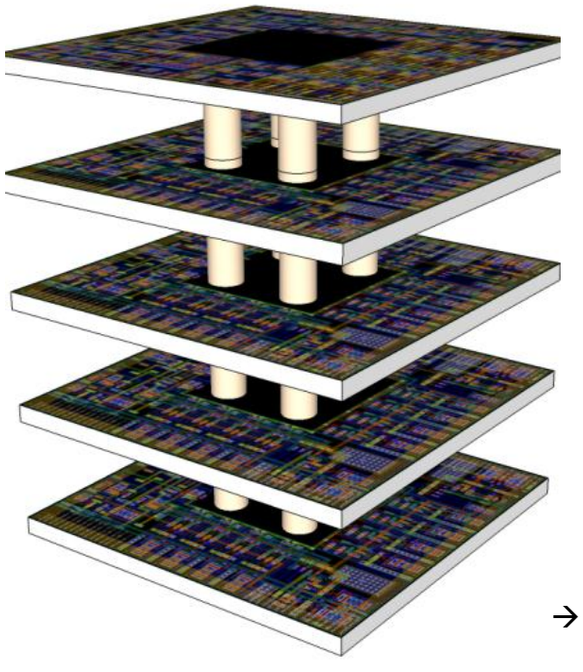
Pattern recognition for tracking is naturally a task in 3D architecture



First VIPRAM prototype in 2D submitted in Dec. 2012

The challenge: Increase the patterns density by 2 orders of magnitude and increase the speed by a factor of >~ 3, while keeping the power consumption more or less the same

3D building blocks can be implemented and tested first in 2D:



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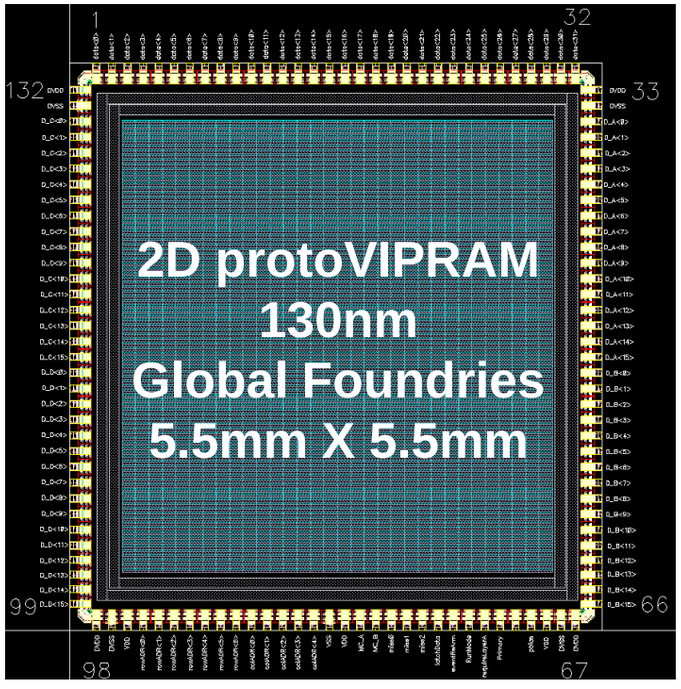
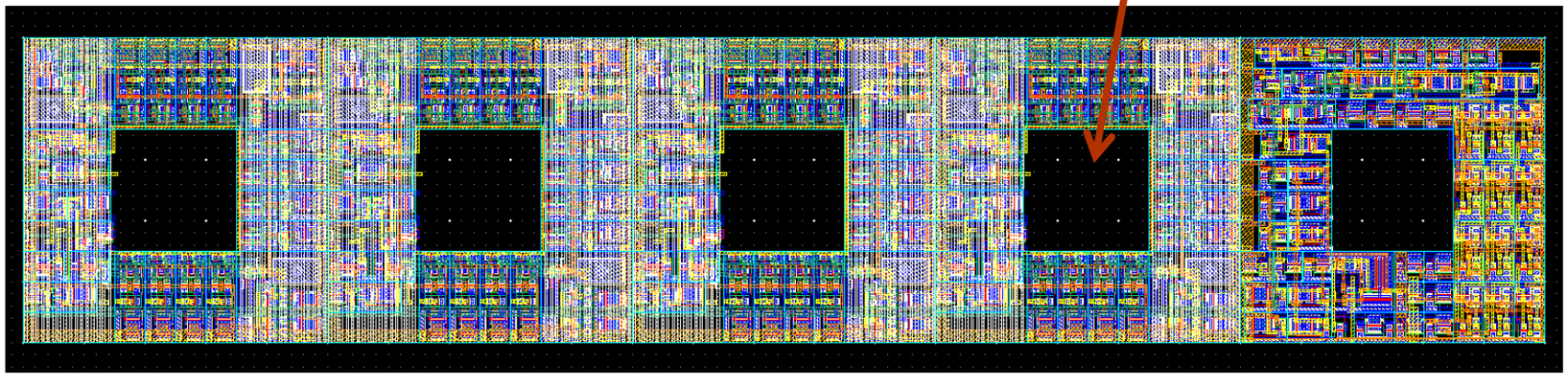


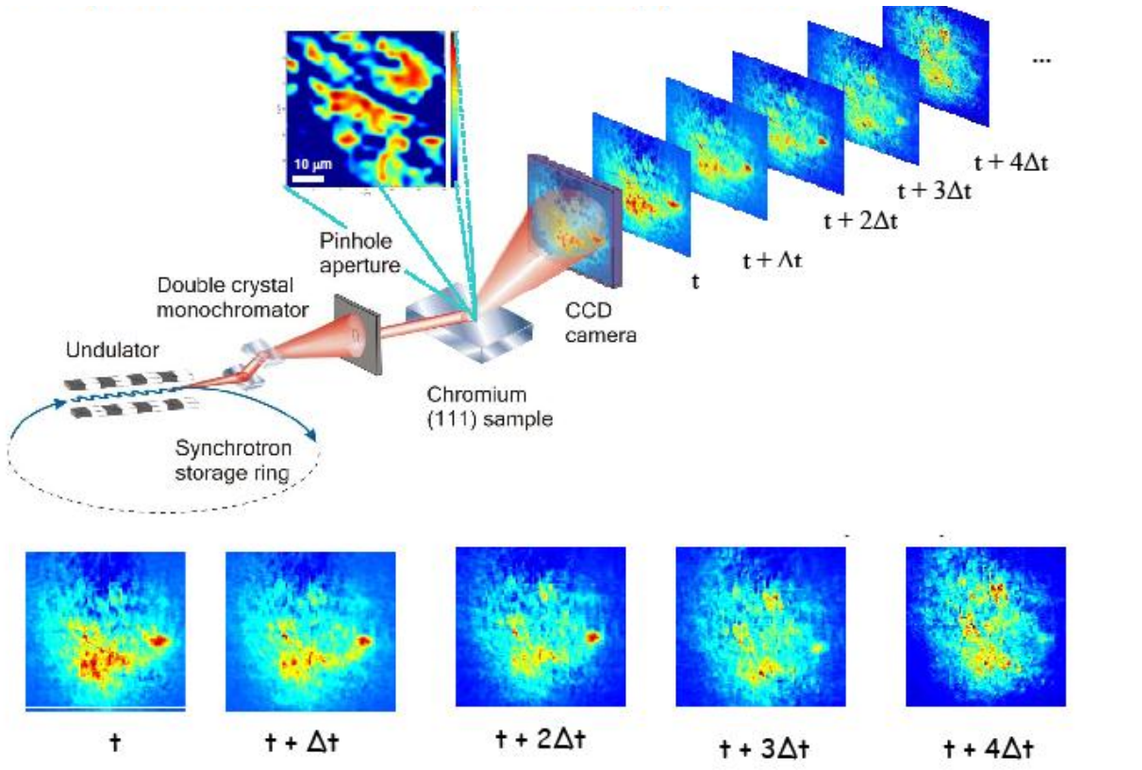
Keep this area open to incorporate 3D connections in future submission

CAM CAM CAM CAM ML

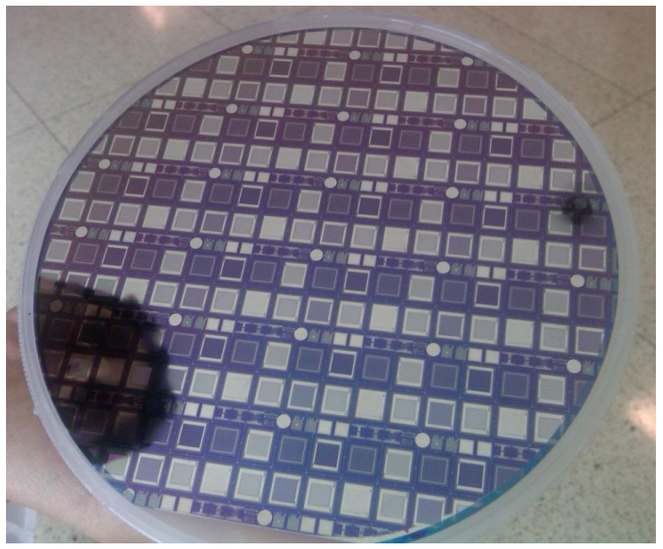


“VIPIC” = Vertically Integrated Photon Imaging Chip
A 3D ASIC for photon correlation

- Detector: Si 500 micron thick sensors for soft X-rays
- Low-power, time-of arrival and charge sharing corrected intelligent pixel detector
- Immediate application in producing science with light source
- no comparable device available (2D autocorrelation @ ~10 microsec or better)
- Develop practices and techniques applicable later in devices for HEP
- Intelligent pixels (raw data not sent; only on-detector inter-pixel processed data)



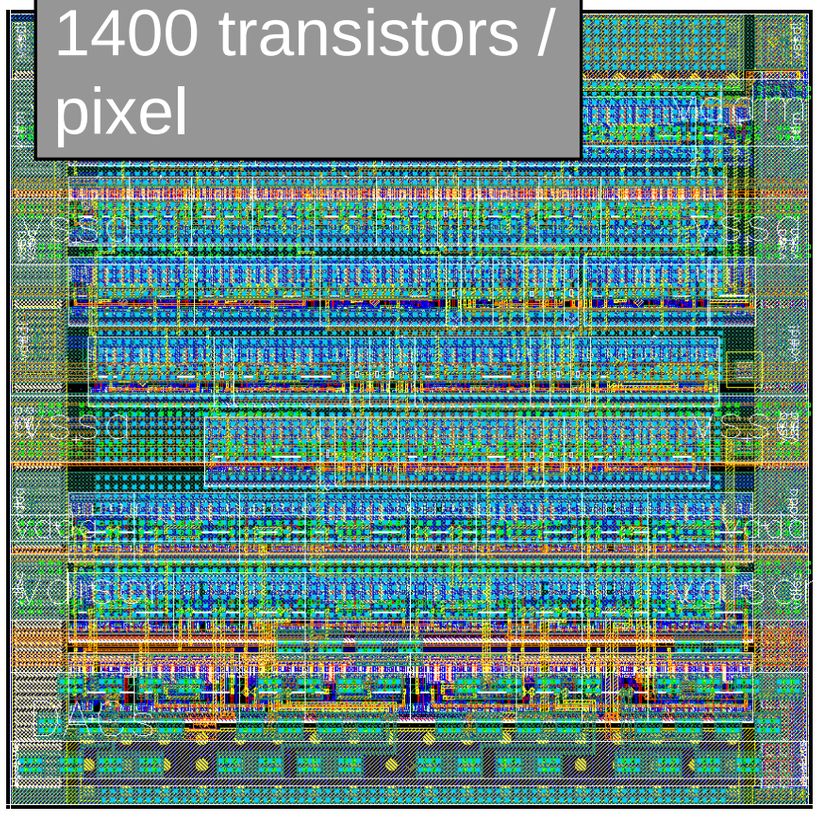
O. G. Shpyrko et al., *Nature* **447**, 68 (2007)



Sensor wafer for all 3D pixel chips
(designed at Fermilab fabbed at BNL),

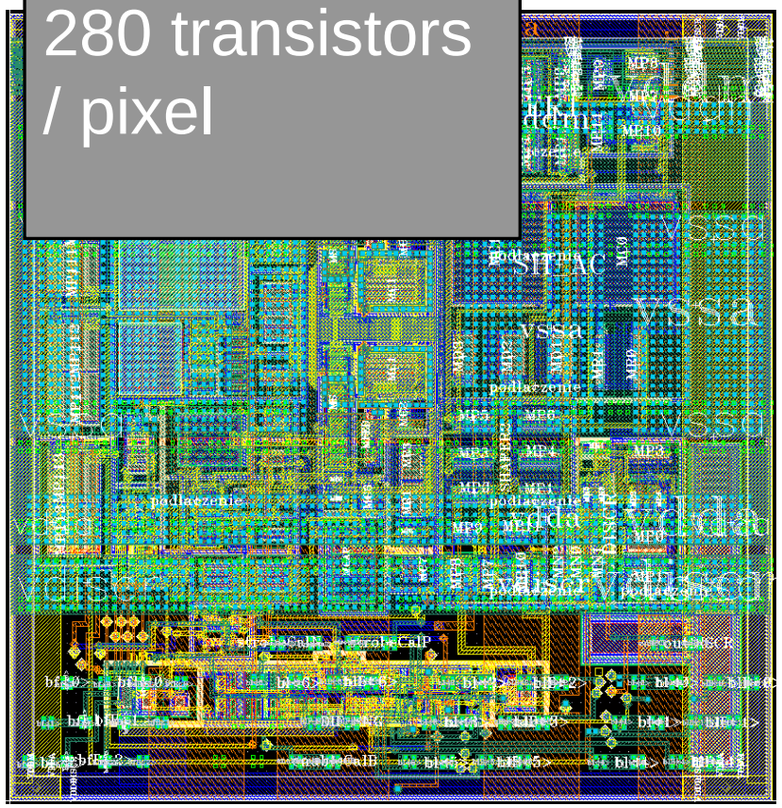
Fermilab designs for VIPIC

1400 transistors / pixel

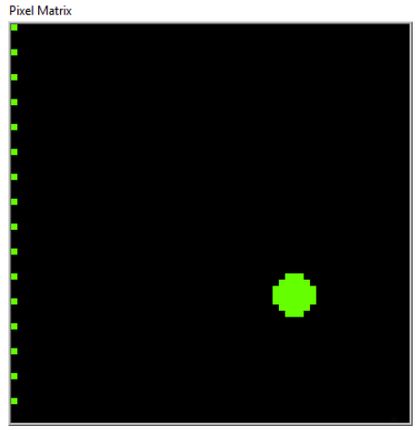


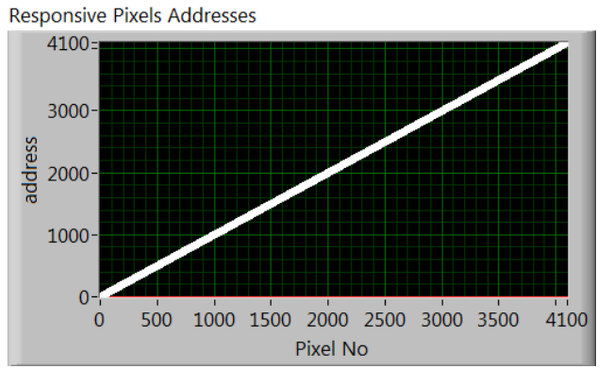
Digital part of pixel

280 transistors / pixel



Analog part of pixel





Chips have been tested with downloaded pattern and performed very well. Now waiting on sensor bonding

- Demonstrates ability to separate digital and analog layers, and bonding them together
- 64 × 64 array of 80 μm^2; shaping time τ_p=250 ns, power ~25 μW / analog pixel, noise <150 e^-
- Two dead-time-less modes of operation (64 × 64 matrix / in 16 sub-matrices of 4 × 64 pixels):
  1) timed readout of hits acquired at low occupancy (address and hit count) σ_t=10μs
  2) imaging – counting of events
- Sparsified readout with priority encoder circuit (hit pixel address readout only)

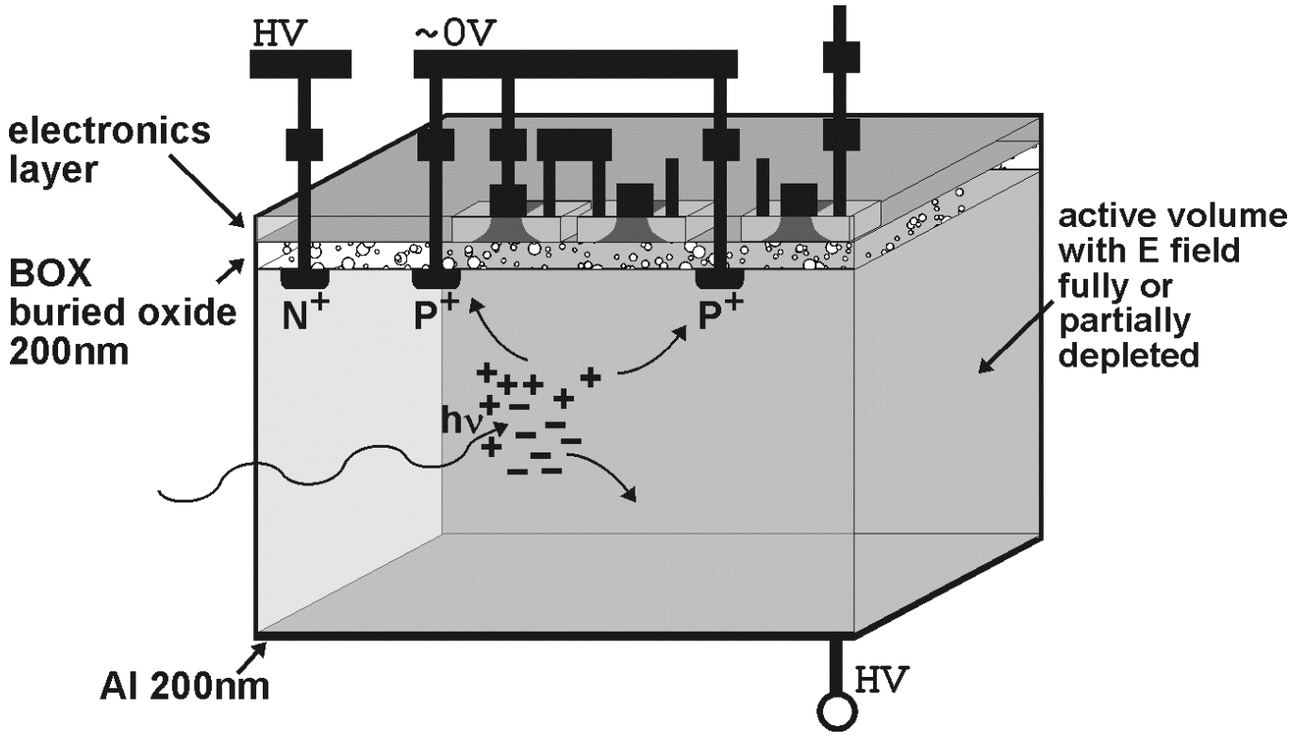
Silicon-on-Insulator (SOI) development

- SOI device contains a thin (200nm) silicon device layer mounted on a ‘handle’ wafer, separated by an insulating buried oxide layer. Handle wafer can a high resistivity detector.
  - First studied in 1993 by CERN/CPPM/IMEC
  - 2000s Crakow group in-house fabrication

- Fermilab collaborates with KEK and OKI/LAPIS (industrial partner) under a Japan-US agreement (MoU 2007) on monolithic SOI devices.

- Also working domestically with American Semiconductor through SBIR grant

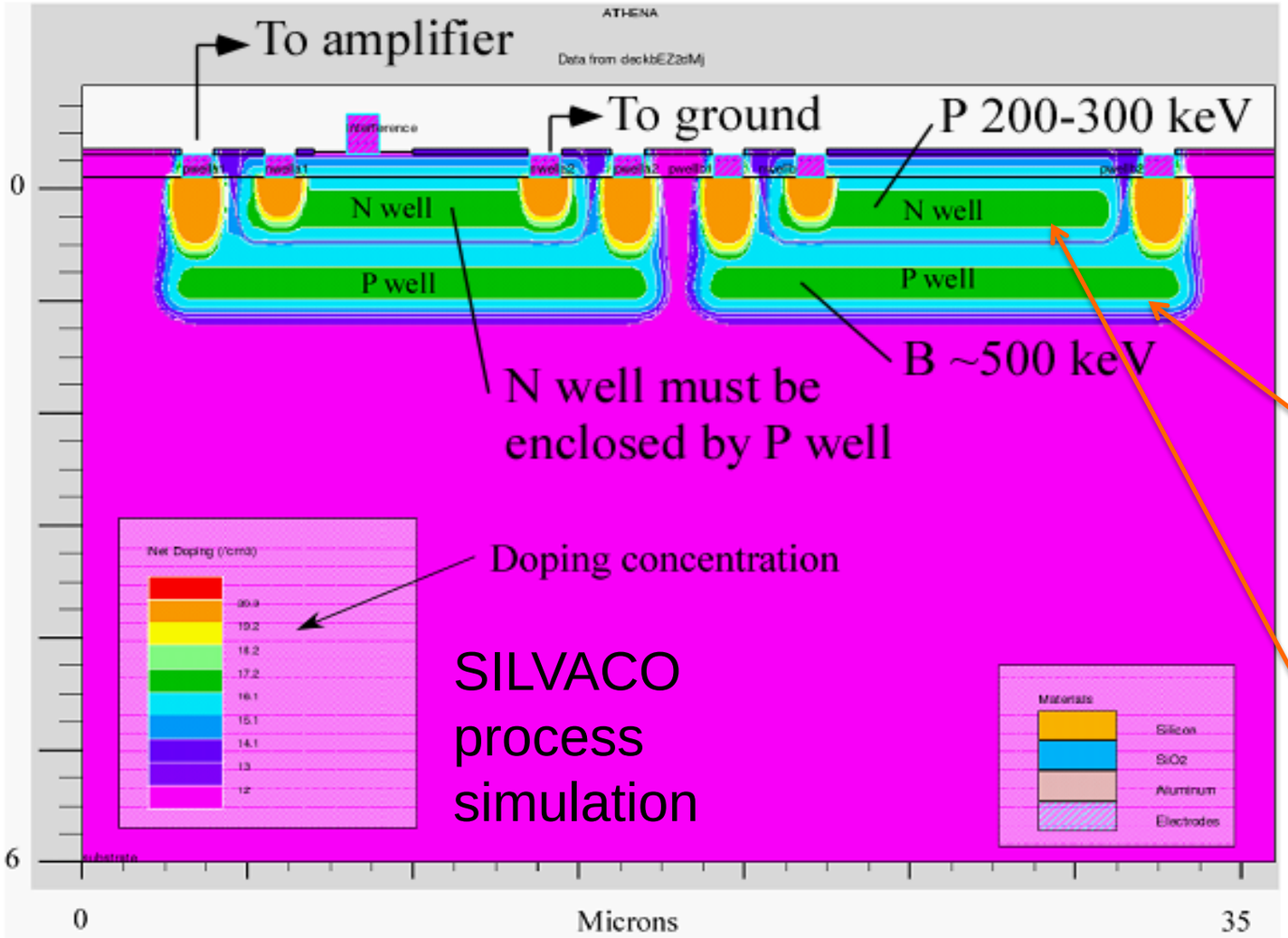
- Collaborate with Cornell:
  - device simulation
  - development of laser anneal process



Develop MAMBO = “Monolithic Active pixel Matrix with Binary cOunters”

SOI Pixels: Fermilab process improvement

- Triple role of shielding between the SOI electronics and detector layer:
  - to avoid back-gating in transistors (DC potential underneath the BOX shifts threshold of transistors),
  - to avoid injection of parasitic charges (from the SOI electronics to detector),
  - to avoid strong electric field in BOX (that results in accelerated radiation damage).



- ‘Nested well’ structures used to minimize the back-gate effects.

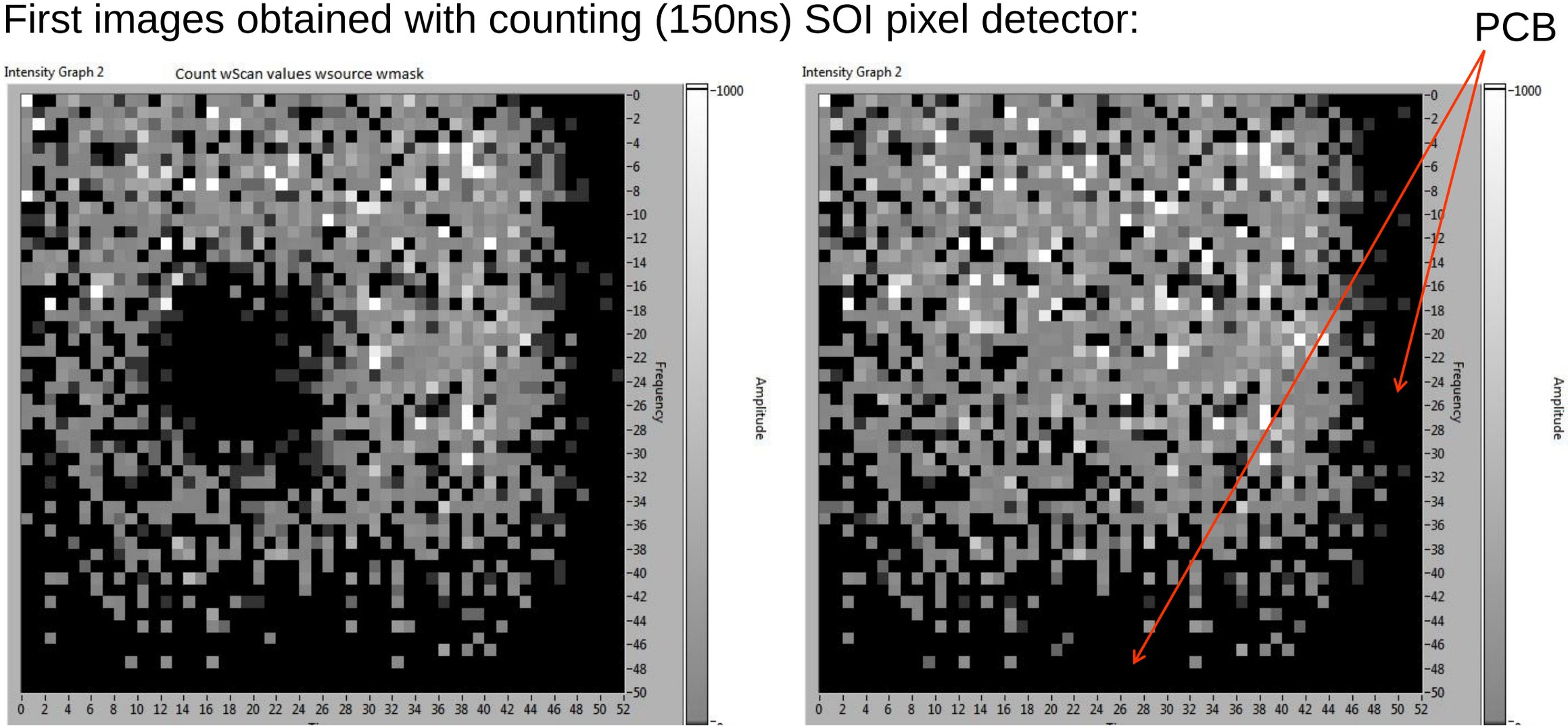
This well collects the charge carriers

This well separates digital circuits from sensor substrate and prevents back gating

SOI pixels: Results

– Starting in 2006, a sequence of counting MAMBO chips were developed, gradually improving the circuitry and understand better the technology

First images obtained with counting (150ns) SOI pixel detector:



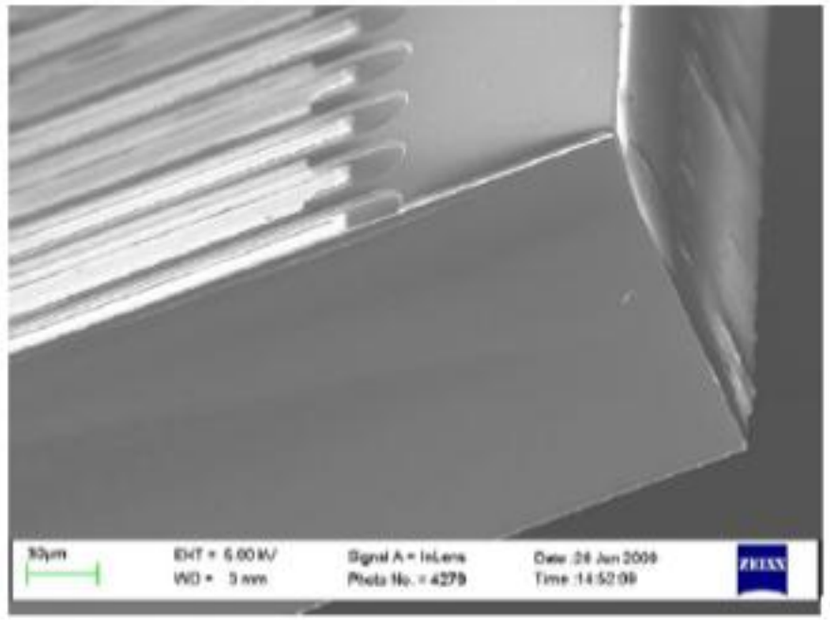
(1.9 × 1.9mm^2) square W mask

^{109}Cd source (22keV X-rays)
On MAMBO-5

flat field

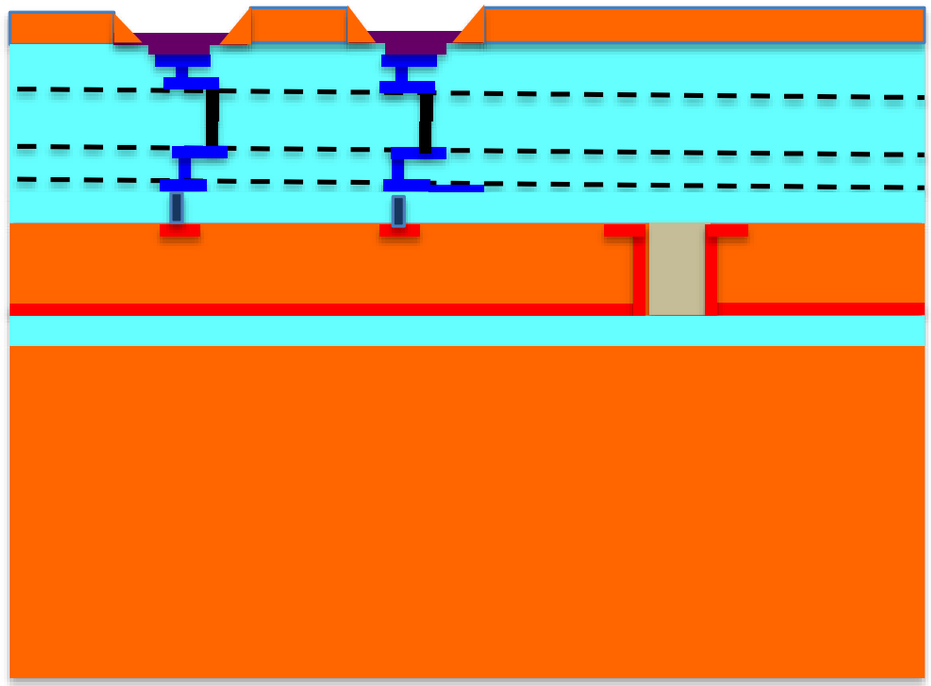
Active Edge Sensors

- An outgrowth of 3D detector development by Sherwood Parker and collaborators
- Deep reactive ion etch of silicon to create a nearly vertical trench with smooth edges avoids charge generation centers
- Filled with doped polysilicon or implanted and annealed to create a “backside” electrode
- UC Santa Cruz/Naval Research Lab is exploring an alternate process involving cleaving and atomic layer deposition



- The goal of this work is to combine active edge technology with 3D electronics and oxide bonding with through-silicon vias to produce fully active tiles.
- These tiles can be used to build large area pixelated arrays with good yield and low cost because the only bump bonds are large pitch backside interconnects.
- We are building a demonstration array including active edge sensors, oxide bonded wafers, and “damascene” dummy readout wafers
- Cornell is doing simulation work to support the design phase

VTT Active Edge Sensor



Summary

- 3D ASICs provide all the benefits you would expect from expanding into a new dimension:
  - Higher read out speed
  - Integrated analog and digital layers
  - Analysis or triggering decisions can be made at the detector level
  - Edgeless tiling of sensors enabled

- Fermilab has been involved in 3D ASIC development since 2006 and has been instrumental in developing accepted techniques since then

- We are concentrating now on developing specific applications, including new track triggering designs for HL-LHC, fast associated memory for L1 triggering, ILC type high pitch detector readout and time correlated counting detectors for X-ray science.

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- VICTR2 Chip - UC Santa Barbara, Brown U.
- CMS Pixel – CERN, Torino, Perugia
- Mechanics and Integration - UC Davis, Yale, Cornell, SLAC
- Active Edge/3D - Cornell, SLAC, Hawaii, Brown, UCSC, NRL
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