The TDCpix readout ASIC

A 75 ps resolution timing front-end for the NA62 Gigatracker hybrid pixel detector

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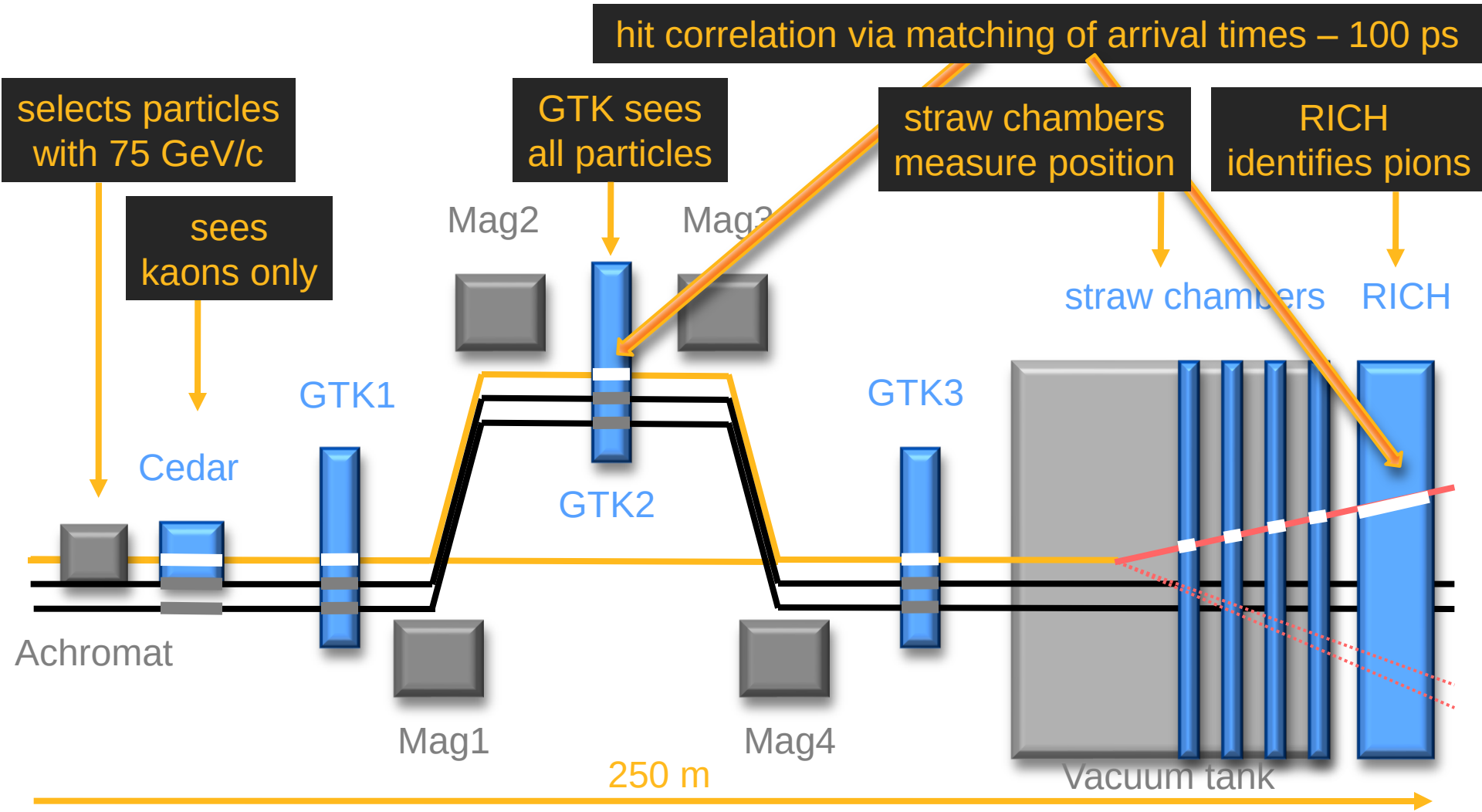
Outline

- NA62
- Specifications
- ASIC Architecture
- Why and Will

NA62 - Introduction

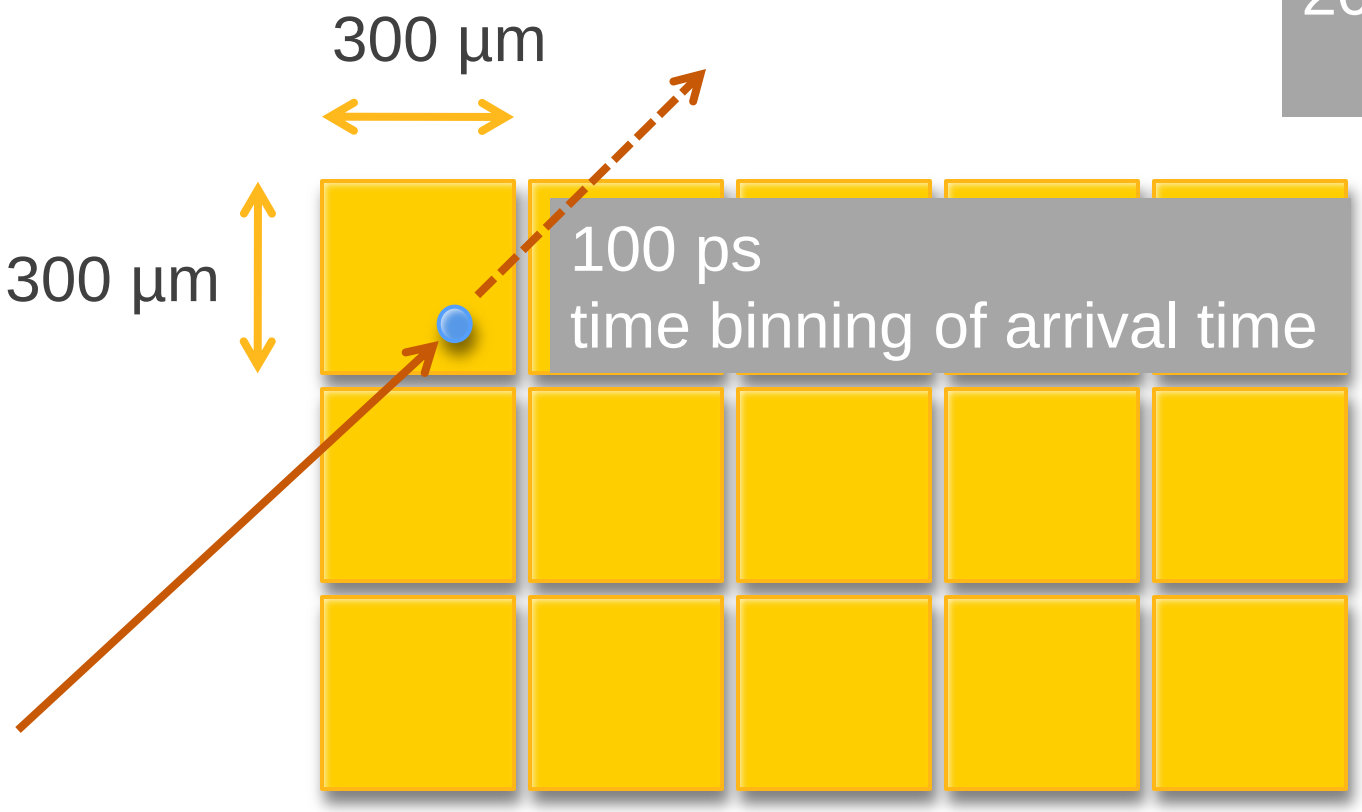
Experimental setup- NA62



beam: hadrons, only 6% kaons-> only 20% of charged kaon decay in the vacuum tank
-> out of which only 10^{-11} decays are of interest (pion-neutrino-antineutrino)

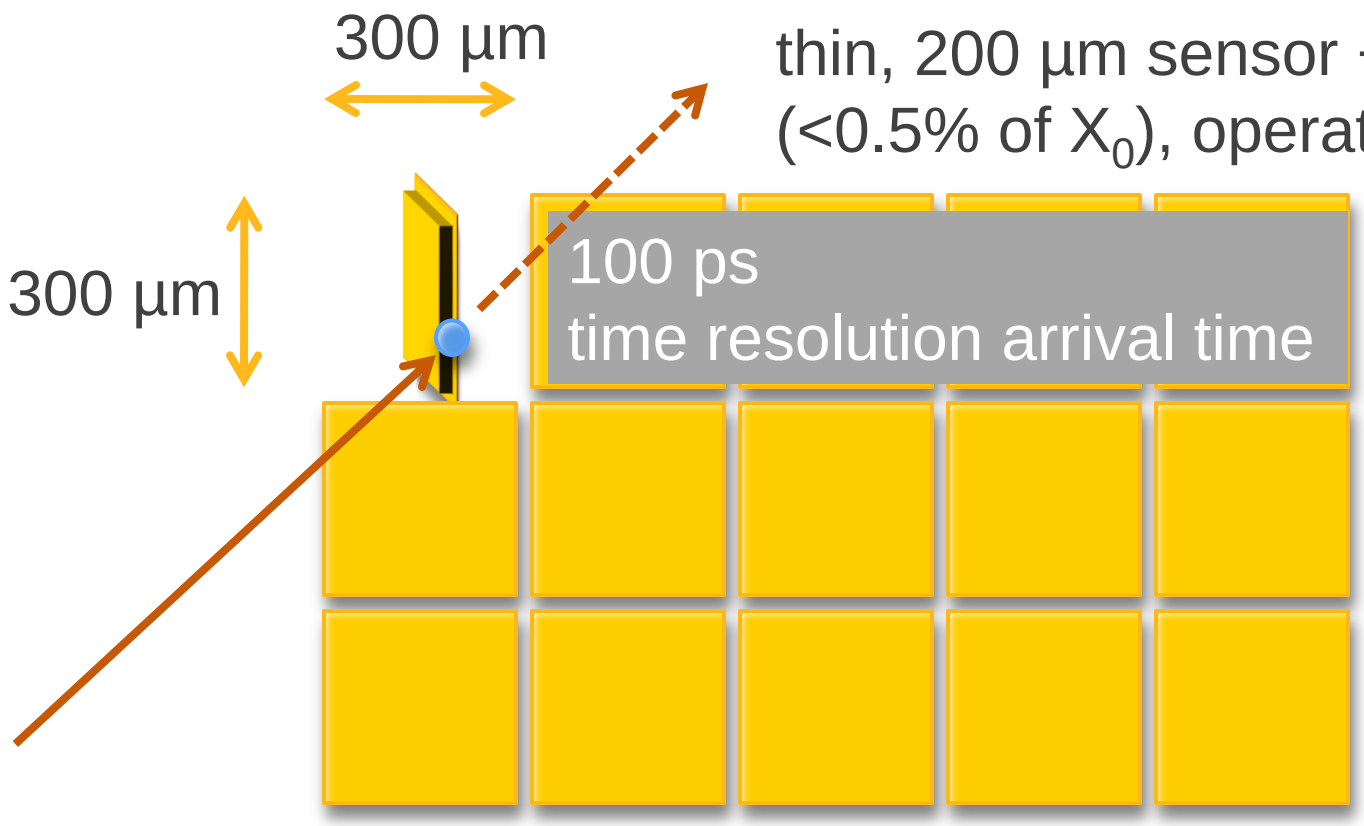
Experimental setup

200 ps per station



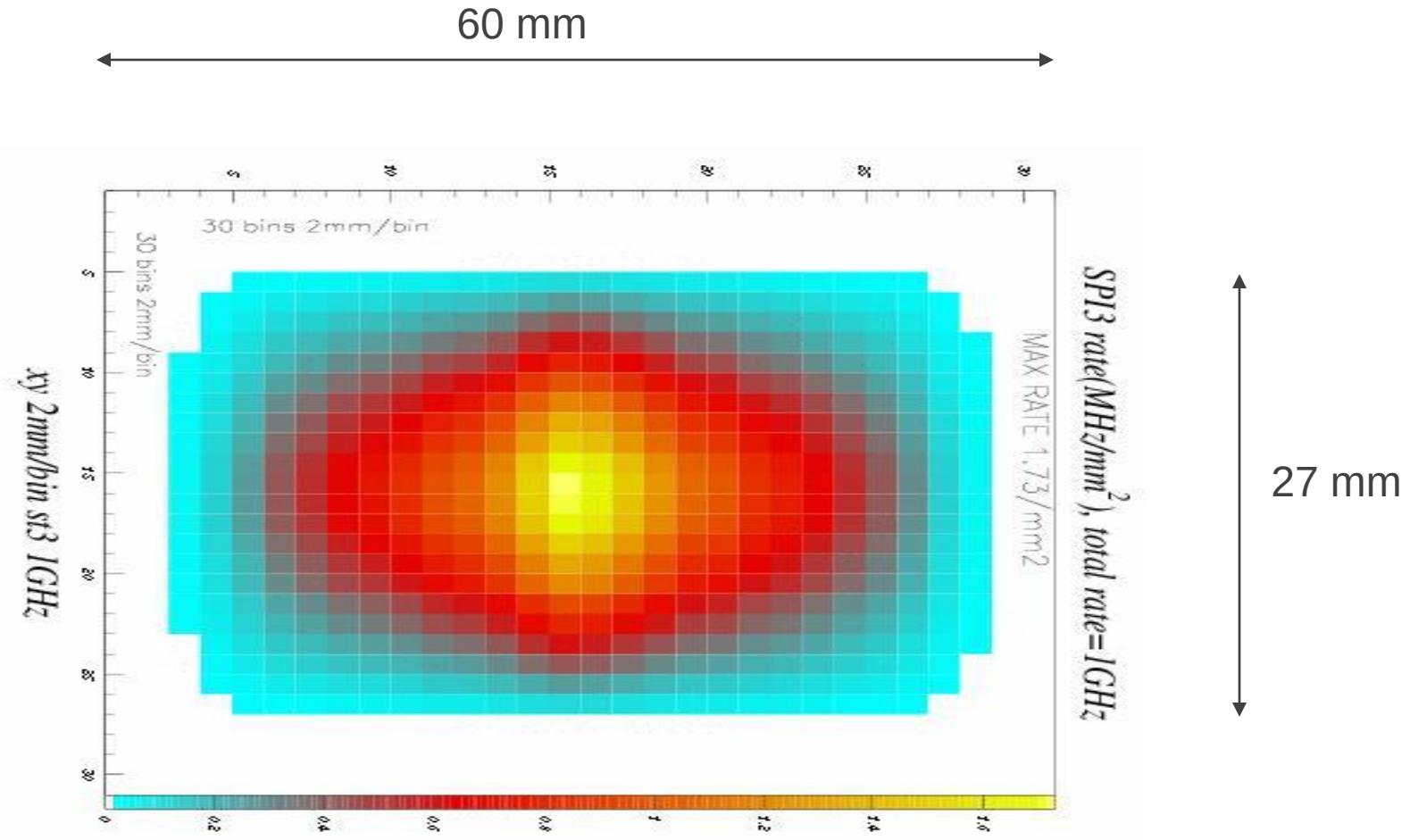
750 MHz particle rate

Experimental setup

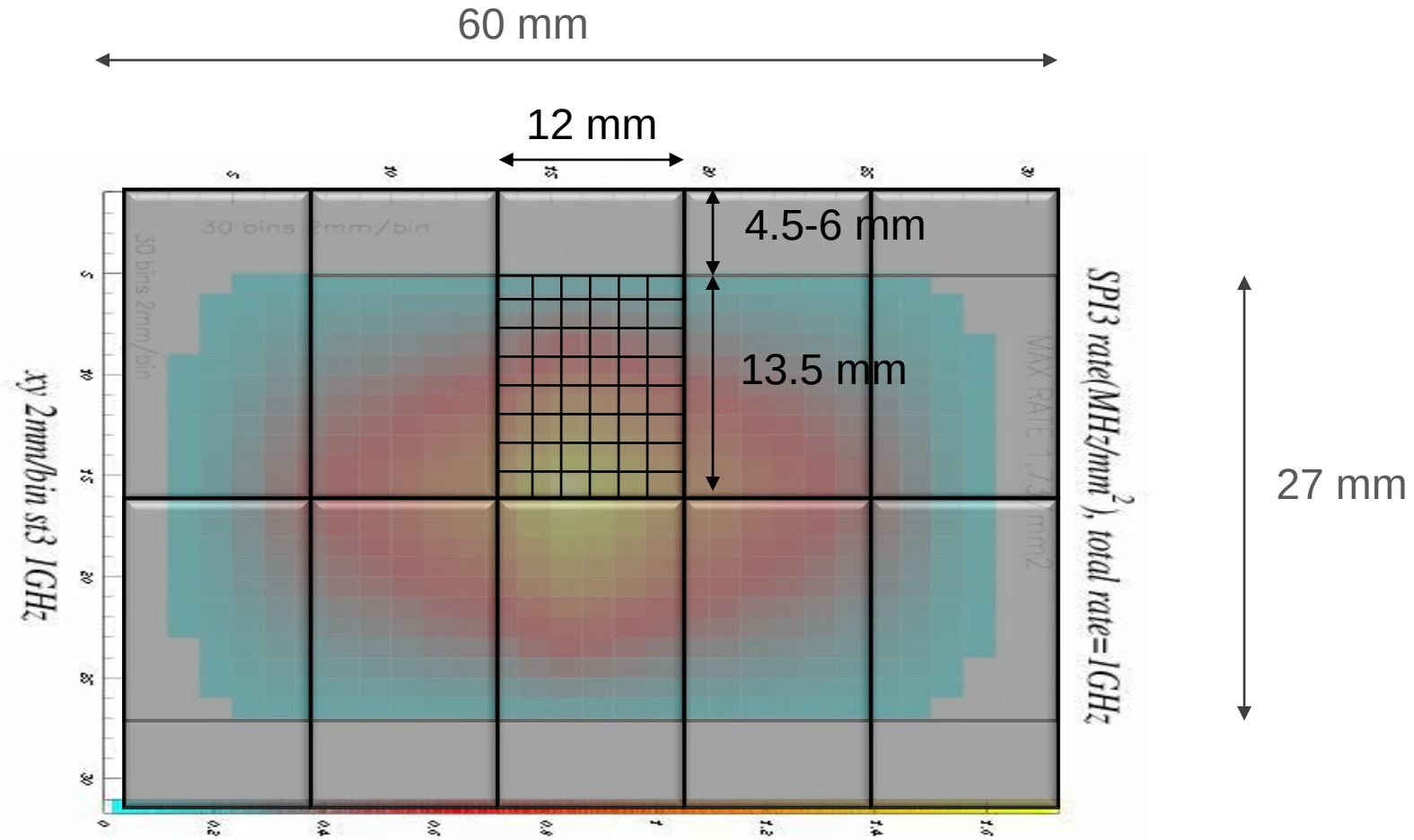


Beam & detector configuration

Beam profile

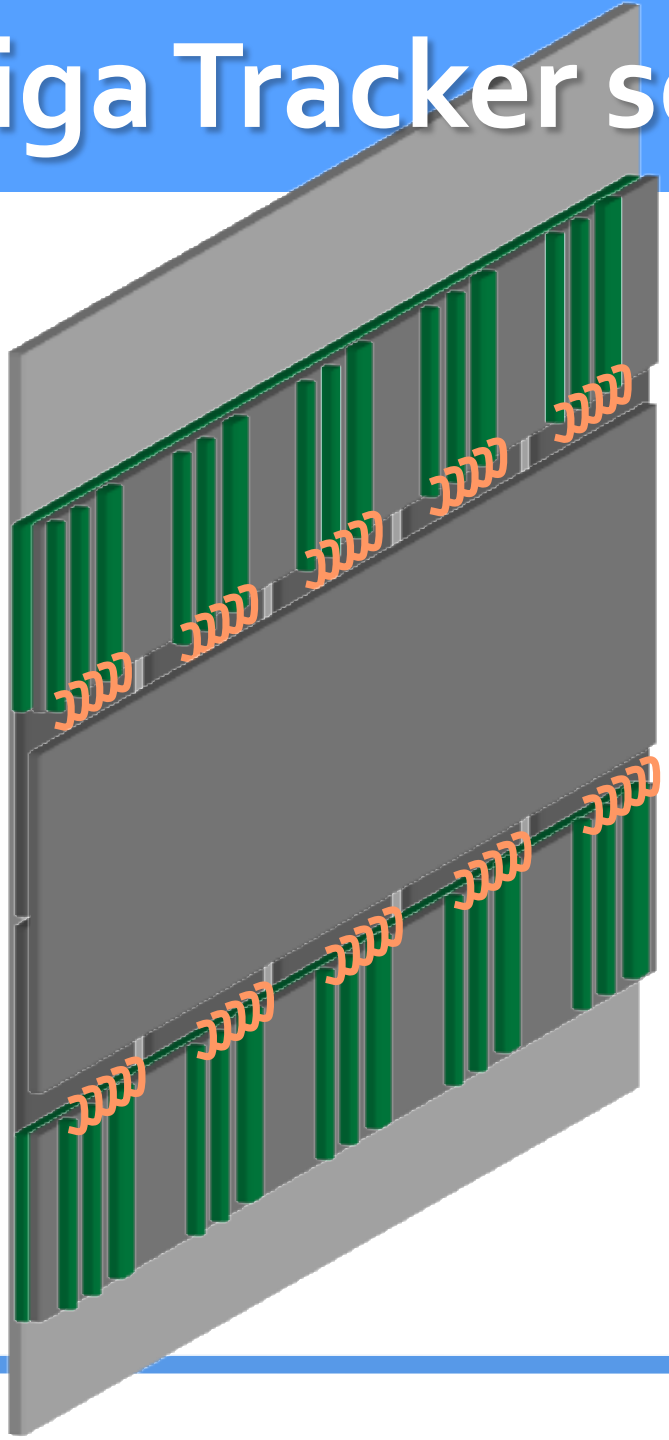


ASIC covering beam

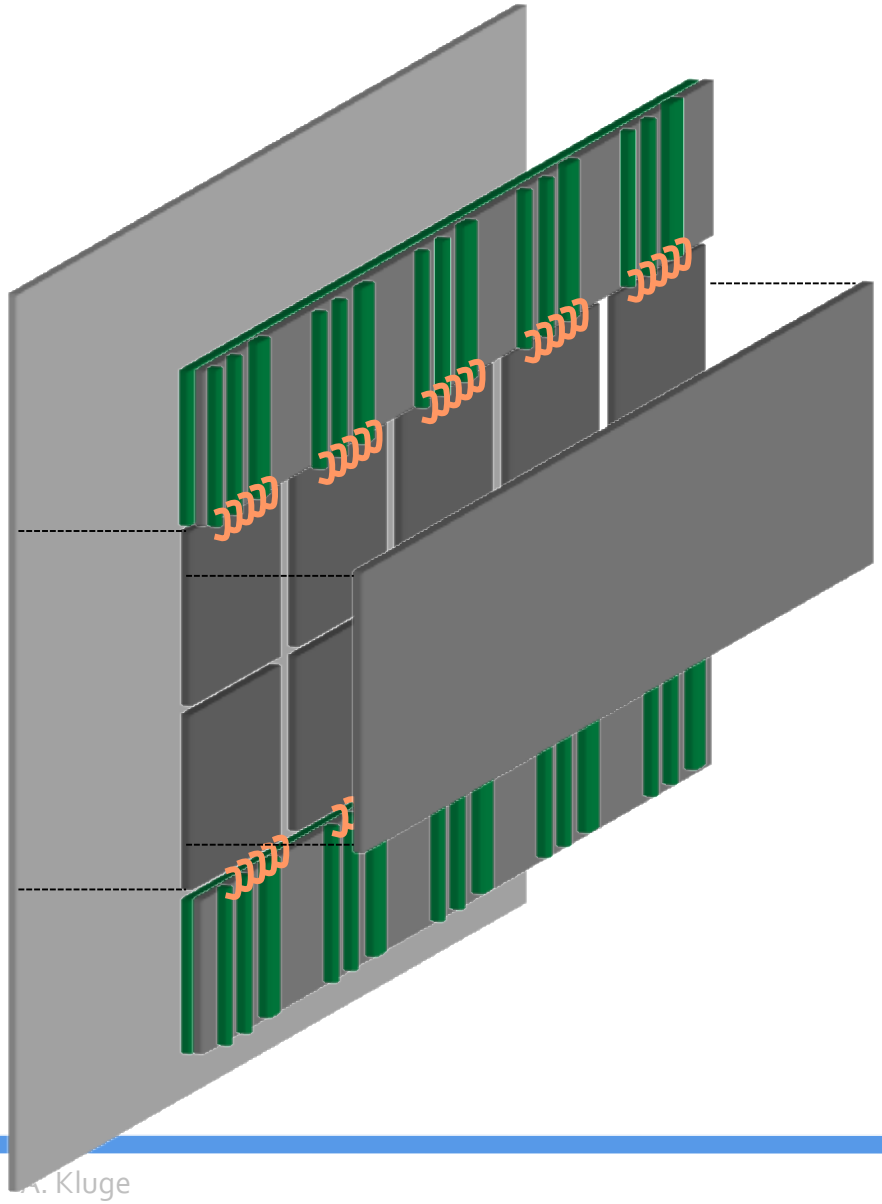


45 rows times 40 columns per chip = 1800 pixels per chip

Giga Tracker setup



Giga Tracker setup



- Sensor&bonds: 0.24% X_0
  200 µm Silicon
- RO chip: 0.11% X_0
  100 µm Silicon
- Structure: 0.12% X_0
  120 µm silicon
- Total: 0.47% X_0 uniform

The electronics specification

General: System Specifications

Number of pixels per chip	1800 = 45 x 40
Size of pixels	300 µm x 300 µm
Active area per chip	12 mm x 13.5 mm = 162 mm^2
Chip design TDC binning	100 ps
Thickness of sensor	200 µm
Type of sensor	p in n
Thickness of read-out chip	100 µm
Dynamic input range	5000 – 60000 electrons

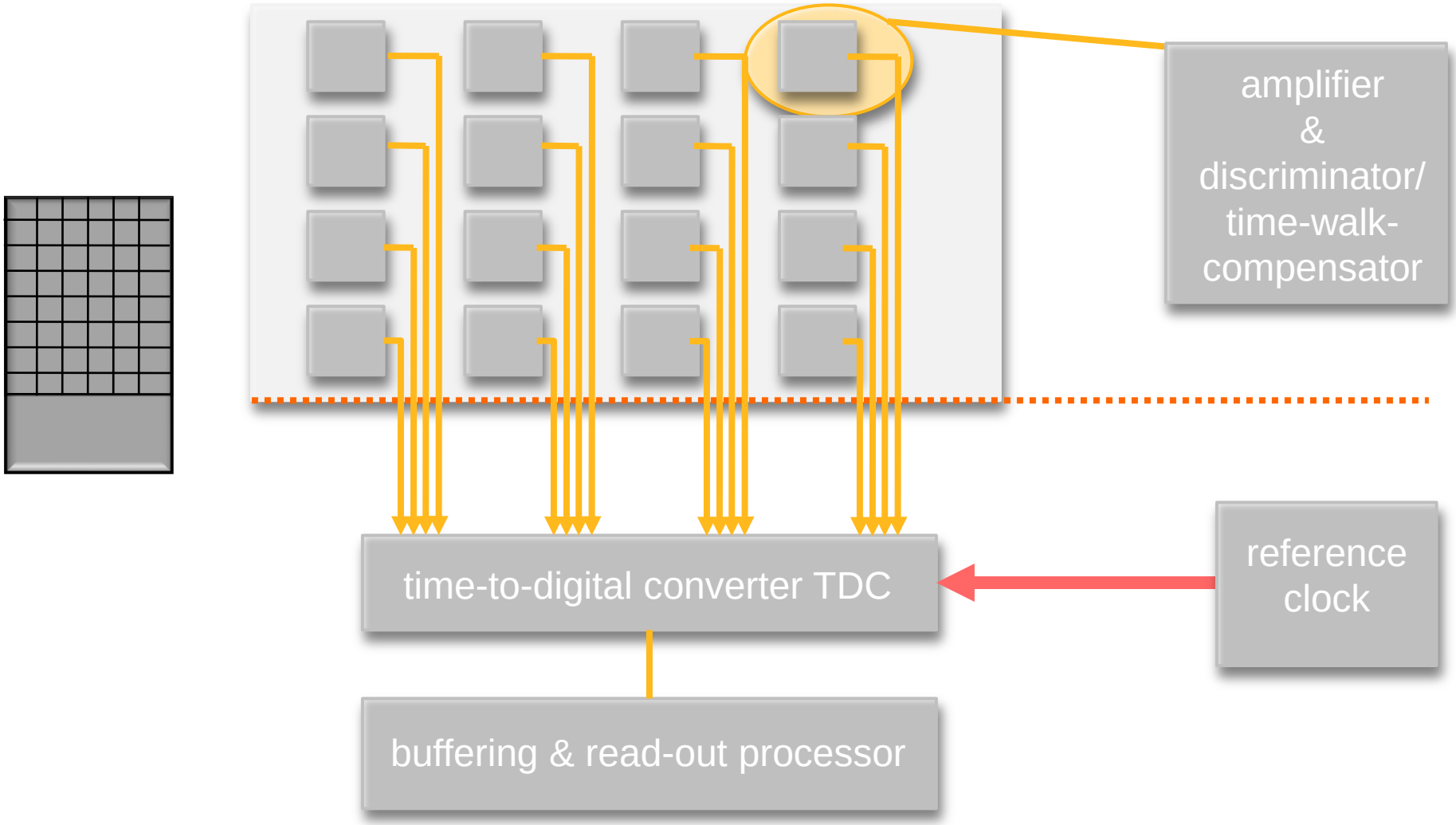
General: System Specifications

Design particle rate per chip	130 MHz nom. / 212 MHz max.
Rate of center pixel	140 kHz
Rate of center column	~ 3.3 MHz or 0.82 MHz/mm^2
Average rate per pixel	73 kHz
Maximum dead time	1 % (2 % in beam center)
Data transfer rate per chip	6 Gbit/s
Total dose in 1 year	~ 6 * 10^4 Gy
Neutron flux in 100 days	2 x 10^{14} 1 MeV neutron equivalent cm^{-2}
Material budget/thickness	0.5 % X_0 per station

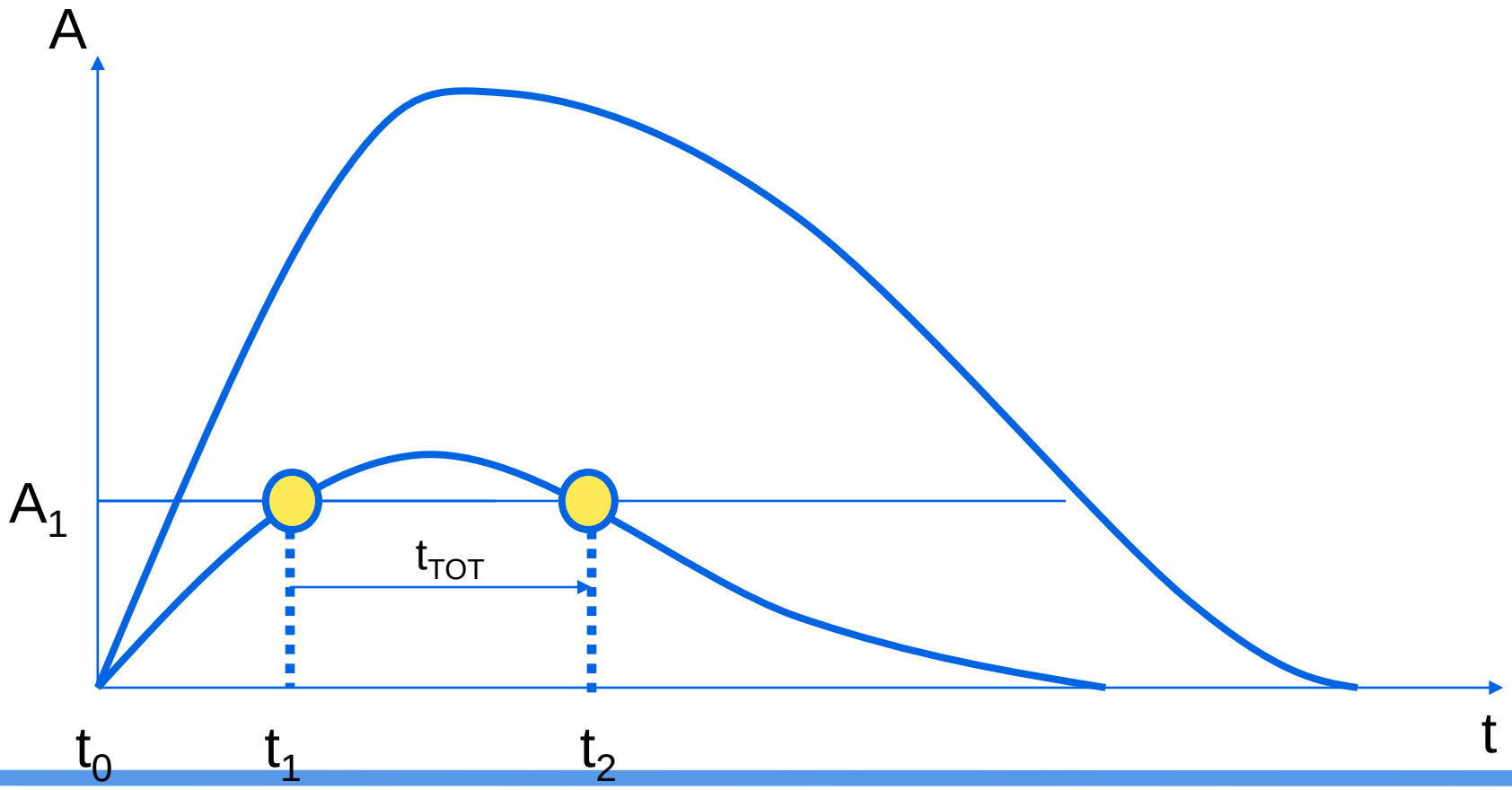
End-of-column architecture

EOC column principle

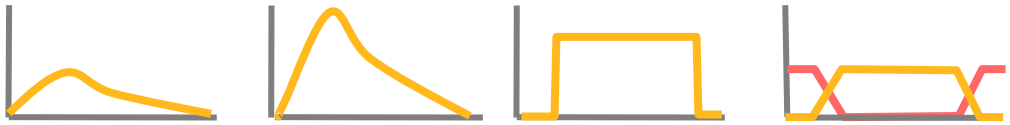
- No digital signals are distributed to pixel matrix during operation



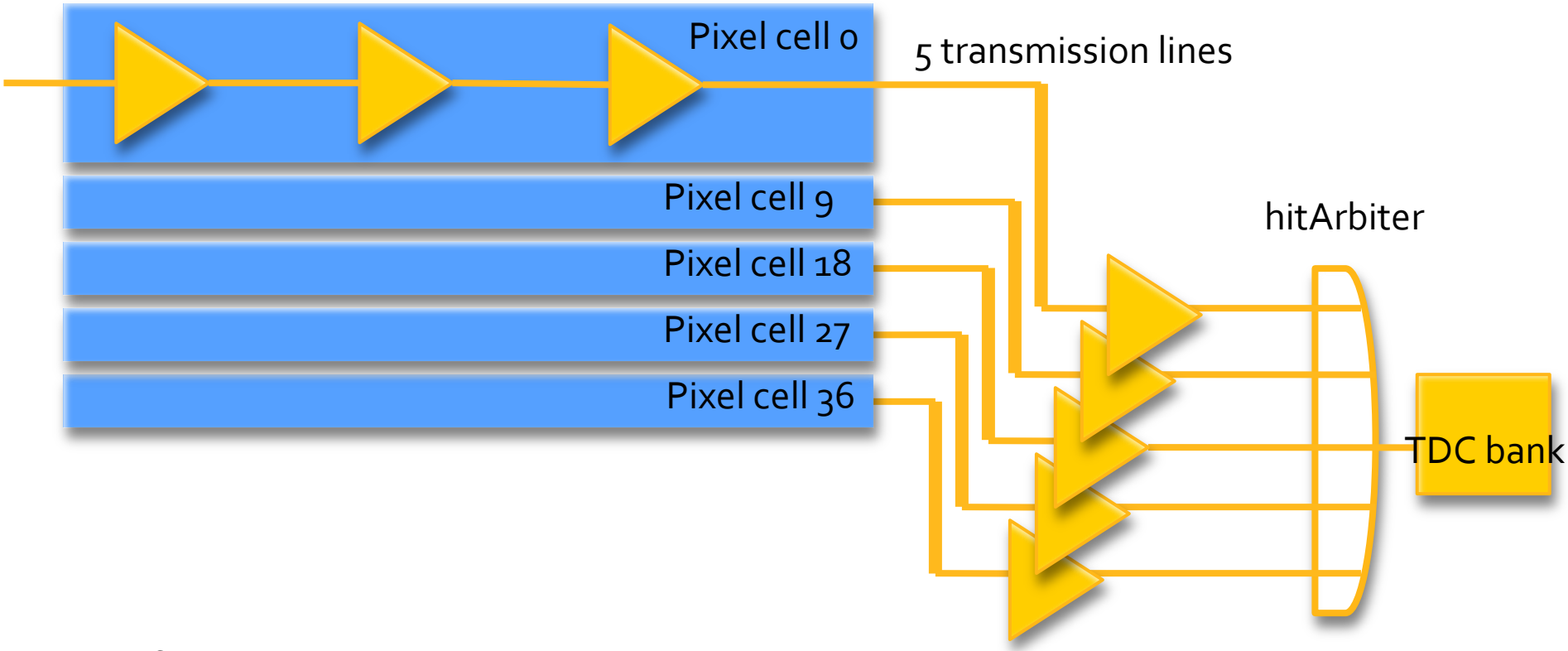
Time-over-threshold



front-end processing chain



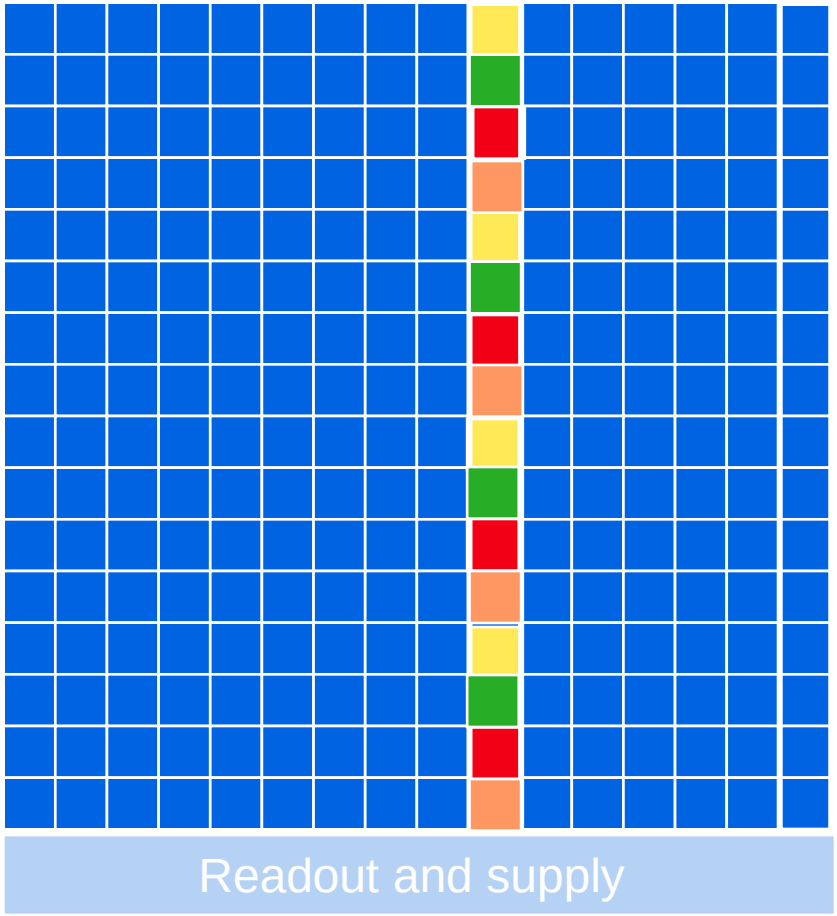
pre-amplifier TOT discriminator transmission line driver



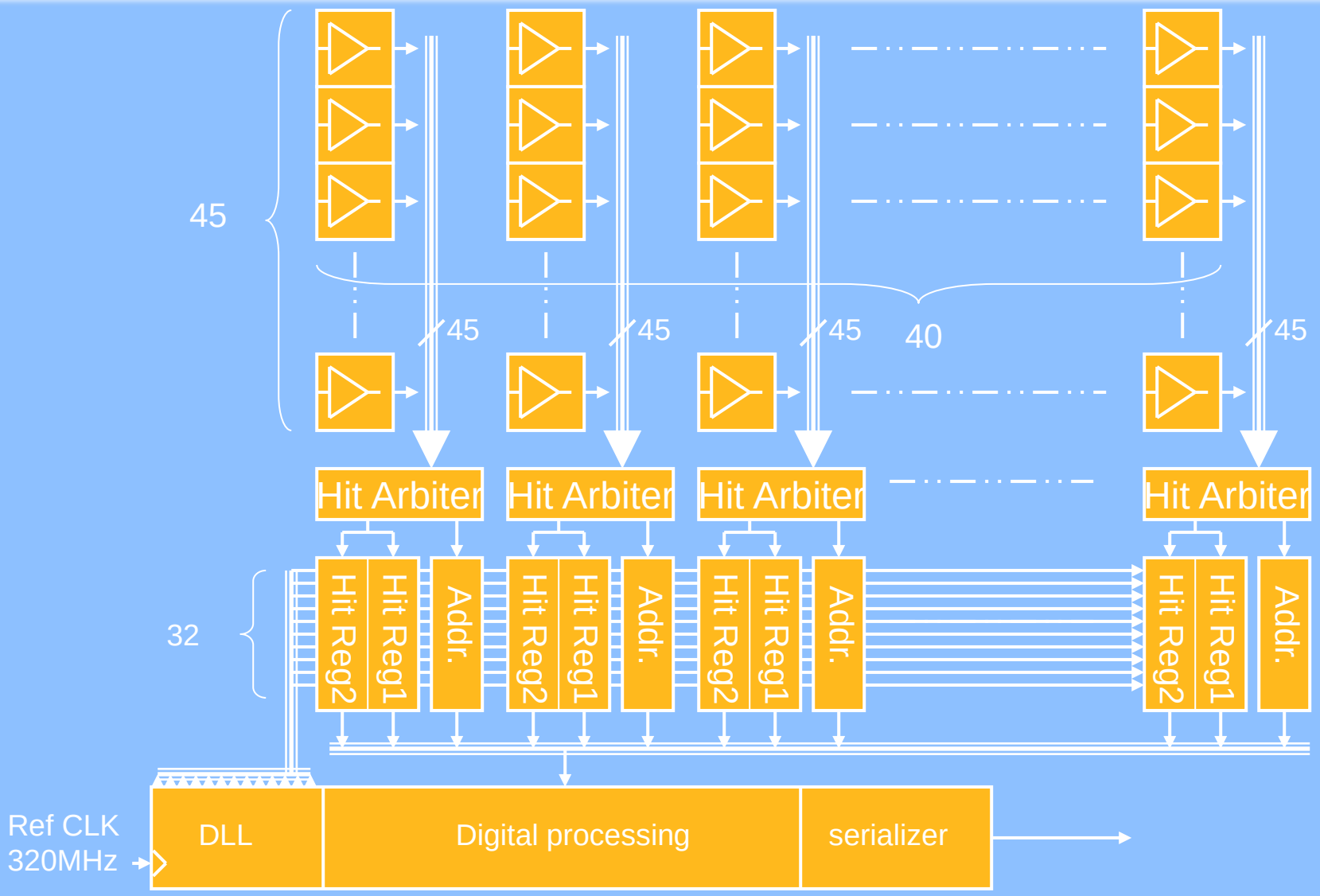
1 out of 9 pixel groups in a column

5 transmission line receivers

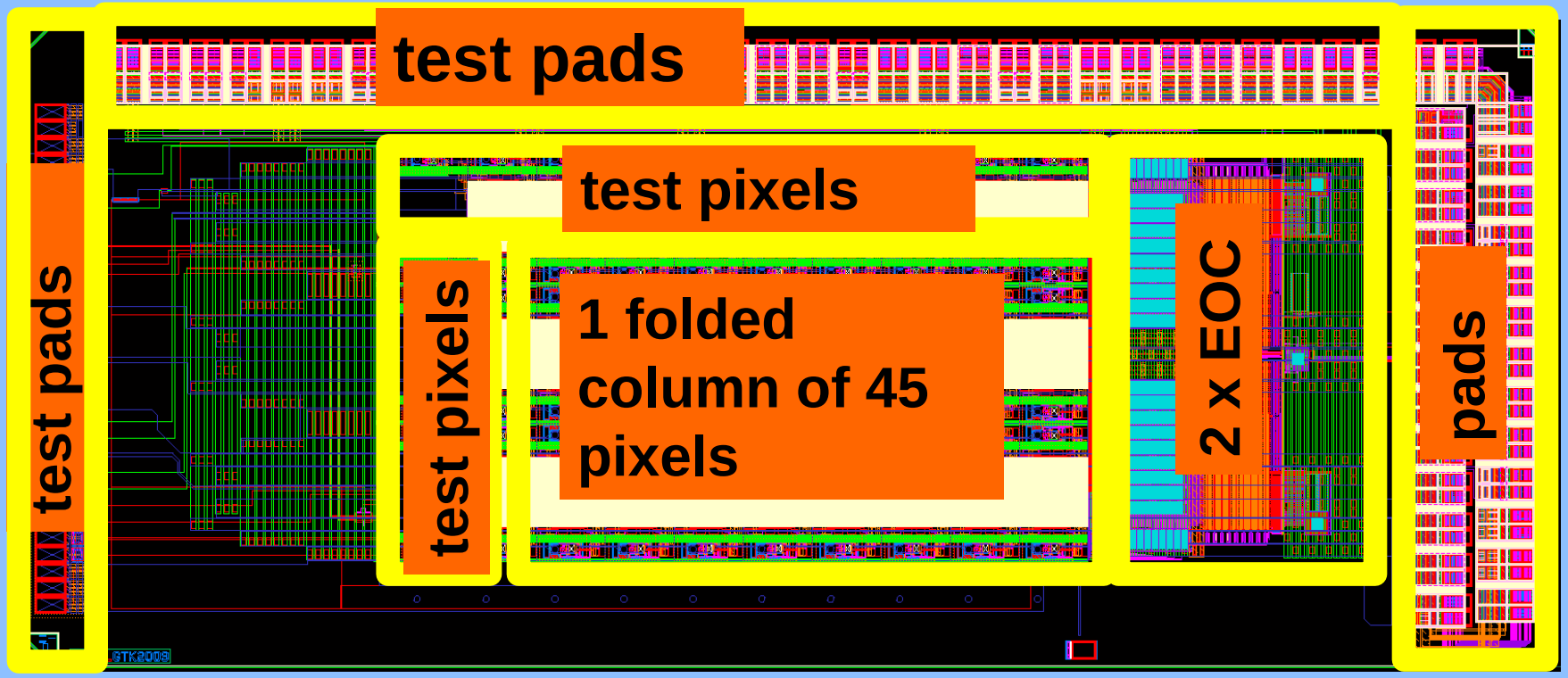
grouping of pixels



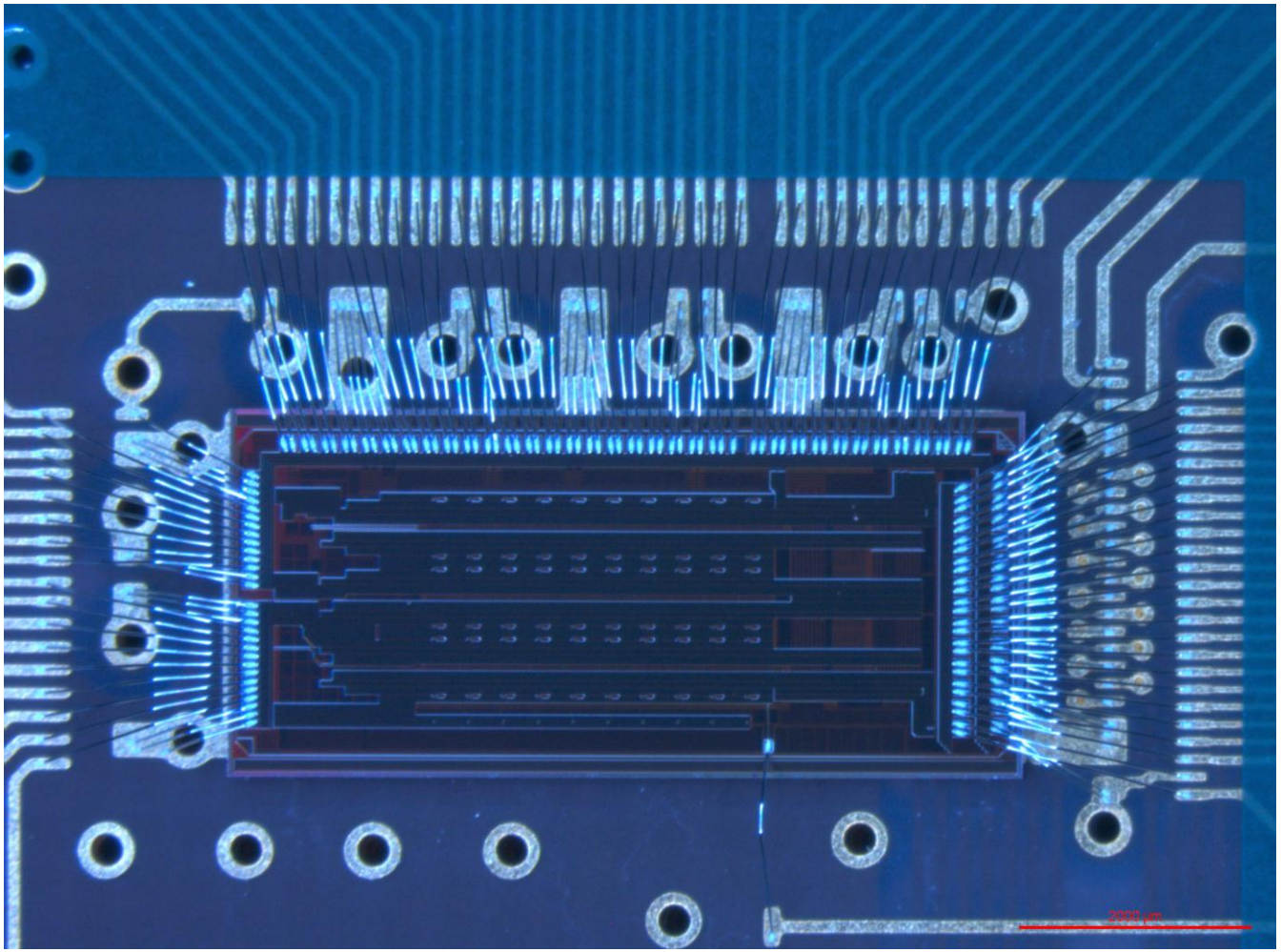
45 x 40 pixel TDCpix



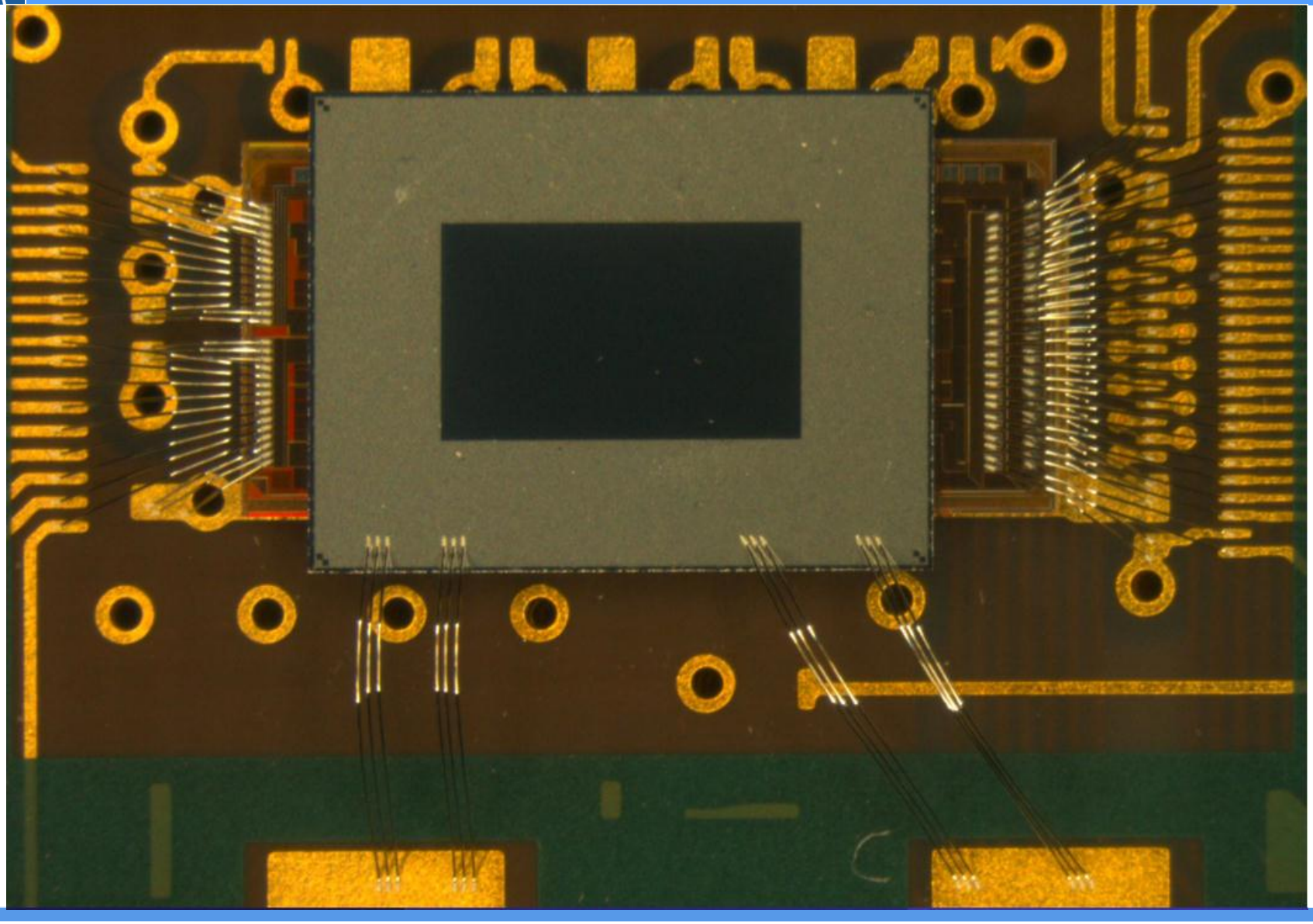
TDCpix demonstrator ASIC 130nm



TDCpix demonstrator ASIC

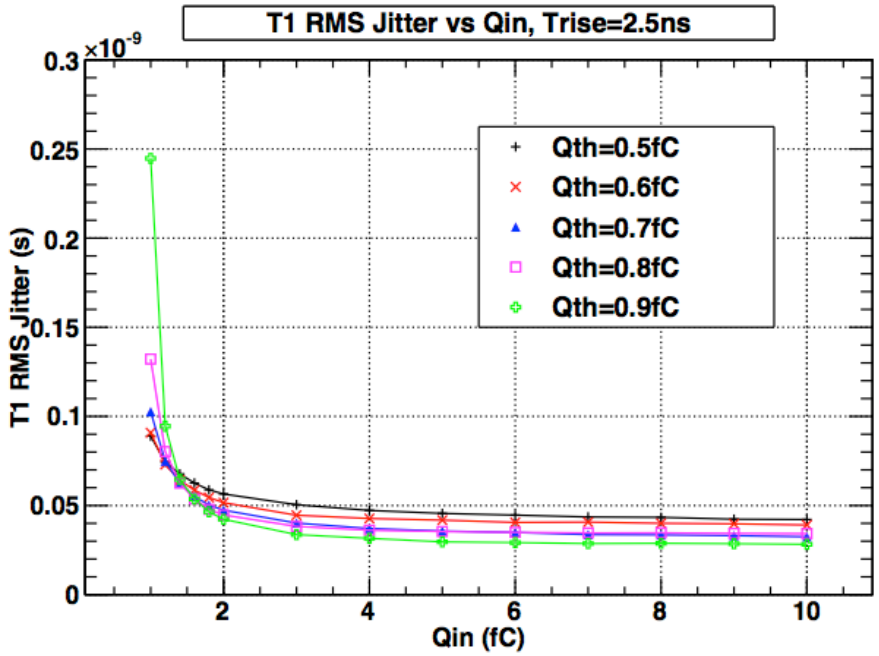


GTK demonstrator ASIC



TDCpix demonstrator: test pulse & laser test

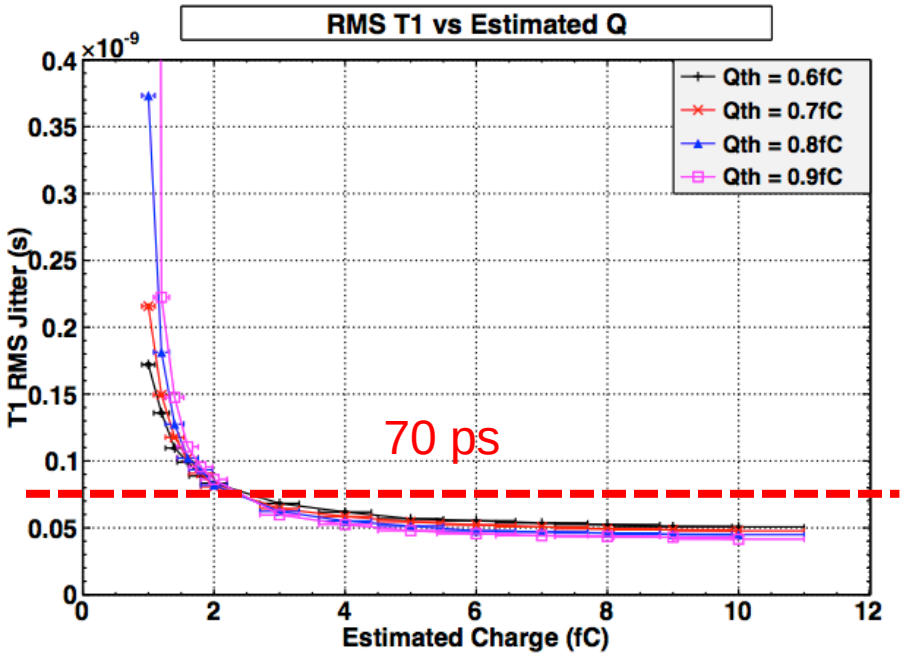
Electrical charge injection.
No detector.



$\sim 40\,ps$ RMS at $2.4\,fC$

130 e- noise @ no detector

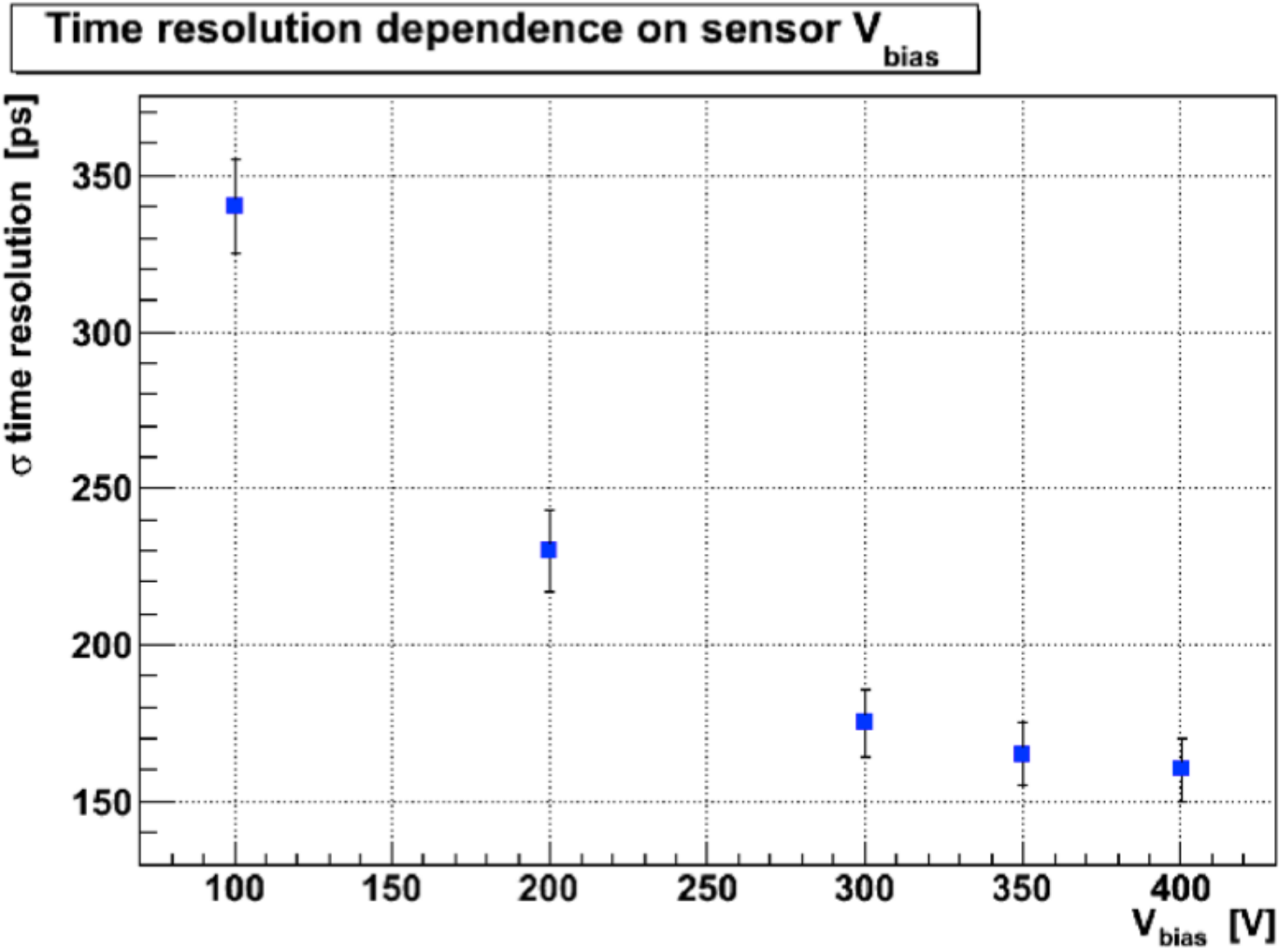
Laser Charge Injection.
Detector biased at 300V.



$\sim 70\,ps$ RMS at $2.4\,fC$

180 e- noise @ 250 pF detector

TDCpix demonstrator: beam test

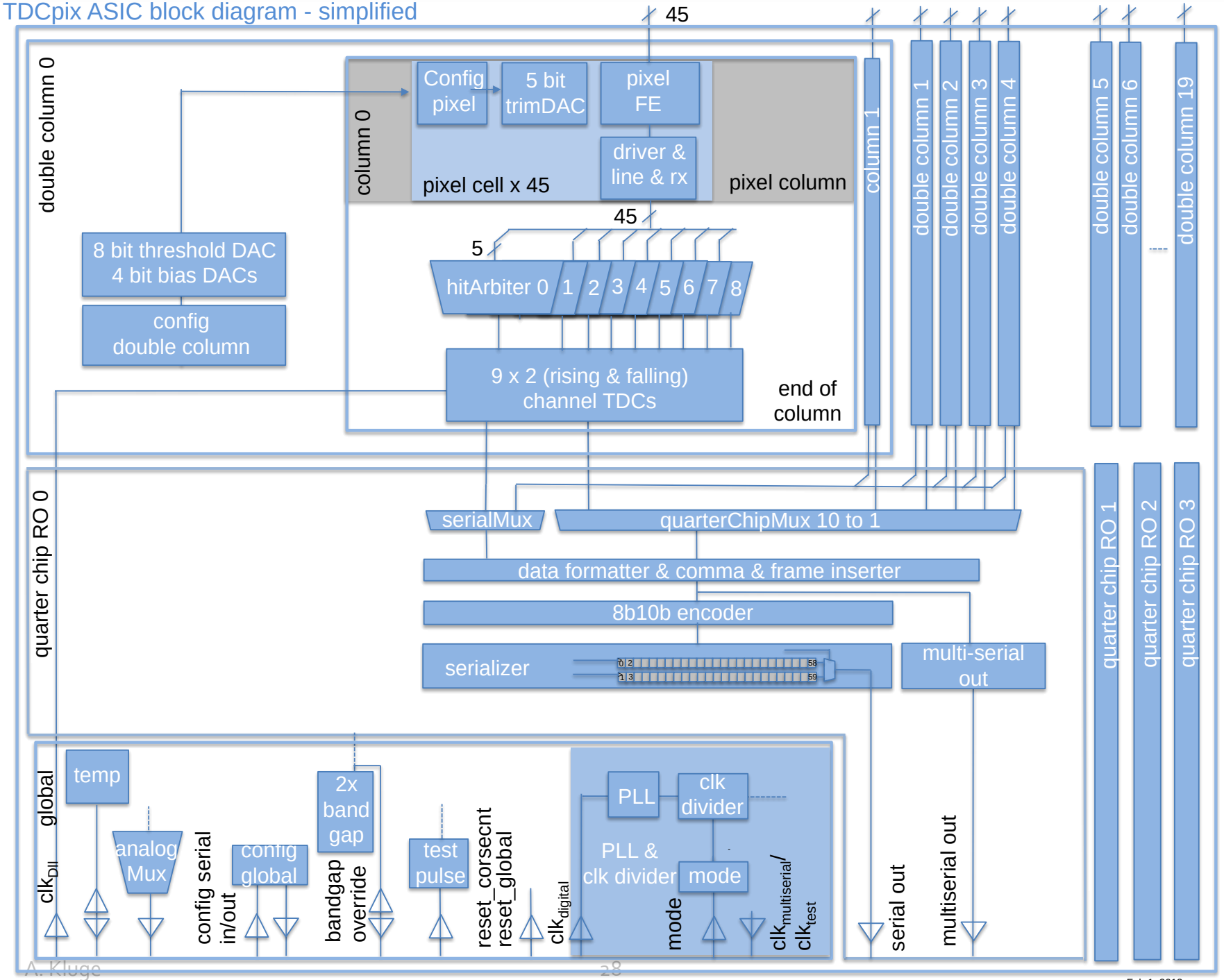


TDCpix

TDCpix at NA62 GTK

- Build a system with 54 000 pixels
  - divided into 30 ASICs = 1800 pixels
- to measure position
  300 um x 300 um pixel size
- and arrival time with 200 ps resolution

TDCpix ASIC block diagram - simplified

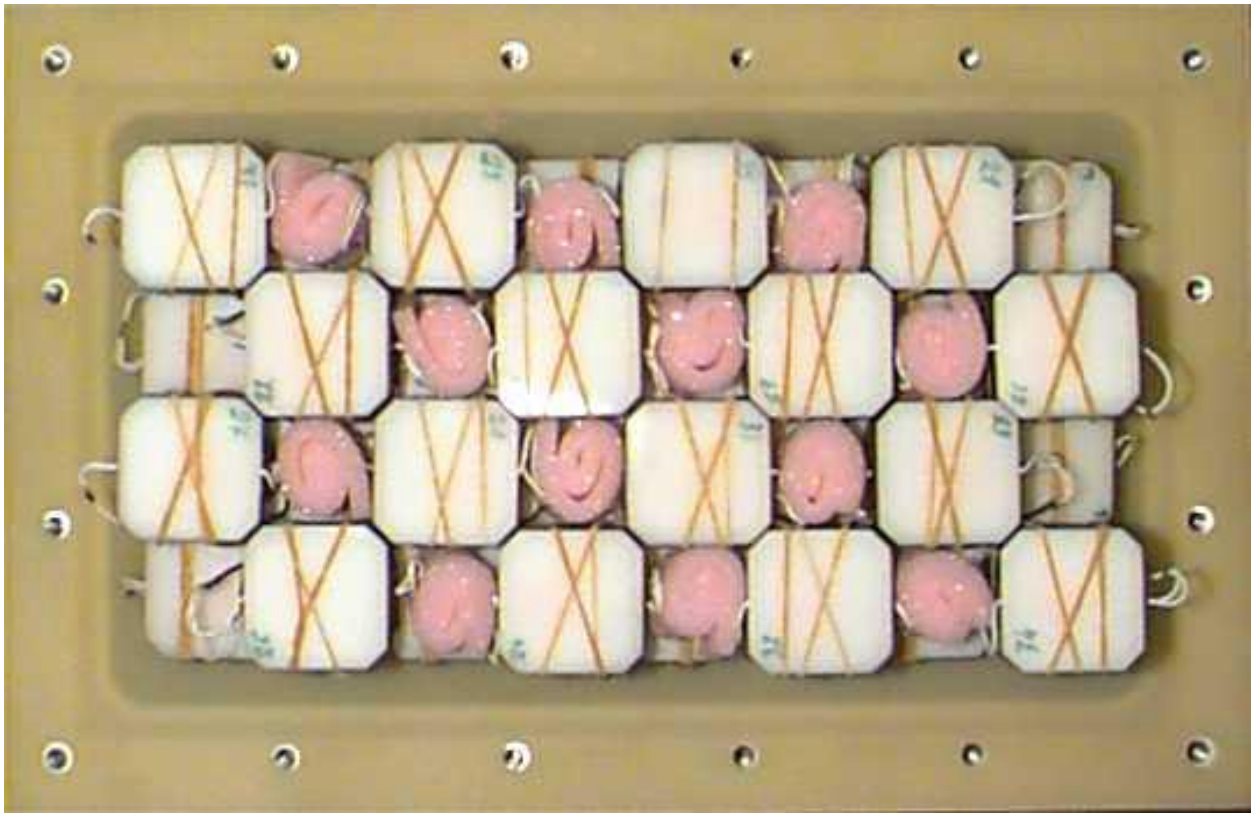


My Friends

- Why …
- Will …

Why is it so complicated?

TOF module 1998



12 cm

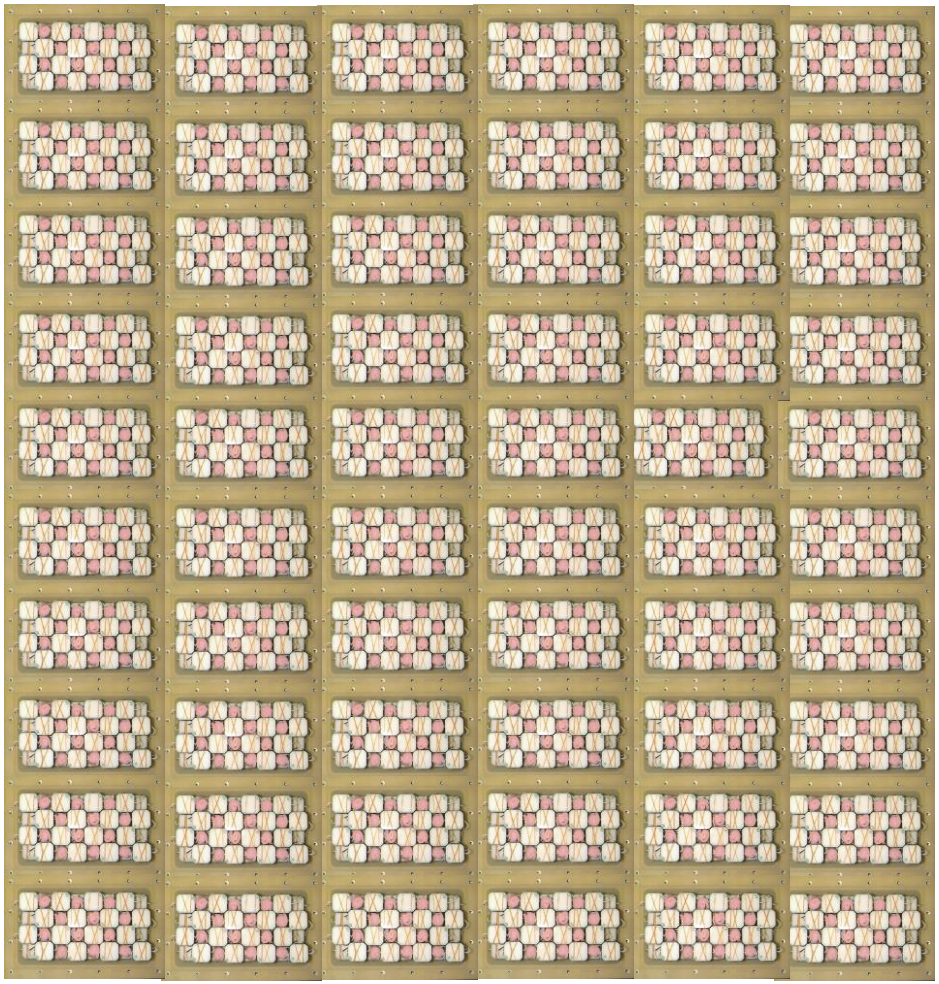
24 cm

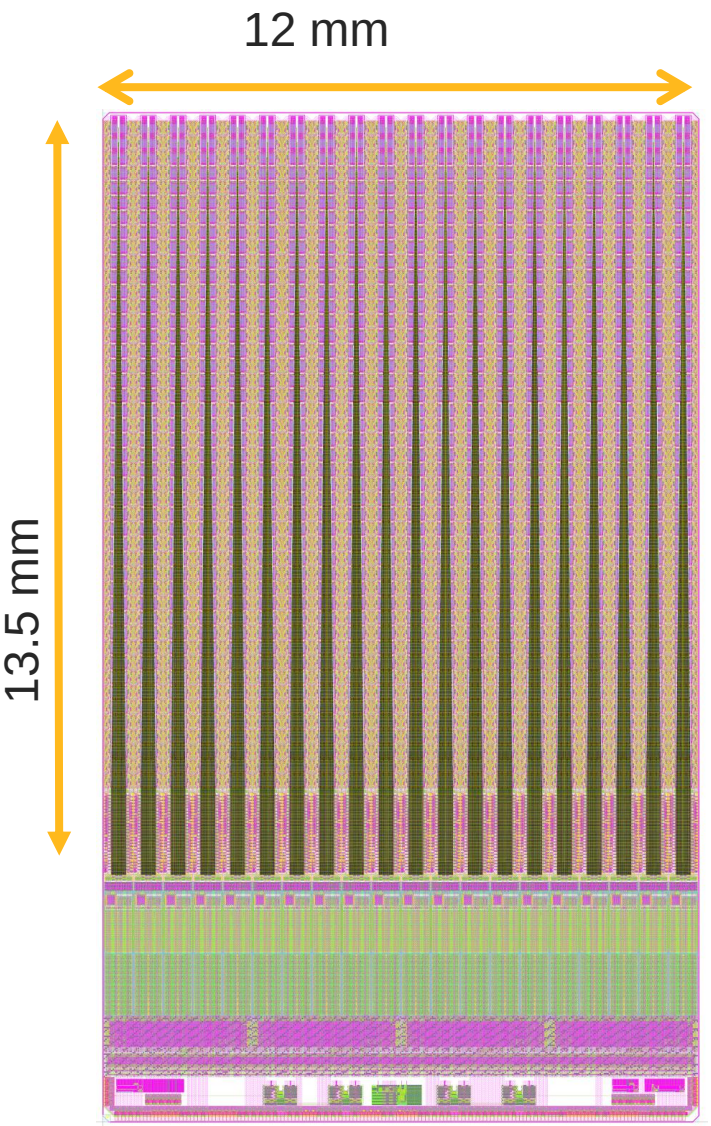
TOF module 1998
8 x 4 cells
90 ps resolution

3 cm x 3 cm “pixel”

- TDCpix
  - 40 columns x 45 rows
  - 300 um x 300 um
  - 200 ps resolution

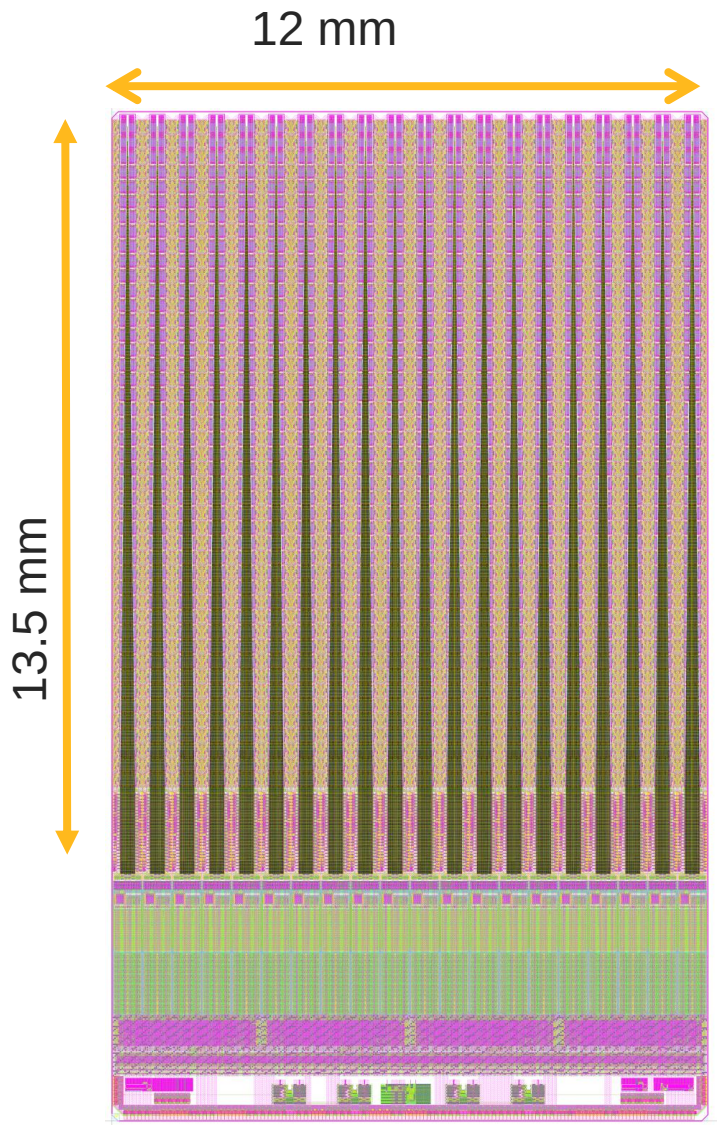
TOF array <-> TDCpix





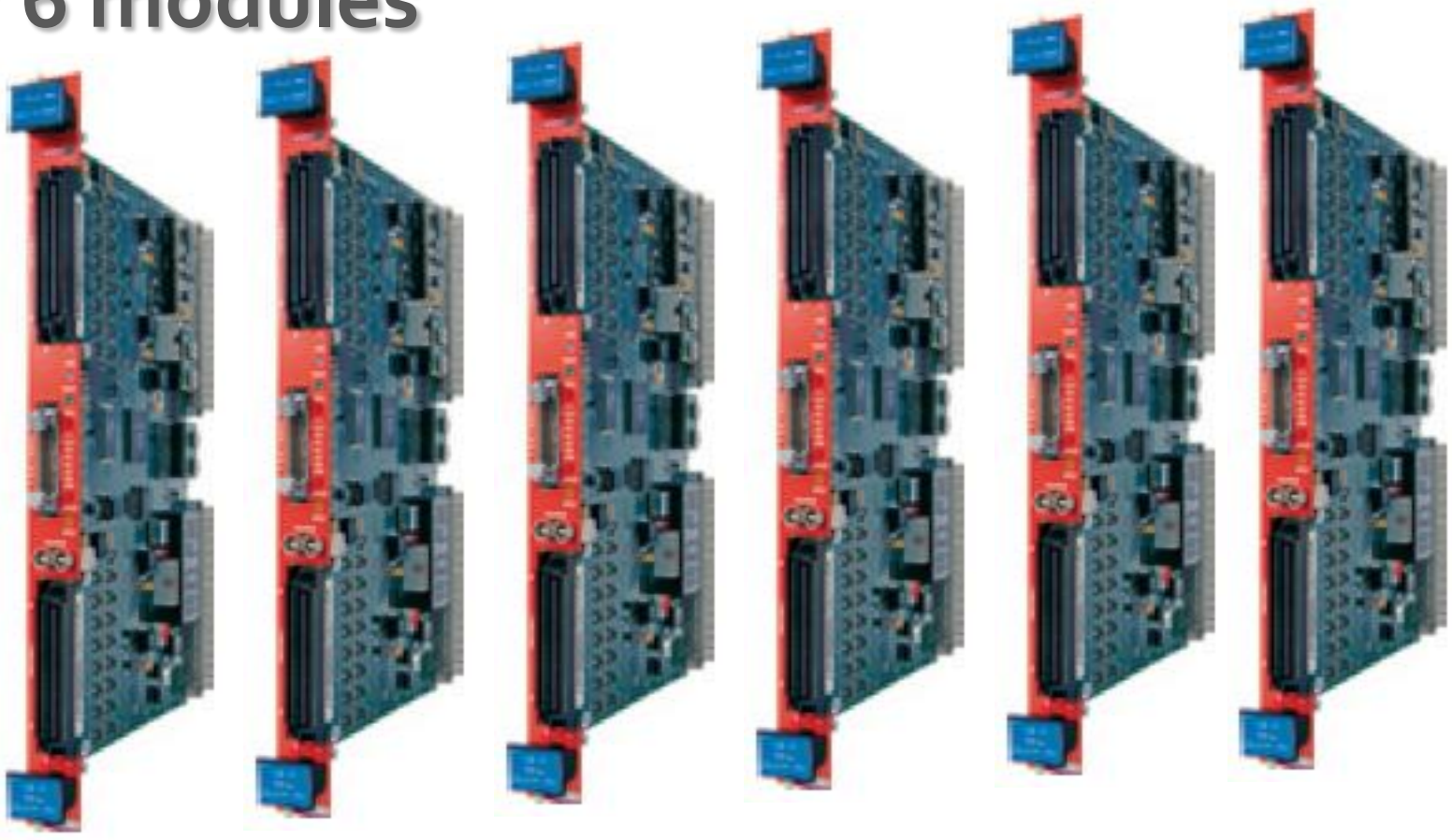
TDCpix

- 1800 front-end channels
- 360 x 2-channel TDCs (100 ps time bin)
- 4 x 3.2 Gbit/s serializers



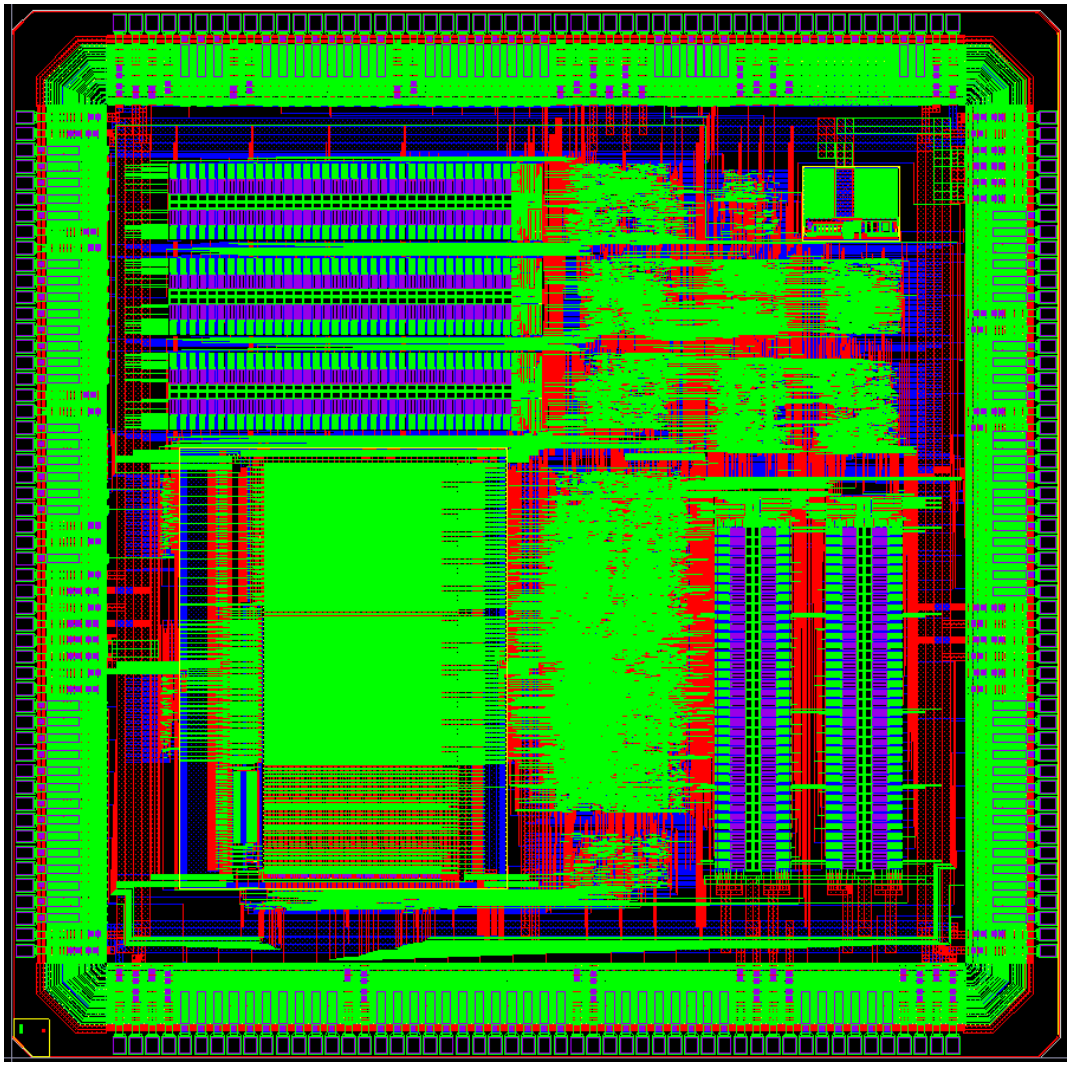
TDC in VME modules

- VME module 128 channels
- → 6 modules

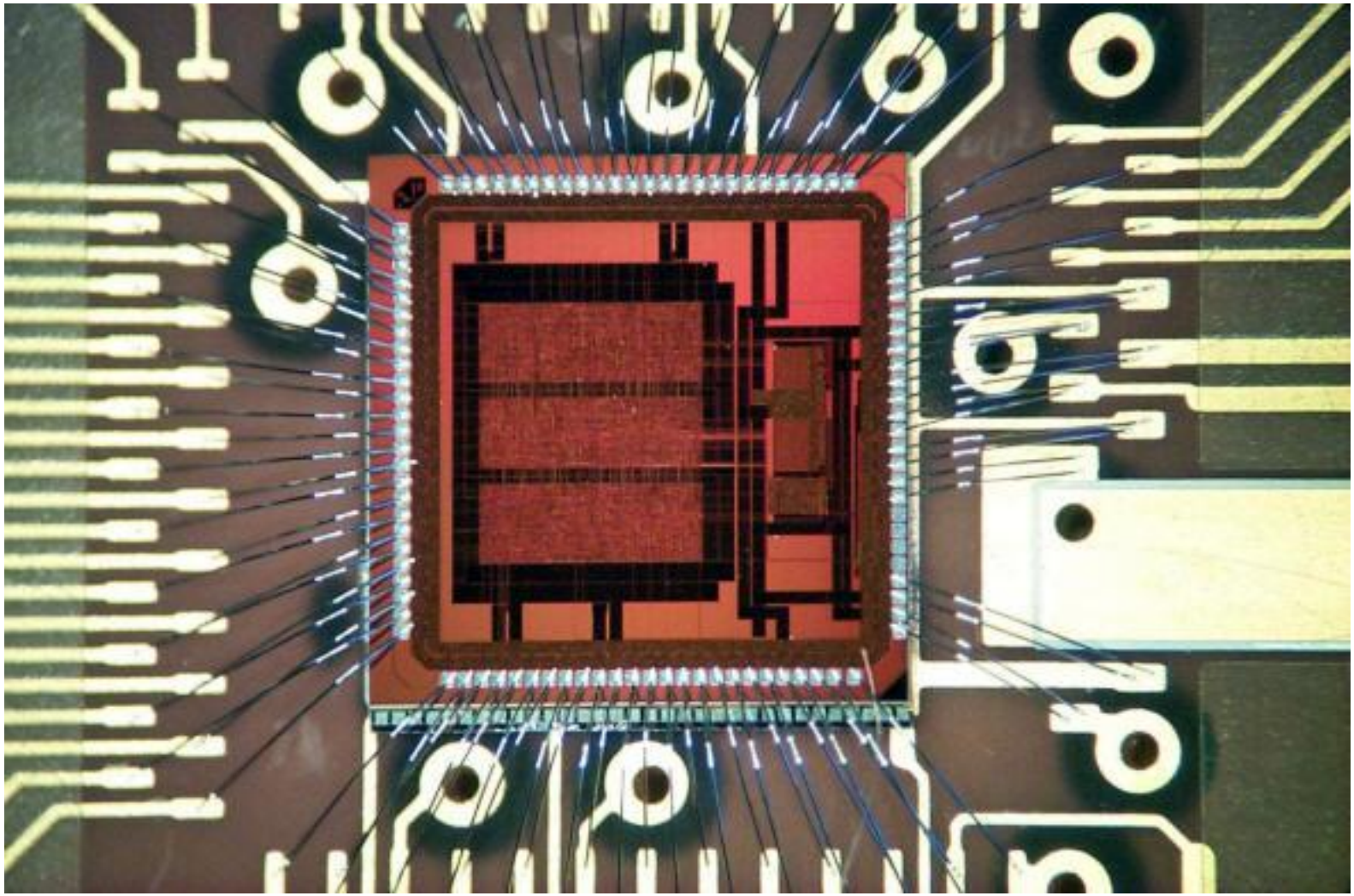


TDC in ASICs (HPTDC)

- 32 channels
- → 22 chips

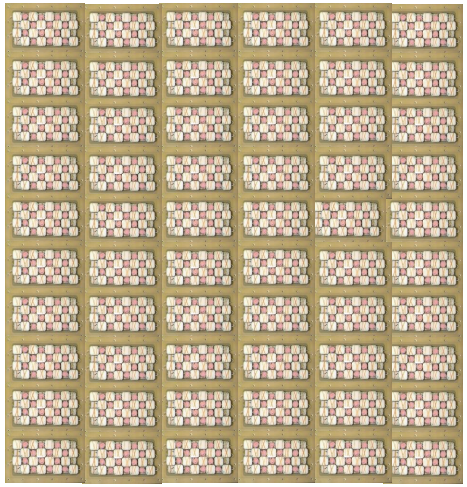


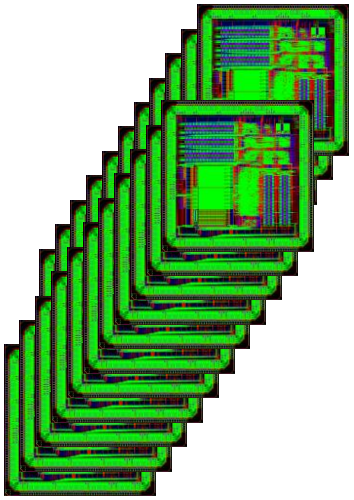
8 x GOL (1.6 Gbit/s serializer)

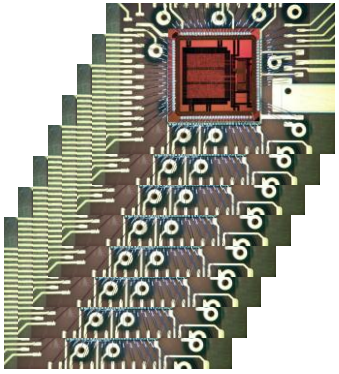


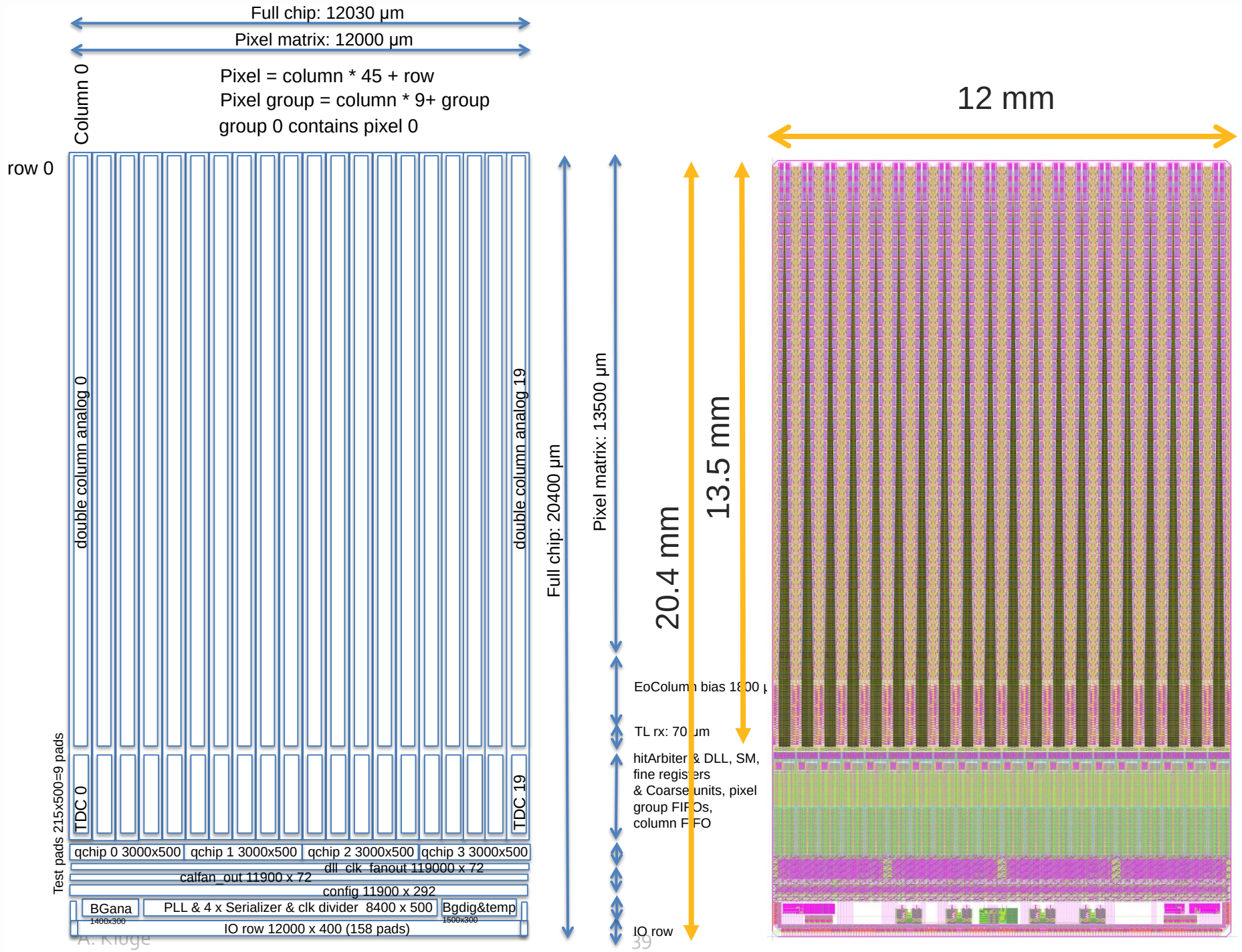
TDCpix

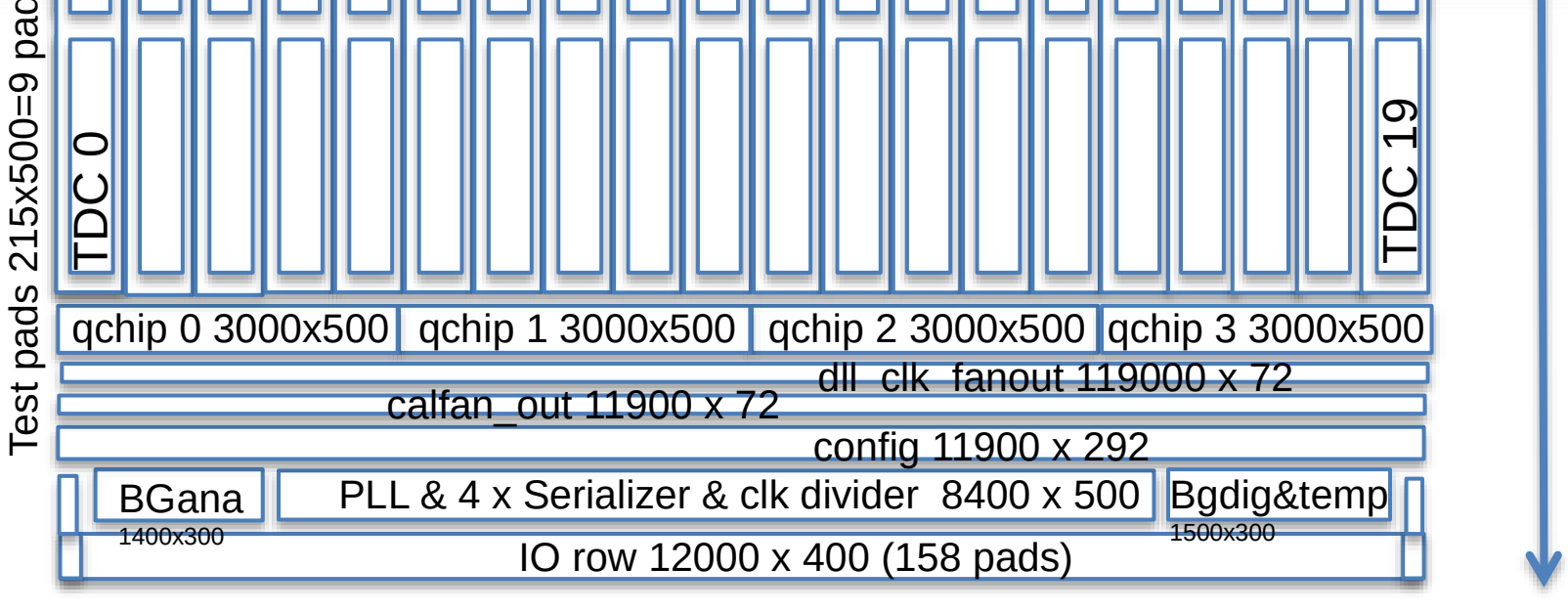
- Pixel chip with:
  - sub ns time resolution
  - triggerless architecture
  - 4 x 3.2 Gbit/s serializer








Full chip: 12030 µm
Pixel matrix: 12000 µm
Column 0
Pixel = column * 45 + row
Pixel group = column * 9+ group
group 0 contains pixel 0
row 0
12 mm
double column analog 0
double column analog 19
TDC 0
TDC 19
Full chip: 20400 µm
Pixel matrix: 13500 µm
20.4 mm
13.5 mm
EoColumn bias 1800 µ
TL rx: 70 µm
hitArbiter & DLL, SM,
fine registers
& Coarse units, pixel
group FIFOs,
column FIFO
IO row
Test pads 215x500=9 pads
qchip 0 3000x500
qchip 1 3000x500
qchip 2 3000x500
qchip 3 3000x500
dll_clk_fanout 119000 x 72
calfan_out 11900 x 72
config 11900 x 292
BGana
1400x300
PLL & 4 x Serializer & clk divider 8400 x 500
Bgdig&temp
1500x300
IO row 12000 x 400 (158 pads)


Test pads 215x500=9 pad
TDC 0
TDC 19
qchip 0 3000x500
qchip 1 3000x500
qchip 2 3000x500
qchip 3 3000x500
dll_clk_fanout 119000 x 72
calfan_out 11900 x 72
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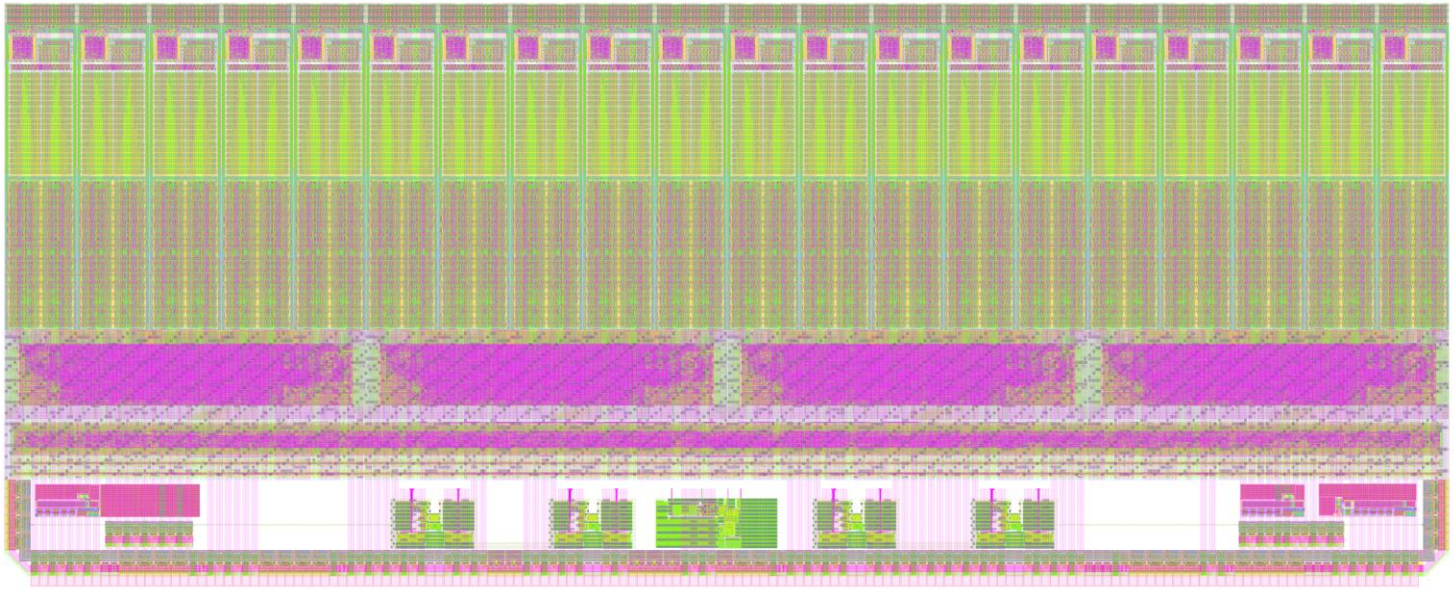
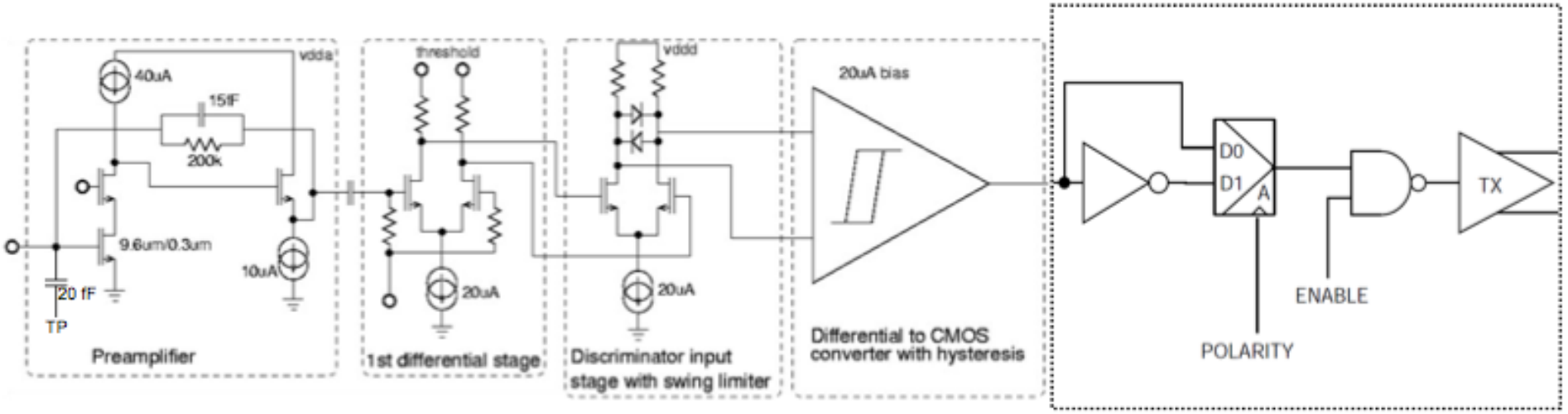


Building blocks

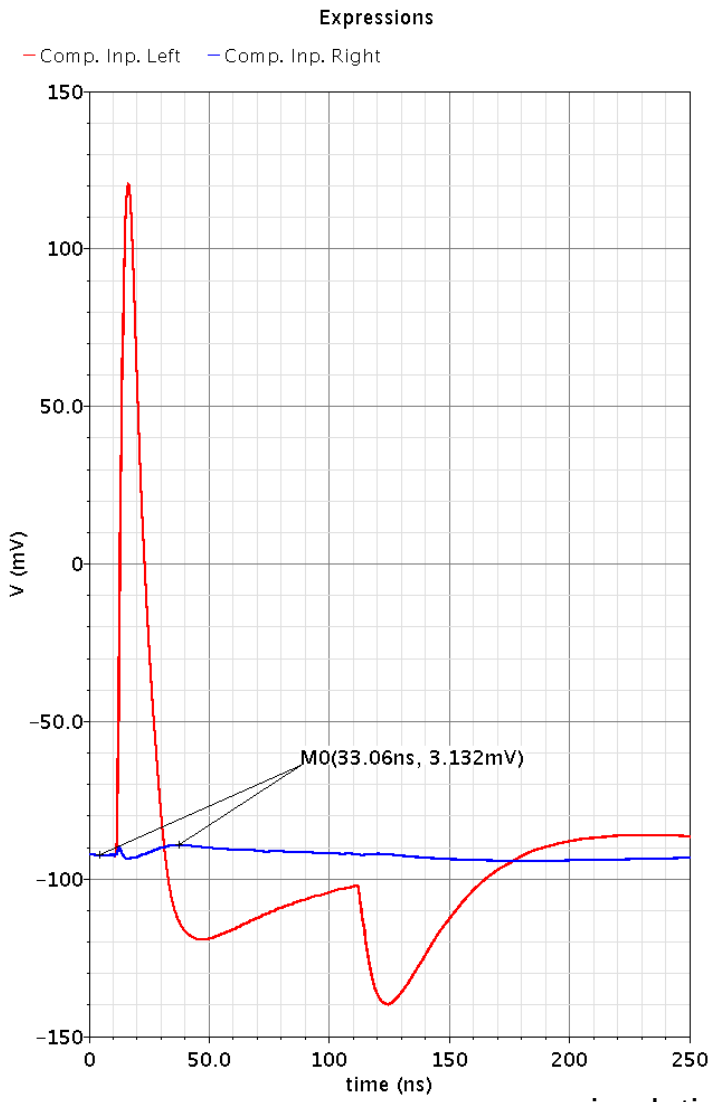
Front-end chain

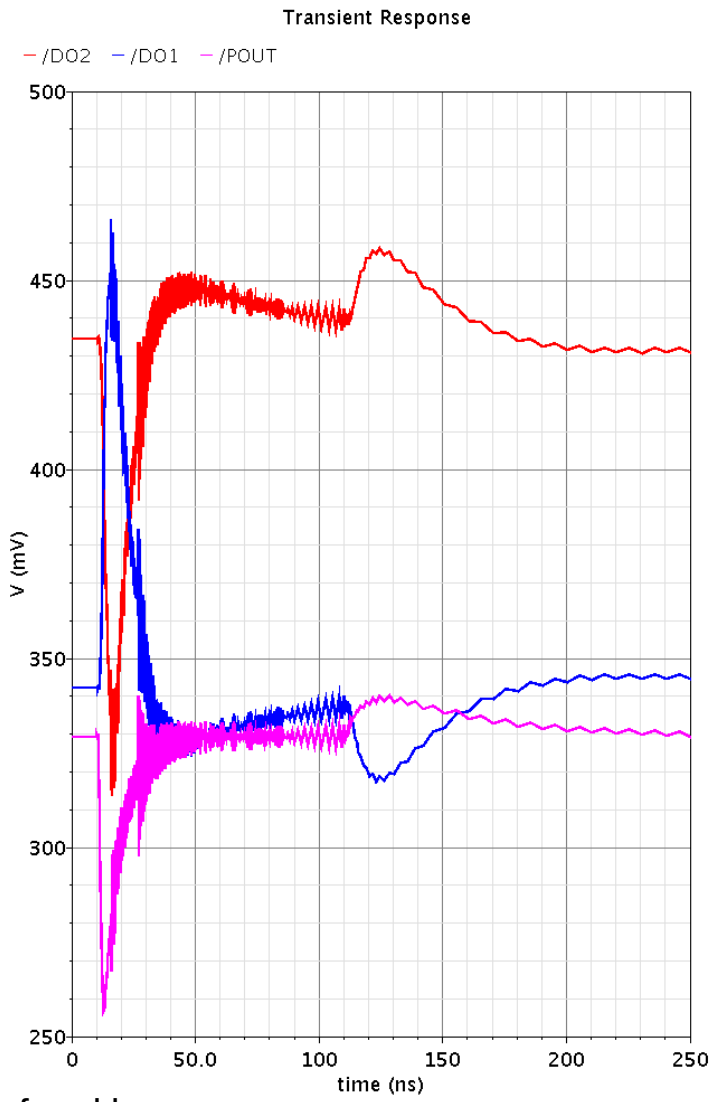


Dynamic Range	0.6-10 fC / 3600-60000 e-
Gain	75 mV/fC
Peaking time	5 ns
ENC (no sensor)	130 e-
FE power	130 µA (56%)
TX line driver	100 µA (44%)
Full matrix power	500 mW

Substrate separation in front-end

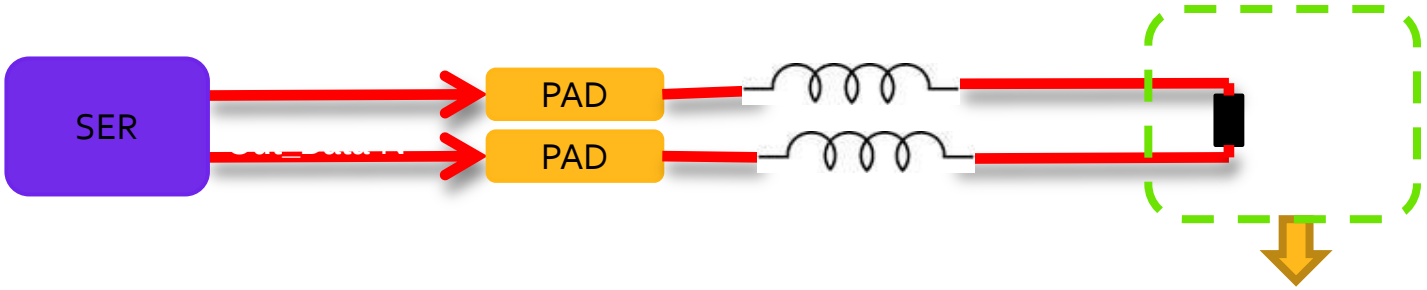
45 out of 90 pixels pulsed
12 power pair connections

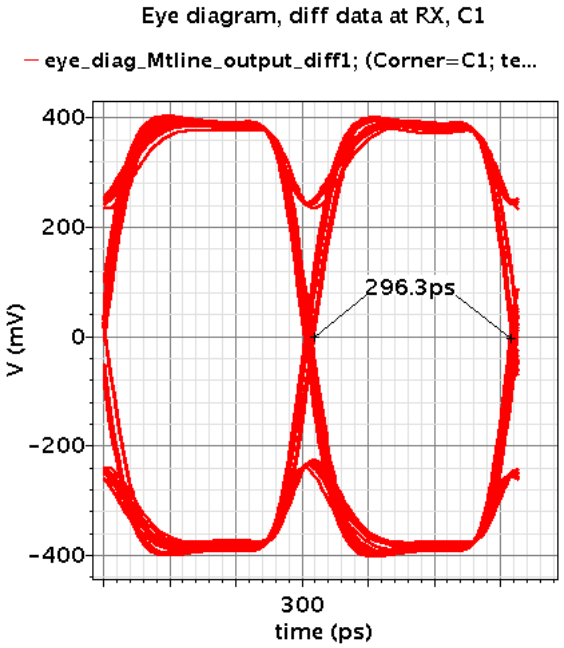


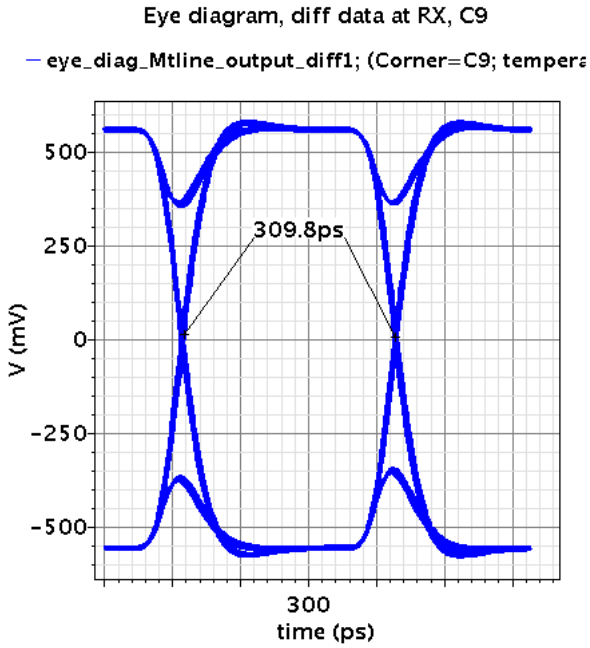


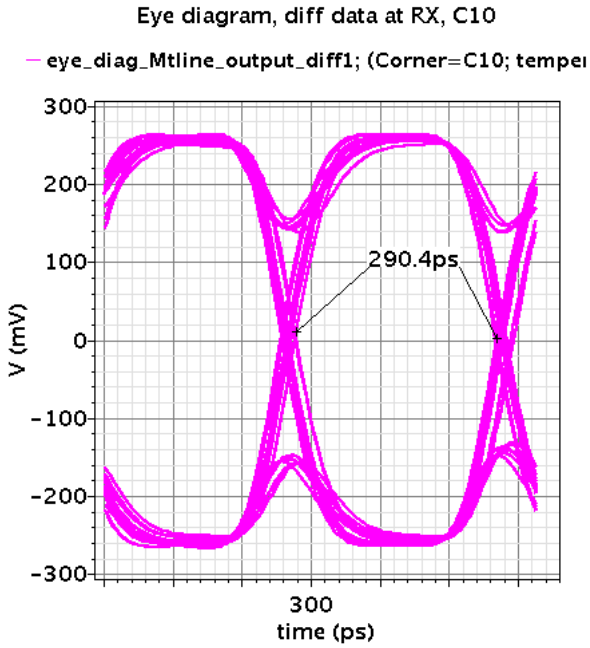
simulation of gnd loop

Serializer Cell– 3.2Gb/s









TDC

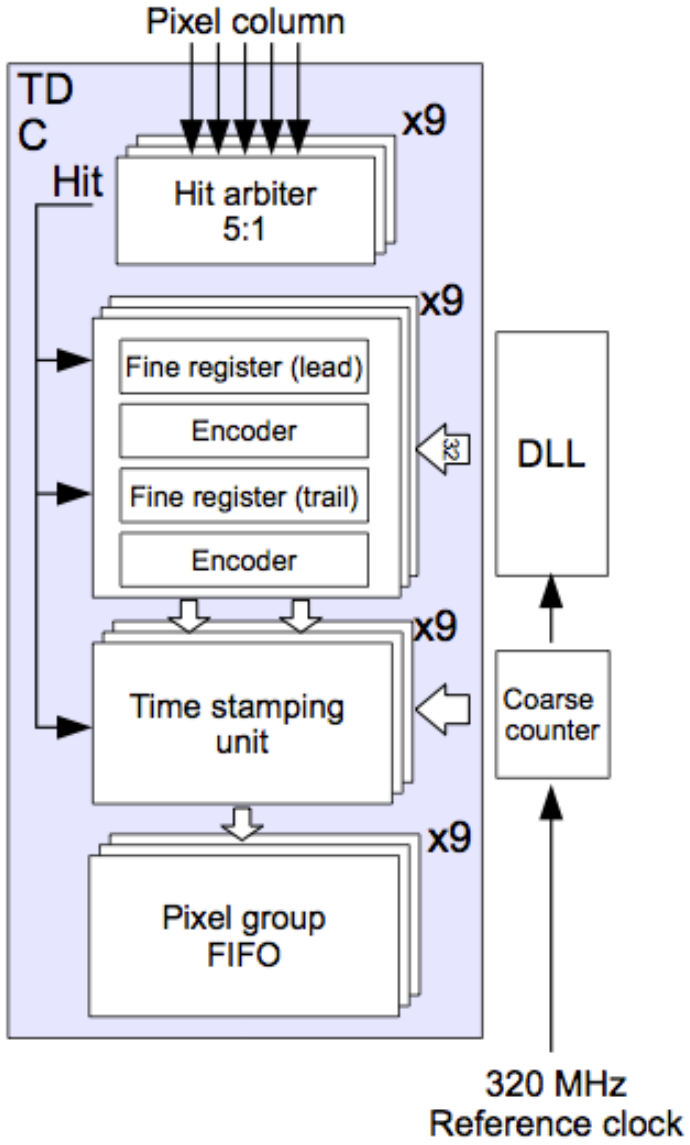
Delay Locked Loop based TDC

- 32 bins, 97 ps width

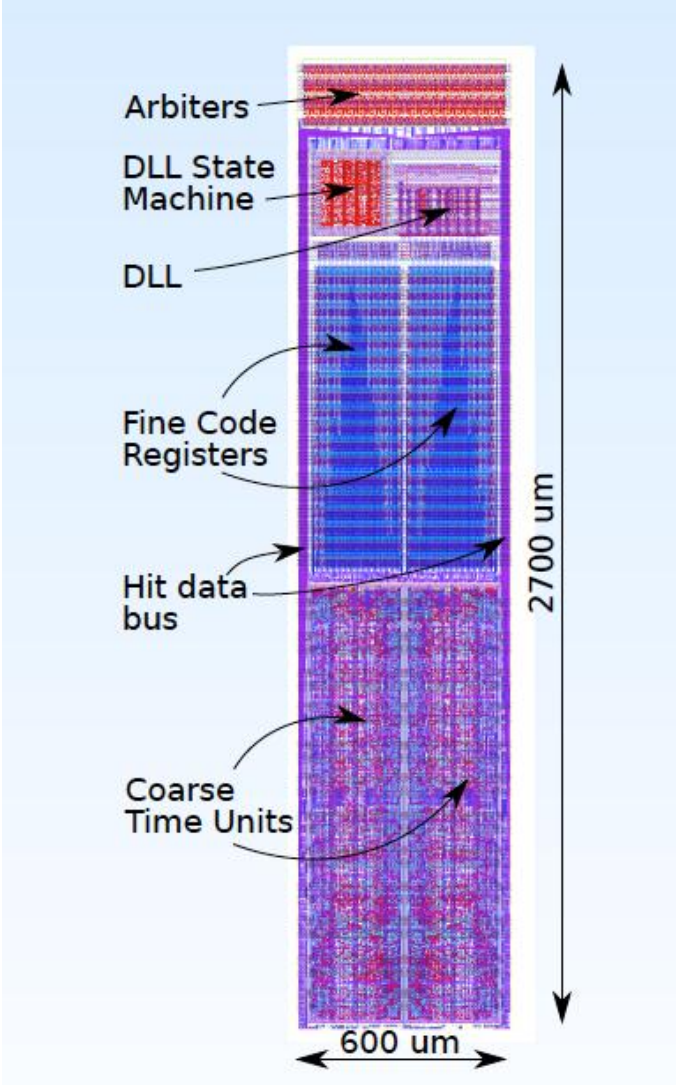
Hit multiplexing

- Extensive simulation with realistic stimulus
  - 99.4% hits recorded, 0.6% hits collide, pile-up recorded

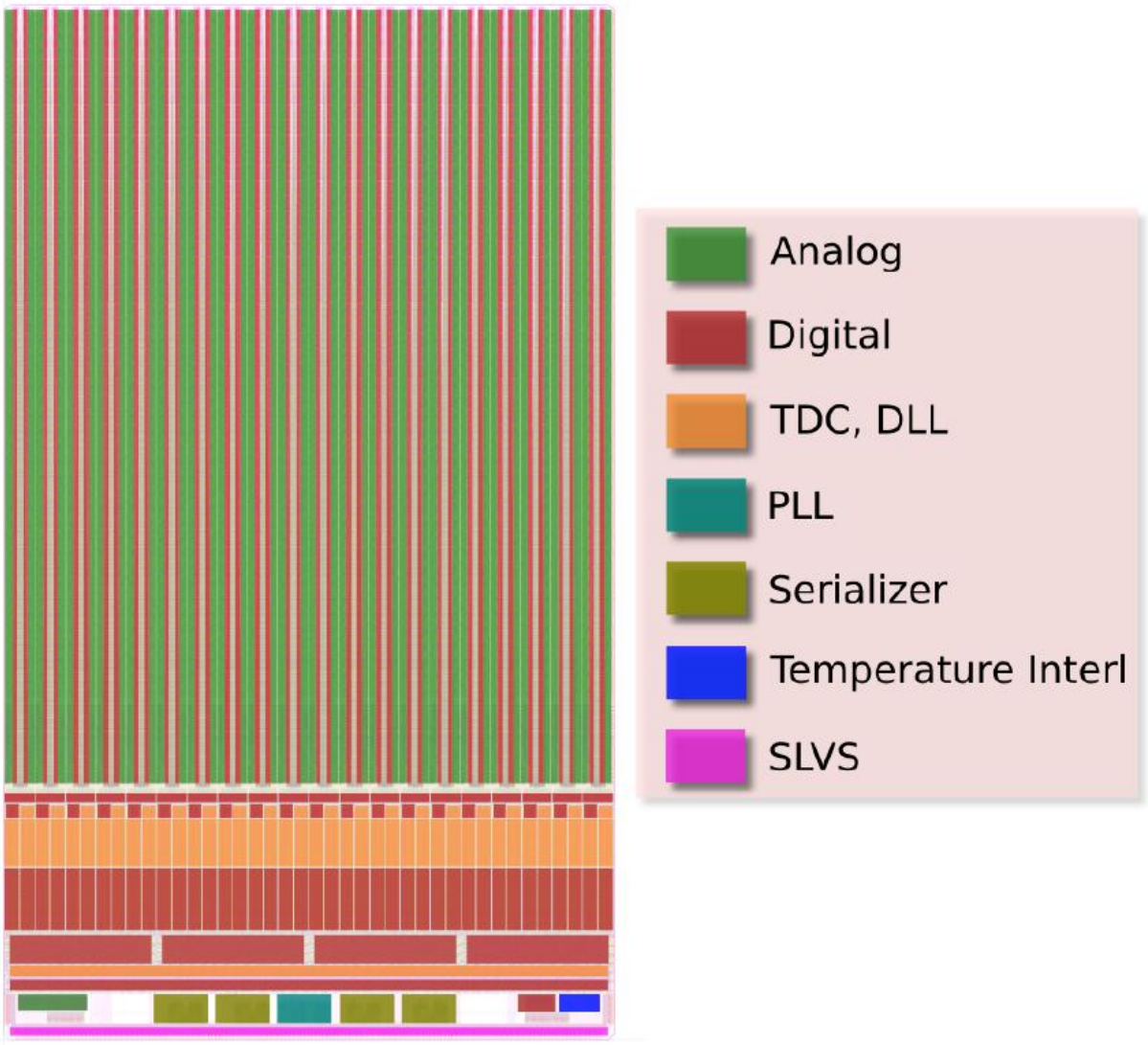
	Power [mW]
DLL	20
Register bank	5
20x DLL + 40x banks	600 (14% of chip budget)



18 x 2 channel TDC layout



Power domains – now system on Chip



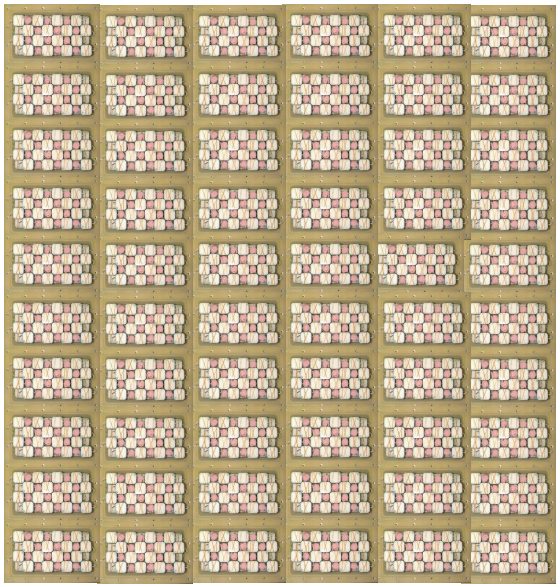
Power domains

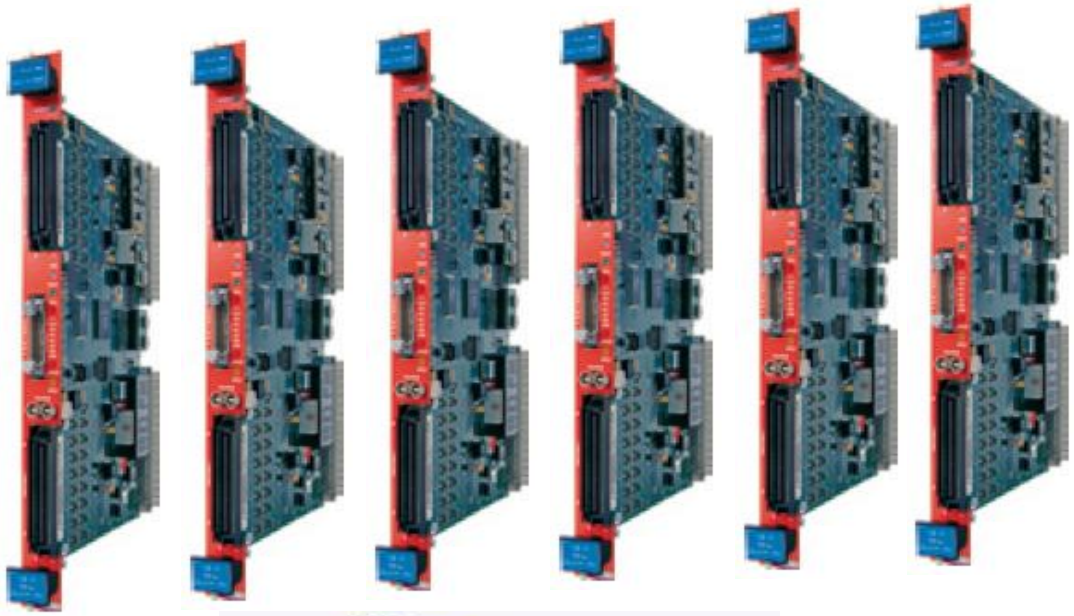
VDD/GND domain	Nom. Current [mA]	%		Power pad *pairs*			
				Main row		Staggered	Total
Analog	272	12.6%		12	+	4	16
Digital	940	43.5%		8	+	5	13
TDC	568	26.2%		7	+	2	9
PLL	92	4.3%		2	+	0	2
Serializer	292	13.5%		12	+	0	12
Temp. Interlock				1	+	0	1
SLVS				5	+	0	5
	2164						**58**

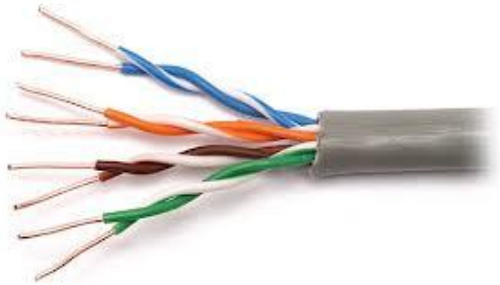
Will

Will it work?

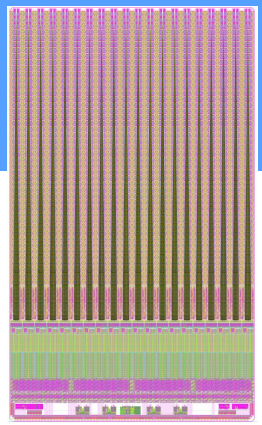
Will it …?

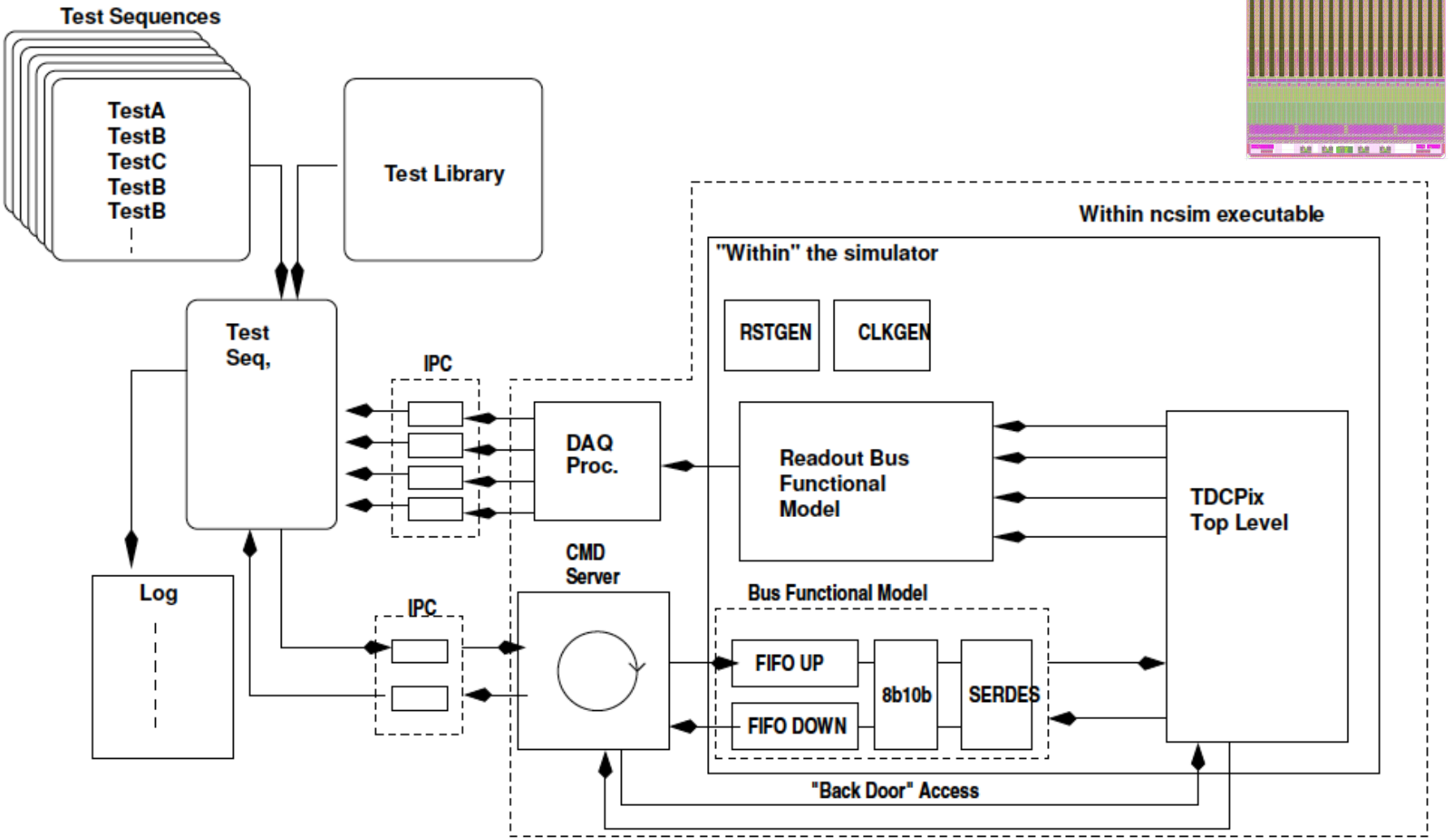






Top level test bench

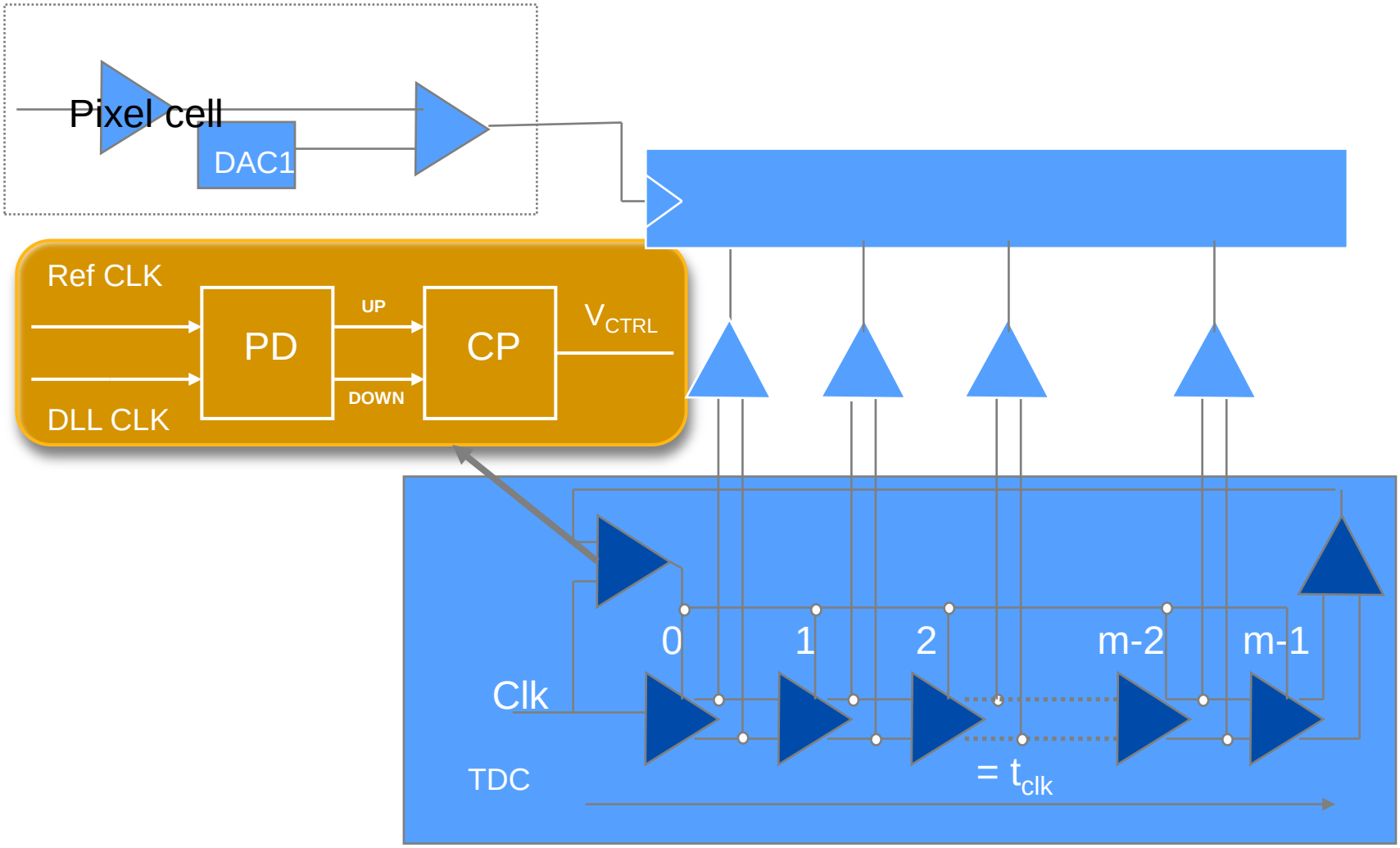




Summary

- Demonstrator with 170 ps @ beam
- TDCpix – pixel chip arrival time tagging
  - 1800 pixels
  - 300 µm x 300 µm
  - triggerless read-out
  - 4 x 3.2 Gbit/s
  - 100 ps TDC time binning
  - with 200 µm thick silicon sensor
  - resolution target: 200 ps

DLL based TDC



Data efficiency

	efficiency max delay	efficiency min delay
Hits sent to front-end	100 %	100 %
HitArbiter received hit from column	99.83 %	99.83 %
HitArbiter successfully assigns address	99.09 %	99.1 %
HitArbiter successfully assigns address or pileup info	99.76 %	99.80 %
Successfully assigned pileupAddress	0.67 %	0.66 %
Input to hitArbiter was not treated	0.07 %	0.03 %
Hits with double address bits	0.02 %	0.01%

all channels have constant latency

Table 4.1: HitArbiter Efficiencies. 100 % = 425714 hits sent to TDCpix front-end.

Time resolution studies

Timing resolution

- Laser: 75 ps RMS
- Test beam: 175 ps RMS

Random fluctuations of input current signal shape

- Position of track hit in pixel
- Charge straggling

Ongoing studies

- Track hit position
  - Position scan with laser: 85 ps RMS
- Charge straggling
  - > 60 ps RMS