Trends and Perspectives in Electronics for HEP experiments

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Acknowledgements to all my group, CERN, HEP colleagues.
None mentioned, non forgotten

Quick outline

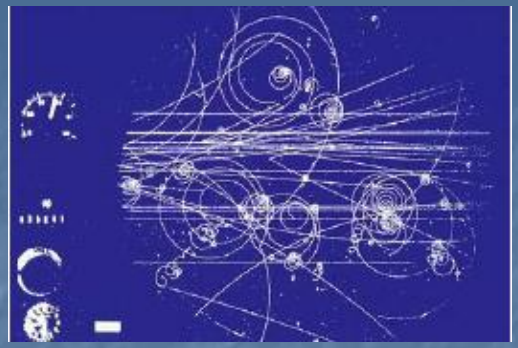
- History (past – now - future)
- Readout architectures
- Electronics required for different detectors
  - Pixels, strips, calorimeter , ,
- Electronics technologies
  - Integrated circuits, Interconnect, links, power conversion
- Our major problem: Radiation tolerance

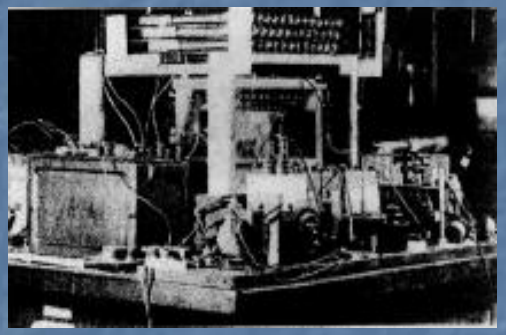
Past

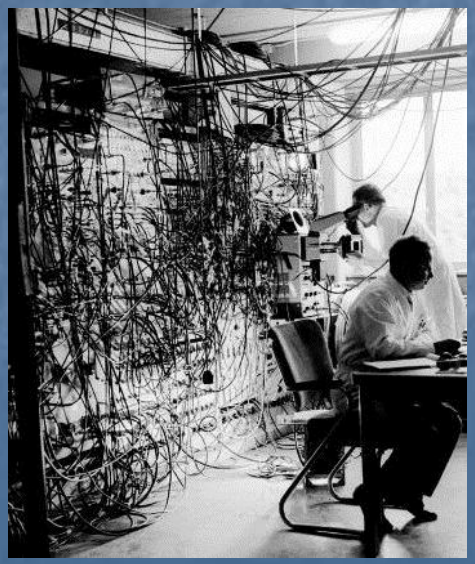
- Electronics has been one of the major ingredients to develop modern HEP experiments:
  - Improved performance: Position, Amplitude, Time , etc.
  - Lower noise
  - Higher channel counts
  - Higher integration: IC integration, low power
  - Higher readout rates
  - Sophisticated high rate trigger systems
  - High reliability
  - Radiation tolerance
  - DAQ is also electronics, but not any more "home made"

At affordable cost

- Extensive electronics engineering expertise required in HEP community

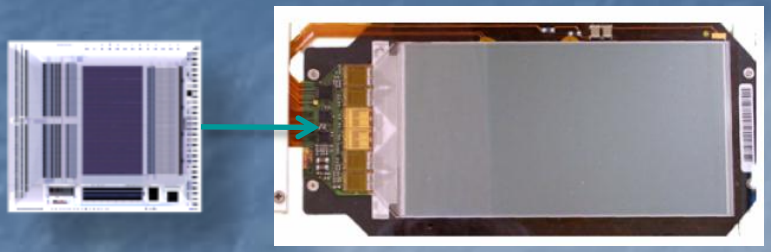






Now (the LHC experiments)

- Radiation "tolerant" Front-End electronics (cavern, muon, calorimeter):
  - 0.7um – 0.35um CMOS/BiCMOS ASIC's
  - Qualified COTS
- Radiation hard FE electronics (trackers)
  - **0.25um CMOS (Qualified standard commercial)**
  - 0.8um DMILL BiCMOS (specialized technology, phased out).
- Optical links
  - Custom TTC (Timing, Trigger and Control distribution)
  - Custom analog (CMS tracker)
  - Custom digital (GOL serializer, ATLAS tracker)
  - Commercial digital
- Power
  - Rad tol/hard linear regulators
  - Rad tol power supplies (cavern, calorimeters)
- FPGA's for fast and sophisticated trigger systems
- FPGA's/DSP/CPU's for DAQ interfaces
- Critical integration of electronics, detectors, mechanics, cooling
  - Required material for cables, cooling an unpleasant "surprise".
- A significant fraction of the cost and R&D needed to develop these experiments is in the electronics



Future HEP electronics

- Better resolution -> More channels-> Higher integration -> IC and interconnect technology.
- Low mass trackers -> Minimize cables, cooling, services -> Low power -> Low power IC technology and efficient power distribution
- Acquire more data at higher rate -> High density, high speed data transport -> IC technology and optical links.
- Hostile radiation environment -> Radiation hard technologies
- High reliability - > Efficient QA procedures
- Low error rates -> Well designed systems and IC's with SEU's immunity
- High speed flexible data processing -> FPGA based trigger systems, CPU based DAQ farms (assumed off detector)
- Large and complicated systems -> Well designed systems and critical sub-system integration -> Extensive system/sub-systems simulation/verification, Integration tests, Coordination.

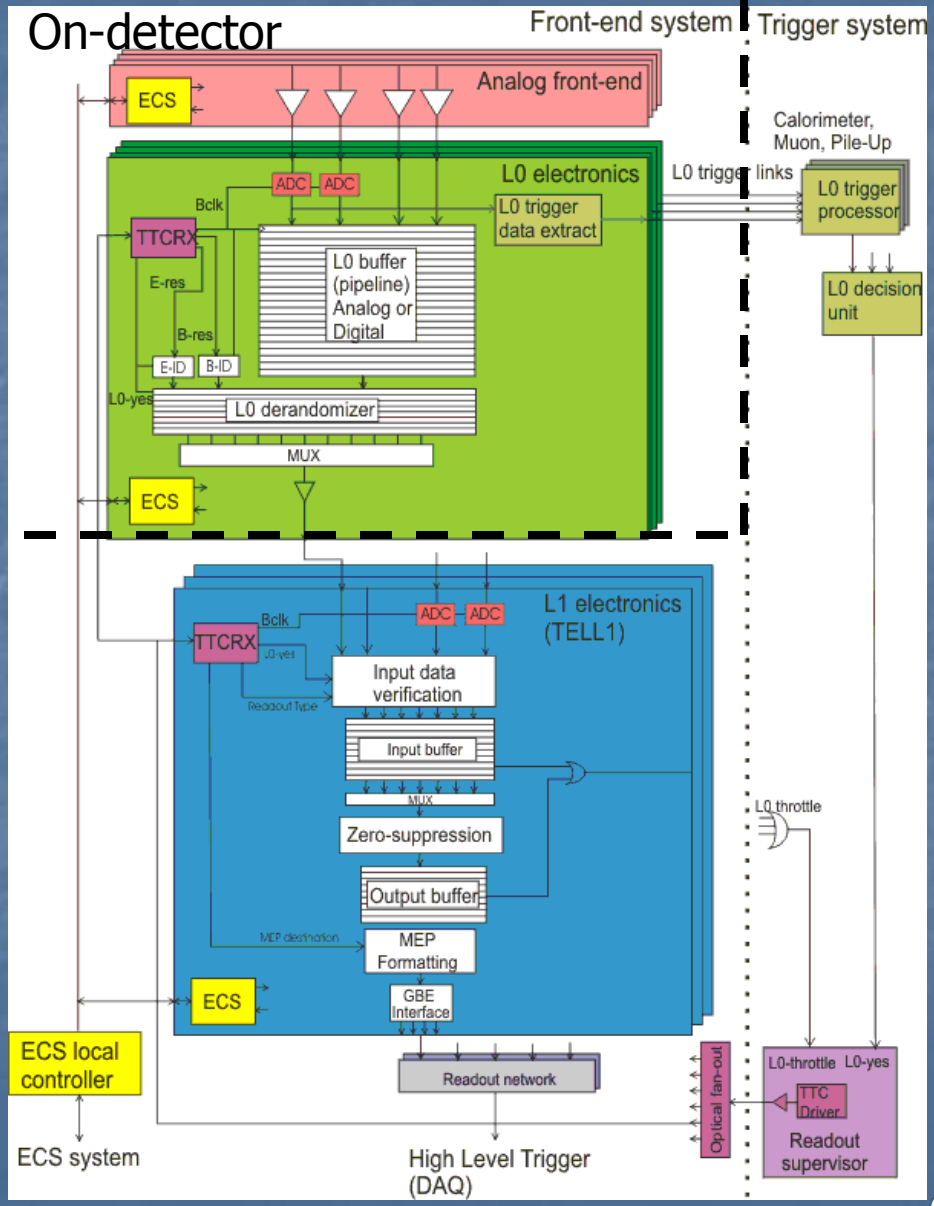
At affordable cost in a world-wide distributed community.

Electronics technologies for this must come from commercial market, but significant efforts required to adapt this to our environment: Radiation, low mass, mixed signal, integration, etc.

Global architecture I

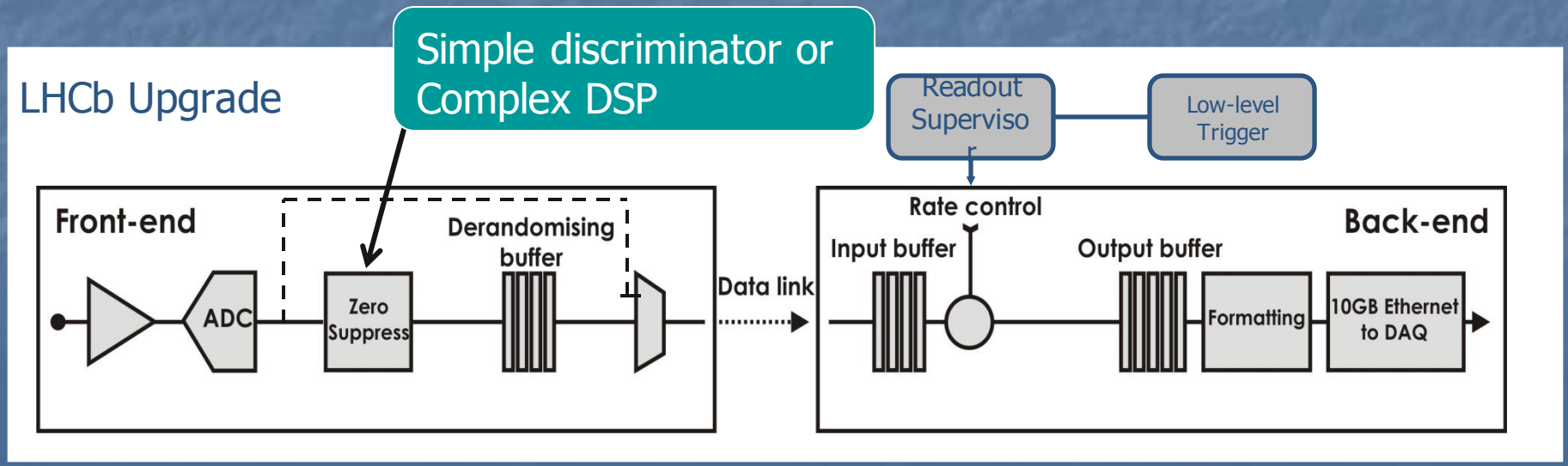
- Global front-end/readout architecture has major effects on electronics
  - Architecture in fact determined by electronics capabilities/limitations
- Triggered: Global event selection with local data buffering (and processing) to minimize readout data
  - Data buffering in hostile environment
  - Specific local processing (trigger towers, , , loss of flexibility ?)
  - (Local data sparcification/zero-suppression)
  - Complicated front-end systems
  - "Moderate" number of links

High rate experiments (LHCb, ATLAS, CMS,)



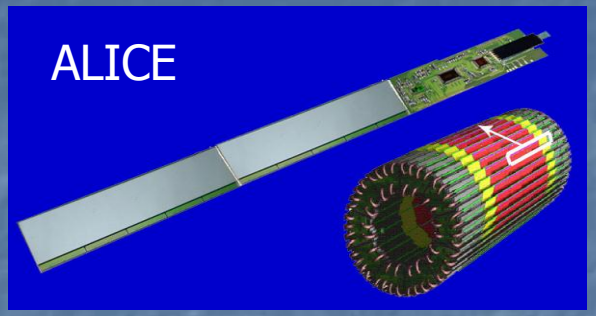
Architecture II

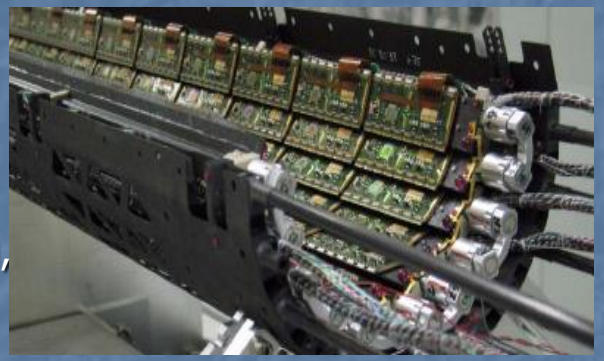
- Trigger less: Minimal local processing, high speed data transport
  - Send out all "raw" data ASAP
    A. Synchronously for easy pipelined event processing
    B. **Sparcified/zero-suppressed with time tag to minimize data (links)**
  - Simple high speed front-ends.
  - Large number(>10k) of data (optical) links
  - Flexible data processing in counting house using latest commercial FPGA's/DSP/CPU/PC (No radiation)
  - Moderate rate experiments (LHCb upgrade, CLIC/ILC, ,)

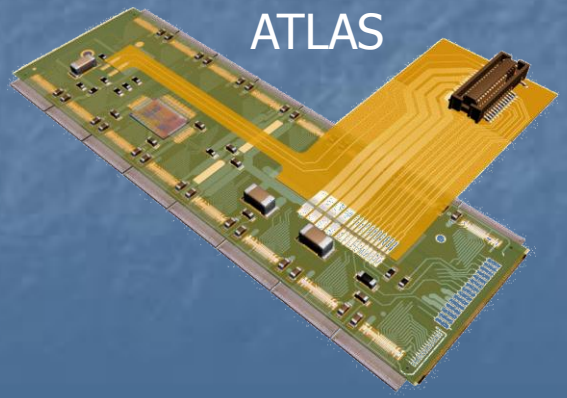


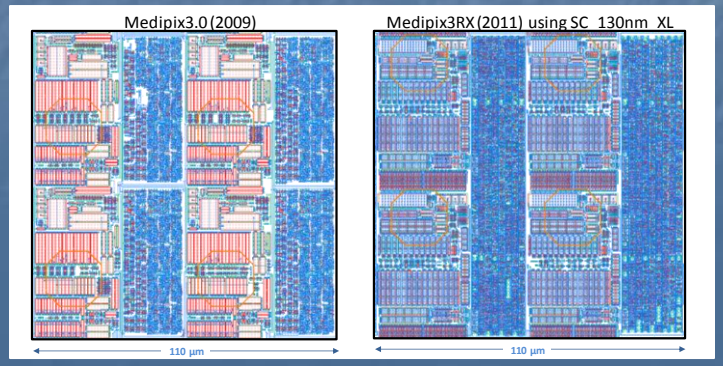
Pixel detectors

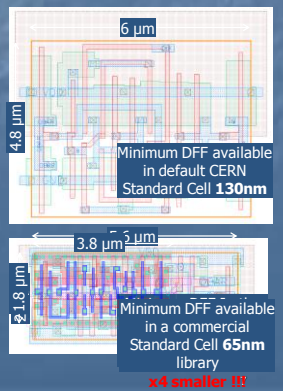
- Pixel detectors are our IC technology drivers as high integration level vital
  - Better resolution -> Smaller pixels, Higher integration
    - Binary versus analog (TOT) readout.
  - Smaller pixels -> Smaller capacitance -> Better S/N -> smaller analog power
    - Limited by pixel to pixel capacitance
  - More pixels, Higher rates (radiation), more features,, -> More logic per pixel -> Higher integration, **Low power** digital required
    - Material in today's pixel detectors are determined by cabling, power distribution, cooling, , , sensors, ASICs
    - Complicated digital pixels:
      Full custom -> Synthesized high density standard cells
      Pixel grouping





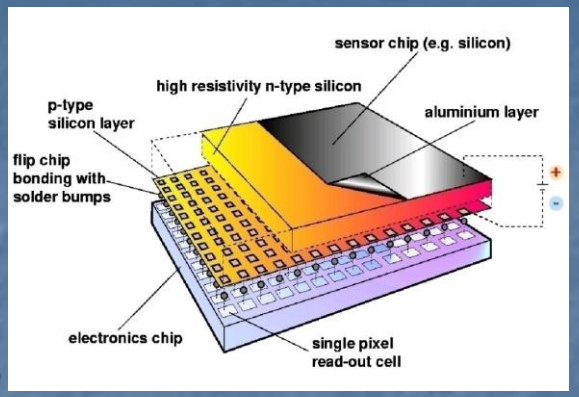


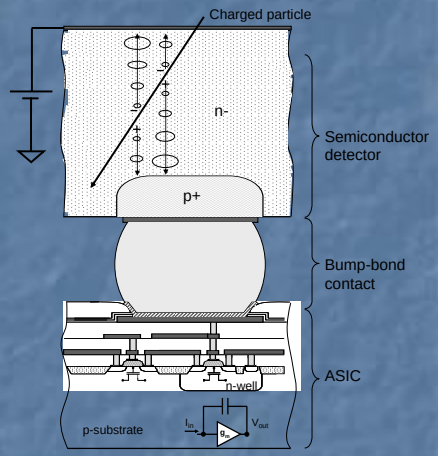


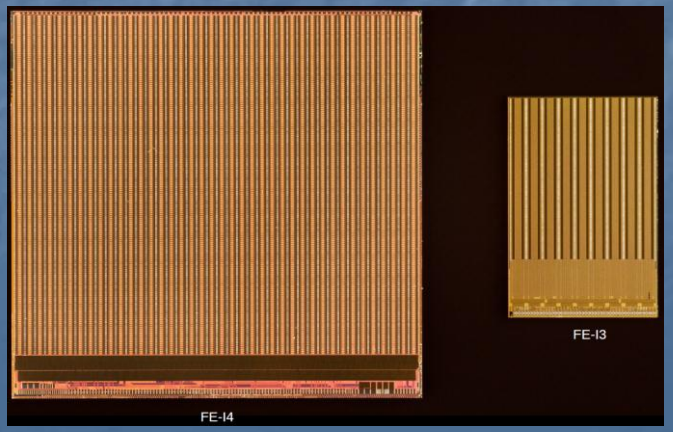


Hybrid Pixels

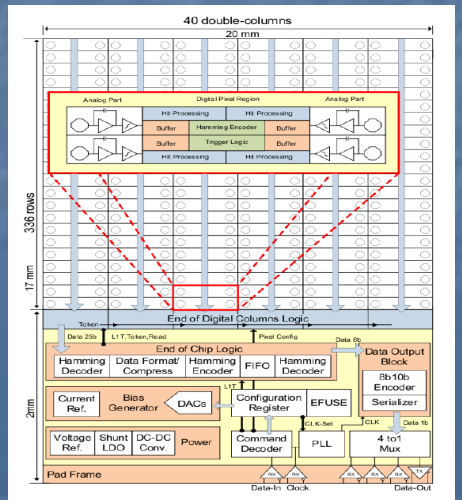
- Decoupled ASIC and detector technology
  - Standard high density ASIC technology
  - Dedicated sensor technologies (Si, 3D, Diamond, ,)
- High cost of bump bonding ASIC and detector
  - Multiple technologies under evaluation in HEP
  - Bonding technics from 3D IC technologies will hopefully bring improvements on this (more on 3D later)
- Material: Thinning ASIC to 50 – 100um
  - Delicate combination with bump bonding
- High radiation level and high rate applications.
- "Limited" by bump bonding, material, cost

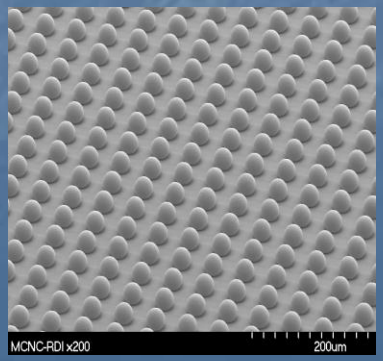






ATLAS FEI4 50 x 250um

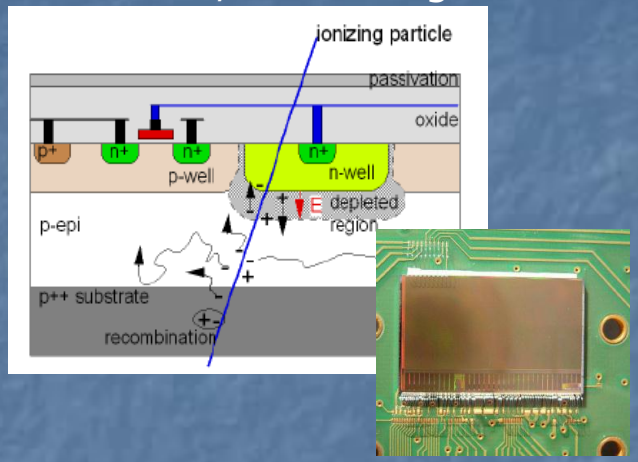




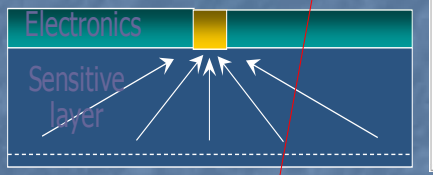
Monolithic Pixels

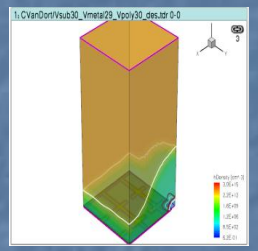
- Aim: Lower cost, Higher resolution, Lower mass
- Diffusion based : Charge collection (~100ns)
  - Epi (epitaxial layer), DEPFET (internal gate)
  - Relatively low rate and low radiation
- Drift based: SOI (KEK), LePix bulk triple well (CERN),
  - "HV" bias critical
  - Can possibly work in LHC environment
- Simple pixel cells (few transistors)
  - Significant boundary circuits needed.
  - SOI: Digital cells in pixel, Cross talk problems
- HEP needs 100% fill factor
- Stitching to make "large" pixel modules
- Challenges: Radiation tolerance, Speed, Rates: on-chip/in-pixel buffering/processing, technology dependence.

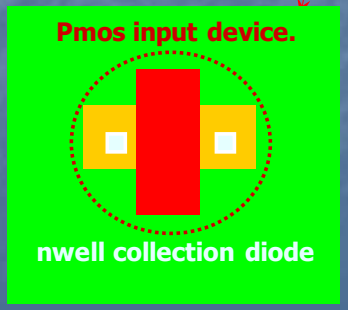
Mimosa, Strasbourg

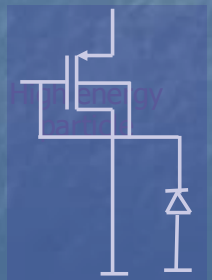


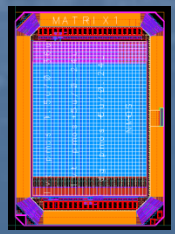
LePix (CERN)

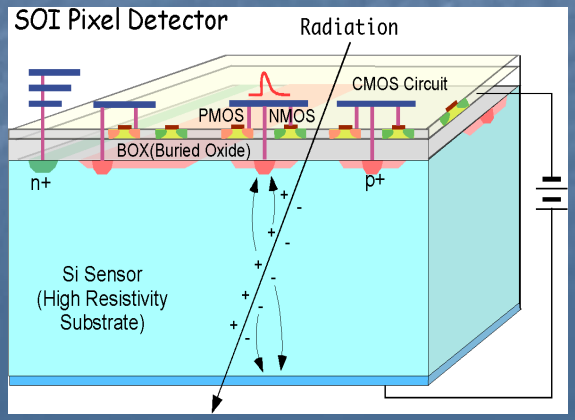


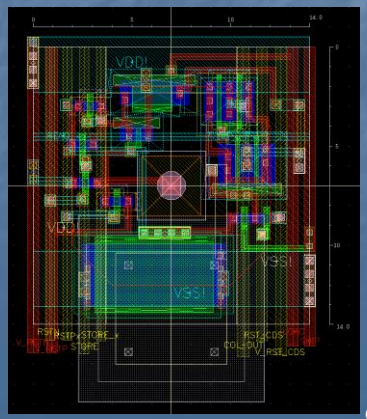








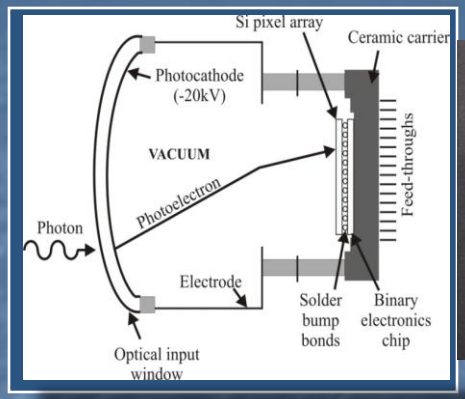


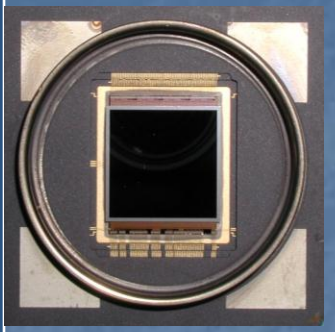


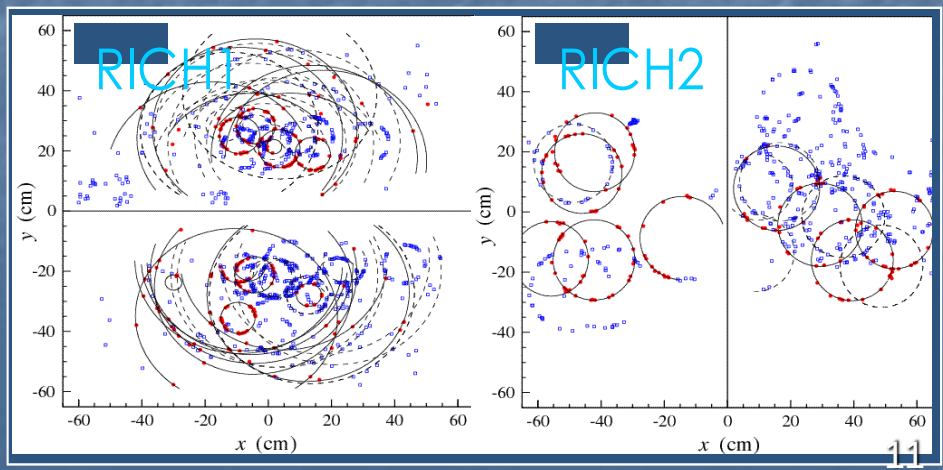
SOI, KEK

Pixel photon detector

- Integration of a pixel detector in a photon tube: Hybrid Photon Detector
  - Electrostatic acceleration and focusing of photon-electrons on pixel detector.
- Single photon detection in LHCb RICH
  - Very low noise
  - Same pixel chip as used in "classical" pixel detector in Alice
- Integration in vacuum non trivial (bake out, vacuum tightness, out gassing, etc.)
- Many potential applications using HEP pixel chips in HPD's, MCP, ,

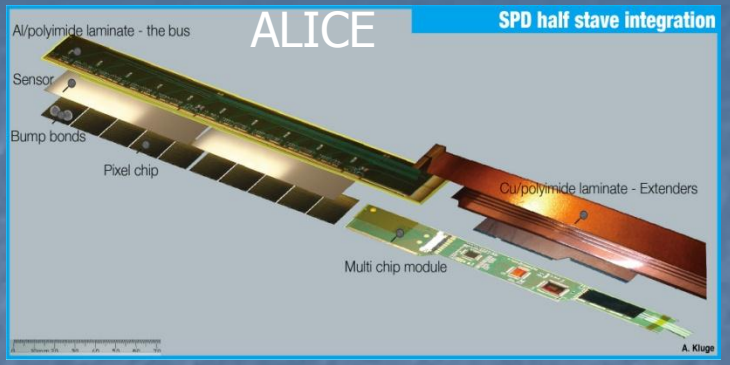


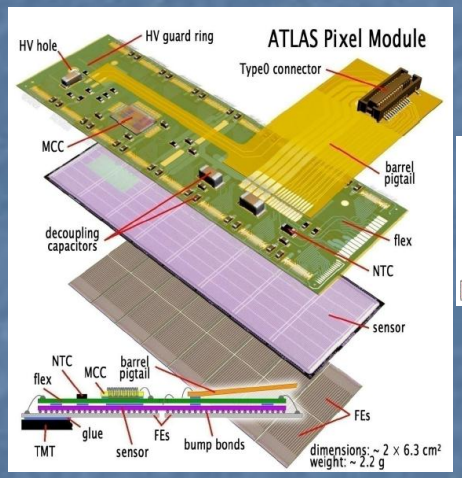


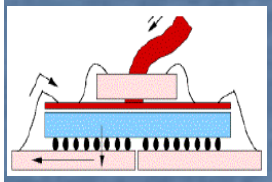


Building pixel systems

- Building low mass hermetic pixel detectors from relatively small pixel modules/assembles far from obvious
  - 100% coverage, Small assemblies, Modules, Power, cooling, readout, ,
- Ladders, modules, edgeless detectors, ,
- Future:
  - Stitching (to make very large pixel ASIC's)
  - TSV (Through Silicon Via's) to have abuteable pixel assemblies ?
    - TSVs are "surprisingly" difficult
  - Micro channel cooling ?







ATLAS

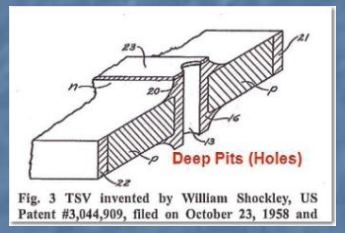
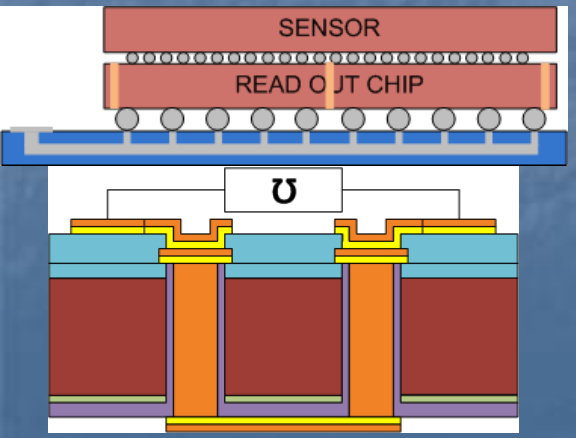
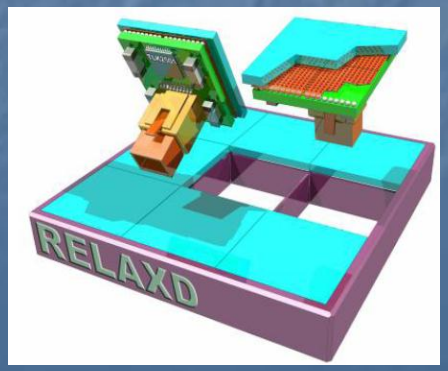
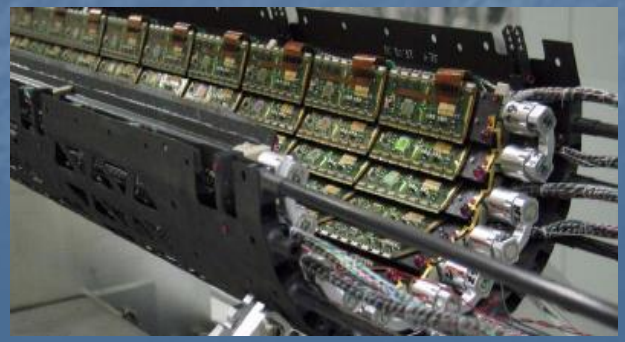


Fig. 3 TSV invented by William Shockley, US Patent #3,044,909, filed on October 23, 1958 and

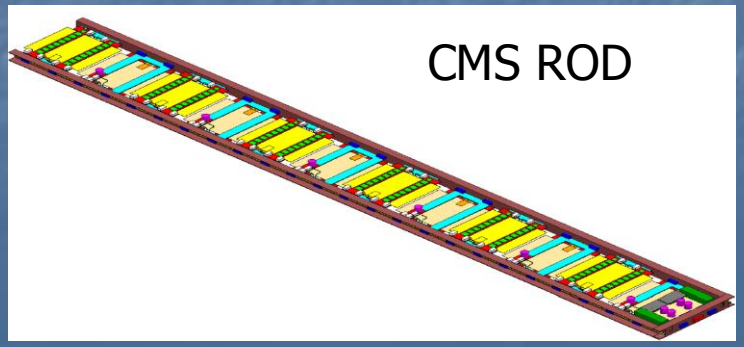


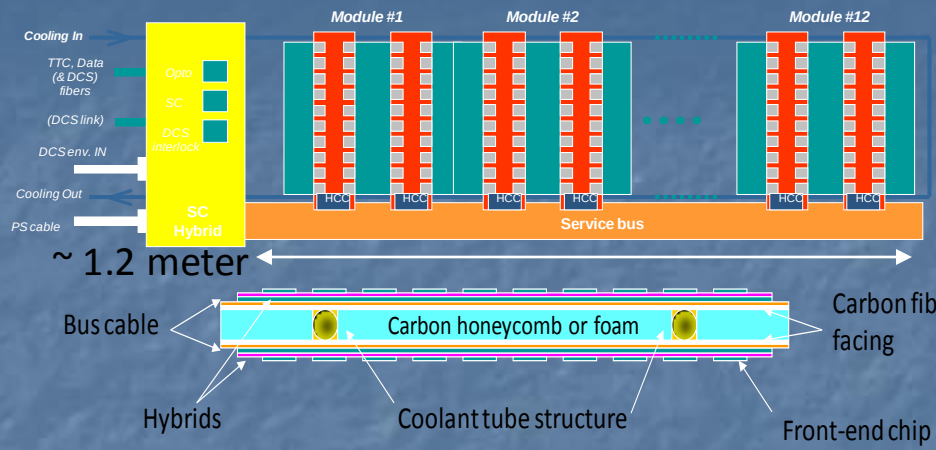


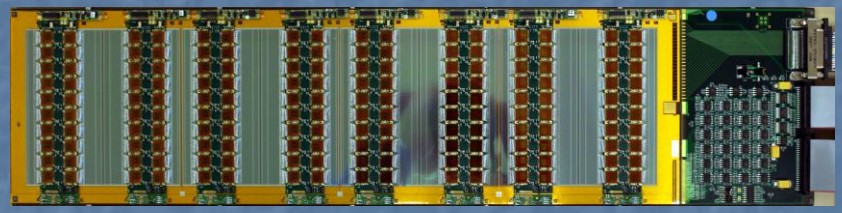


Strip detectors

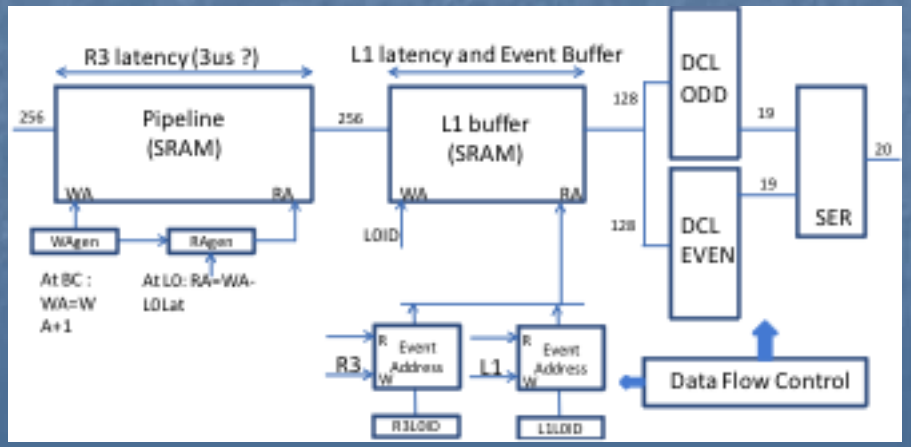
- High resolution tracking over large surfaces (Pixels impractical and too expensive)
- Ladders, long strips, short strips, strixels
- CMS and ATLAS upgrades: Binary.
  ALICE: Amplitude information
  - Analog power decreases when going to 130/90 nm. 65 nm may not give significant gain.
  - Digital power gets dominating so use of modern technologies gives lower power.
- ADC per channel in future ?
  - Very low power 8/6bit SAR ADC or TOT.
- Connection between FE chip and detector: **Wire bonding** or tap or bump ?
- Integration in stave/rod or petals ?
- Powering:
  - CMS DC/DC
  - ATLAS Serial power or DC/DC





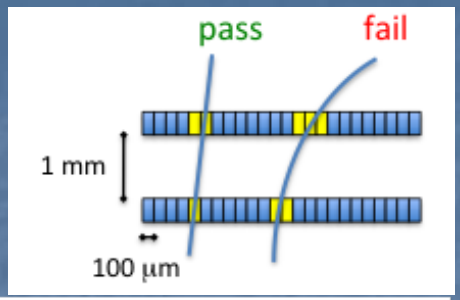


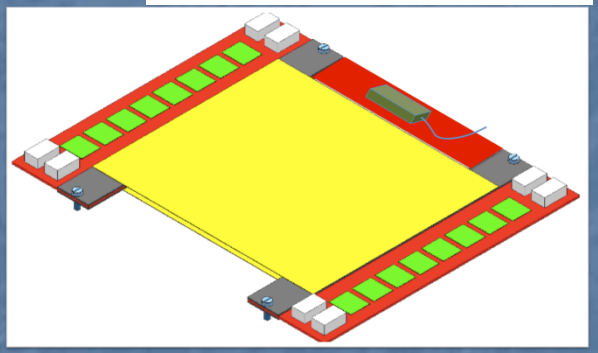
ATLAS stave

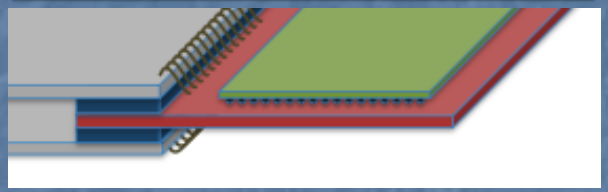


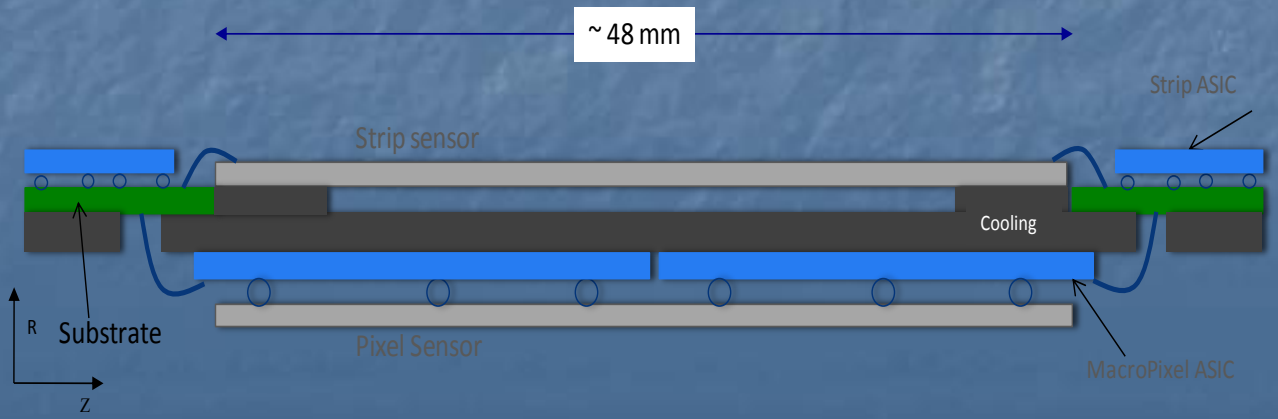
Combining pixel/strip trigger

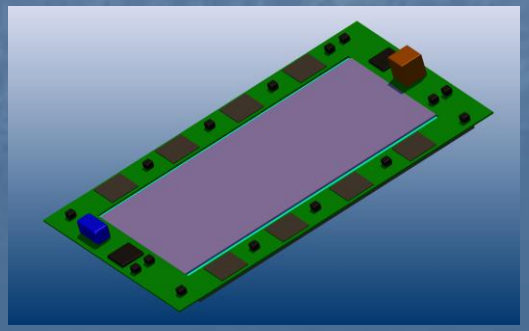
- CMS track trigger
  - At HL-LHC first level trigger saturates (if readout limited to 100KHz)
  - Include tracker Pt information in trigger
    - Send track information for tracks with high Pt.
  - Sufficient Pt resolution, short latency, bandwidth , ,
  - Double layer modules with correlation
    - Strips – strips in outer part
    - Strips – strixels /pixels in inner part (to get Z)
    - Critical: Low mass as not to destroy tracker resolution: Low power, high interconnectivity ,
  - Critical interconnect technology and module assembly





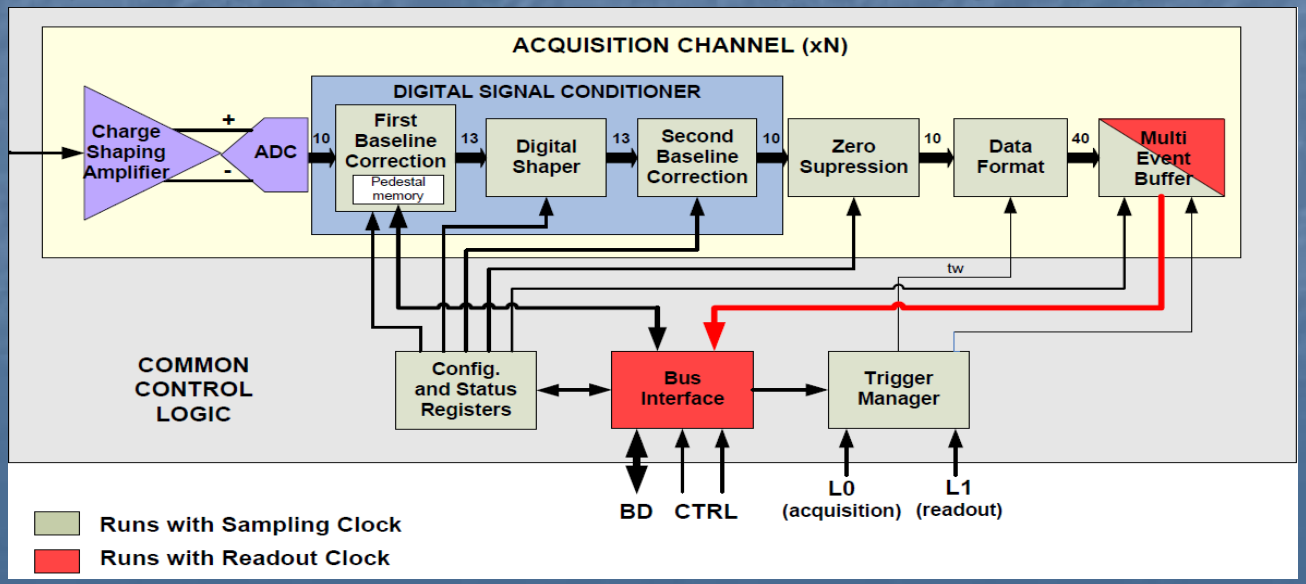






Full DSP approach

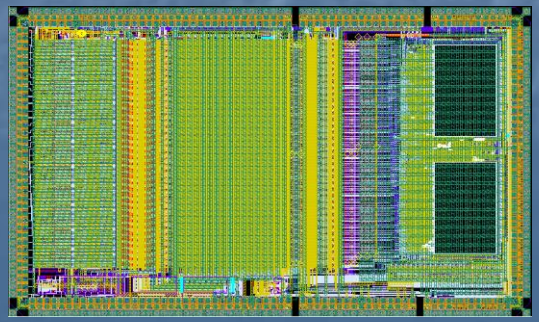
- The world is going digital: ADC plus powerful DSP processing can be integrated in front-end chip.
  - Digital shaping, baseline restorer, pulse detection, zero-suppression, time tagging, clustering, pulse parameter extraction, compression, buffering, link/DAQ interface
- Very low power ADC's extensively developed by industry over the last years.
  - Can be bought from specialized IP companies (do not develop ourselves if not required)
- DSP processing can be done at low power: modern technology, plus power optimized architecture and design.
- Required integration possible with modern technologies
- Example: S-ALTRO prototype: 16 channels, ~1W, 130nm CMOS
  - No significant crosstalk from digital to analog
  - Power dominated by home designed ADC (~60%)
- Realistic future aim: 64 channels, 12/10bits, ~1W.
  - Applications: TPC, GEM, Micromegas, calorimeters, ,
  - Pulsed power can reduce power considerable in certain applications (e.g. ILC/CLIC)

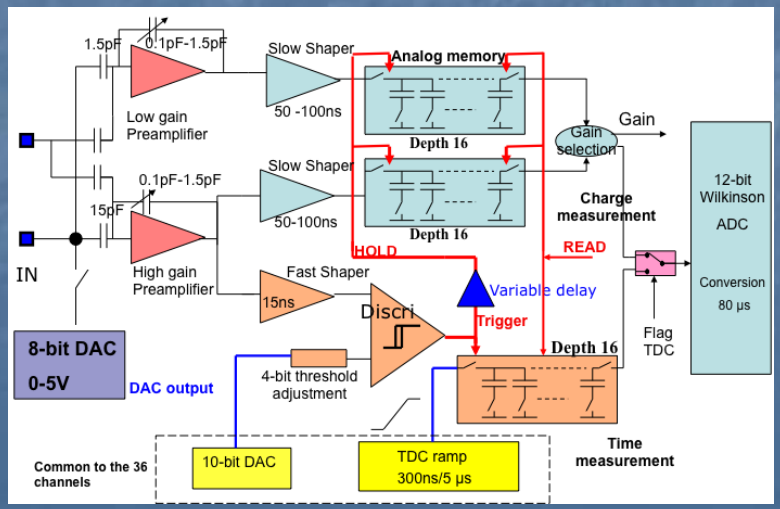


Calorimetry

- Large dynamic range: Low power, 40MHz 14/16 bit ADC's now available as standard multichannel chips and as IC IP's.
  - Good alternative to custom made multi range analog memories
  - Our usual problem: Radiation tolerance. COTS versus modified IP's
- Particle flow: Many channels (10^8), lower resolution per channel, Low power critical (power pulsing in ILC/CLIC)
  - CALICE (ILC) currently using multi gain multilevel analog memories (low power, low cost)
  - Multichannel ADC/DSP seems promising for this in the future (R&D cost).
- Parallel high speed optical links now makes it viable to perform direct ADC in front-end and send all raw data to off-detector processing for "classical" calorimeters.
  - Allows very flexible FPGA based calorimeter trigger systems
  - Original CMS Ecal architecture, but abandoned because of cost/implementation of the ~100k links.

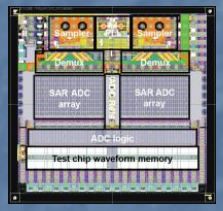
SPIROC,
Omega – In2P3
CALICE

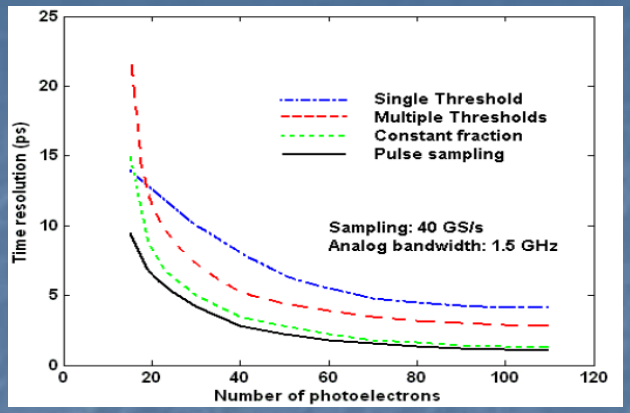




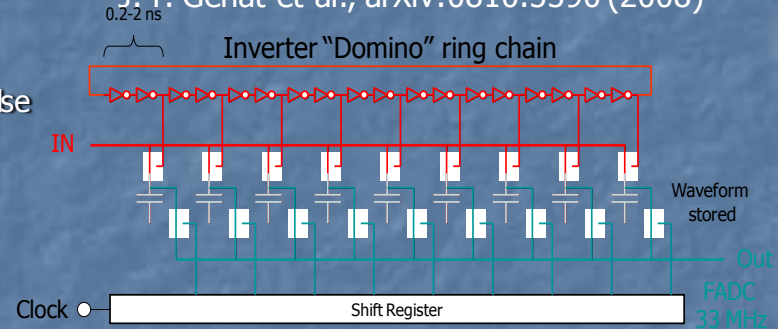
Timing detectors

- High channel count, very high time resolution (~10ps) detectors become feasible with modern micro electronics and novel detectors
- TOF and RICH detectors based on MCP, SiPM, MRPC or MAPMT
  - Examples: Torch for LHCb upgrade, FP420, HPS
- Fast ADC's: 55GHz, 8 bit, 2W
  - How to deal with the massive data flow and power?
- Fast analog memories: 1 – 10GHz Sampling, <1GHz bandwidth
  - High time resolution with software pulse fitting to known reference pulse
  - Multiple chips available in community: PSI, LAL, Hawaii - Chicago,
  - Limited number of channels, limited memory, power, external ADC
- TDC with Constant fraction or TOT time walk compensation (ALICE TOF) .
  - ~ps TDCs feasible in modern IC technologies
- Very high speed circuits now possible with limited power, but requires fast detectors



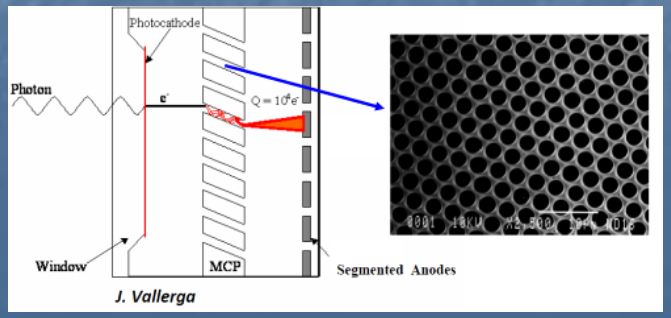


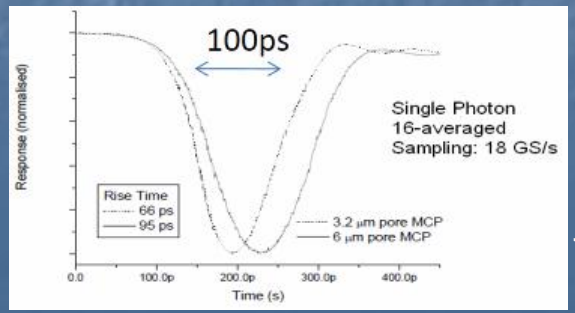
J.-F. Genat et al., arXiv:0810.5590 (2008)



S. Ritt, PSI

"Time stretcher" GHz → MHz

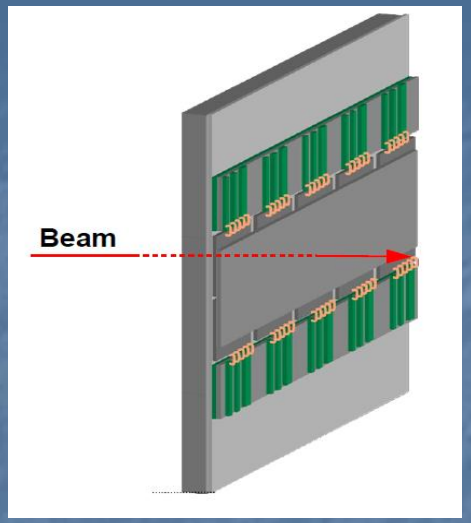


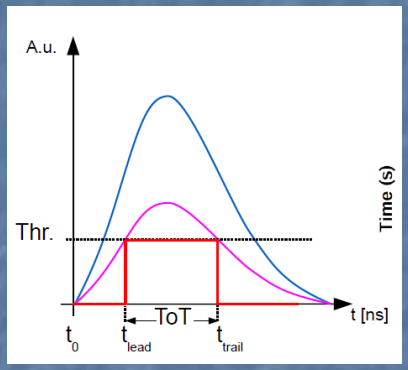


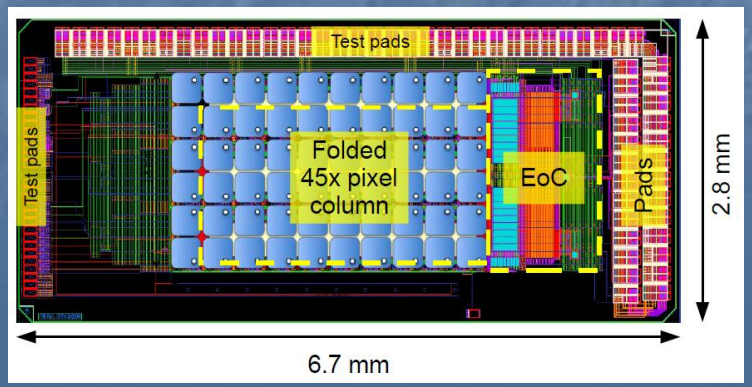
J. Milnes, J. Howoth, Photek

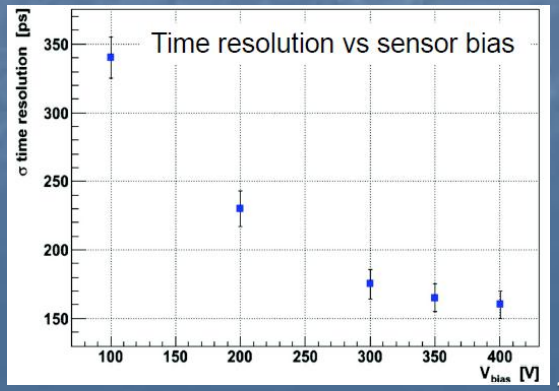
NA62 GTK

- 300um x 300um pixel detector with ~200ps resolution (ASIC: 75ps)
- 3 stations (10 ASIC's, 1 pixel sensor) with very high particle rate: ~1GHz
- Time walk compensation with TOT (or CFD)
- High radiation levels (secondary beam goes straight trough)
- Demonstrated in beam test with 130nm prototype
  - Final 40 x 45 pixel array ASIC/detector planned for 2012
- Pixel detectors with this kind of time resolution can open up new applications of pixel detectors in HEP, medical, material science, bio chemistry, , ,
- What determines ultimate time resolution with silicon pixel ?
  - **Signal variation across pixel, signal/noise, Signal generation in silicon itself** (e.g. 3D detectors)
  - Pixel ASICs and requirements for "low power"





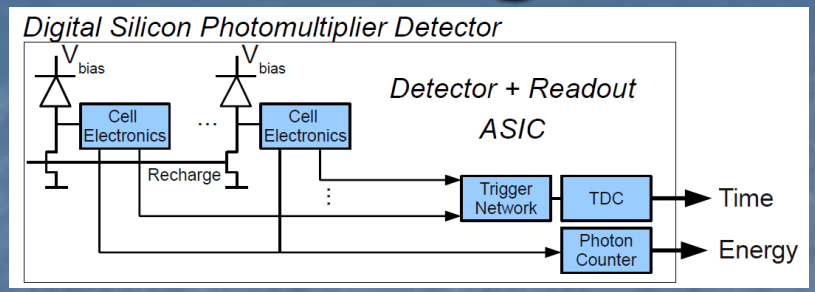


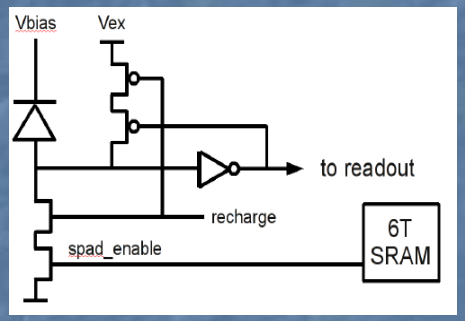


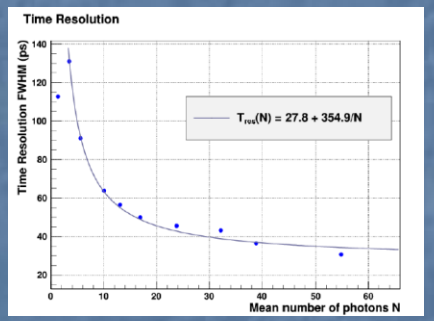
Digital Photon counting

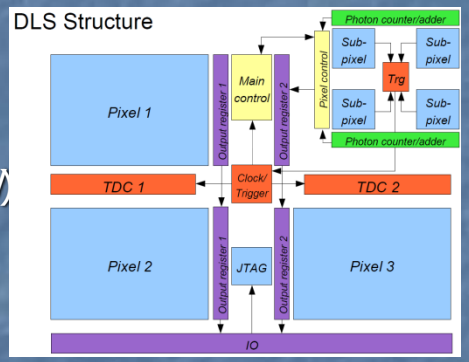
- Single photon counting with SPAD/GAPD array with integrated electronics
  - Use of "standard" IC technology
    - SPAD bias only needs a few volts
  - Optimization of SPAD cell took significant efforts and many trials
    - Dark count rates, cross talk, detection efficiency , ,
- Photon counting, High time resolution
  - 32 x 60um micro-cells/pixels
  - Up to 80% fill factor
  - Integrated TDC, readout, configuration , ,
- Enormous effort in development
  - Foundry (NXP 180nm) and user (Philips *medical*) originally part of same large company
  - Aimed at applications with very high system costs (medical scanners)
  - Investment that will be very hard to find in HEP for such a monolithic detector-chip
- "Open" to let HEP use their technology

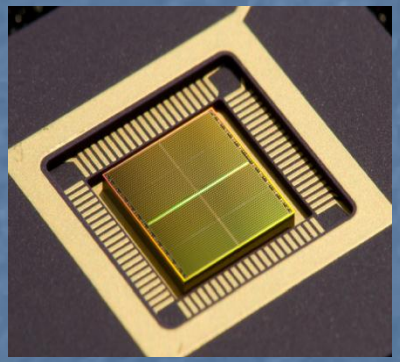
PH detector seminar:
https://indico.cern.ch/conferenceDisplay.py?confId=149010

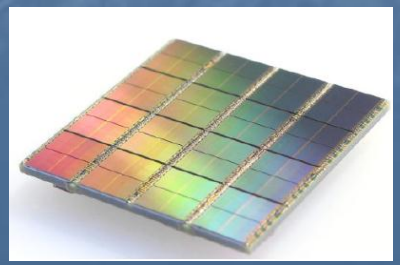








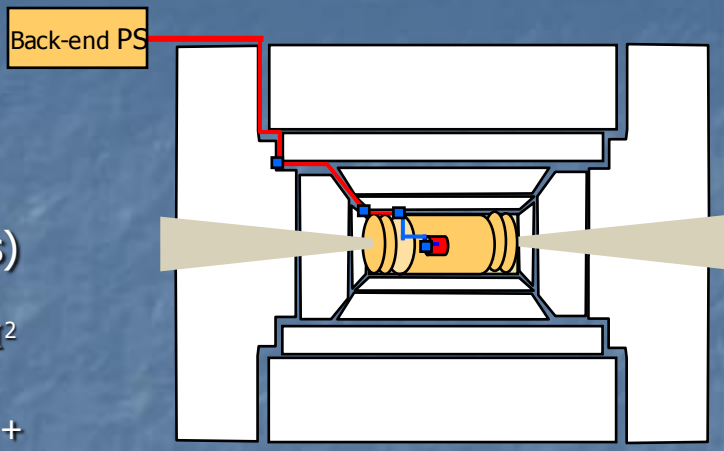


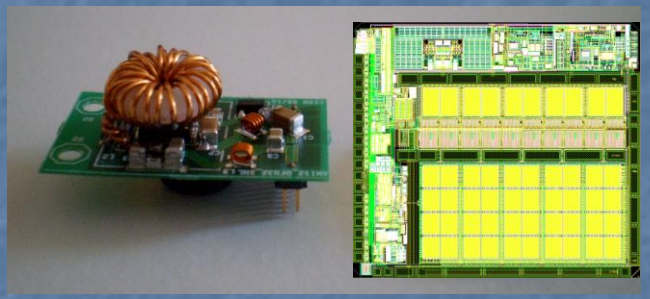


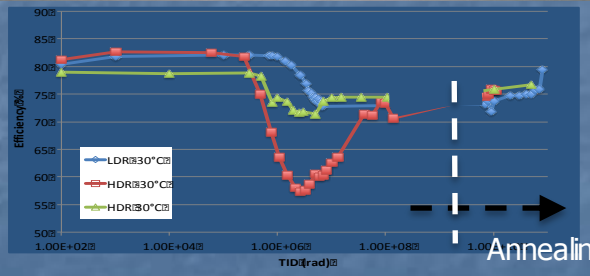
T. Frach, Philips

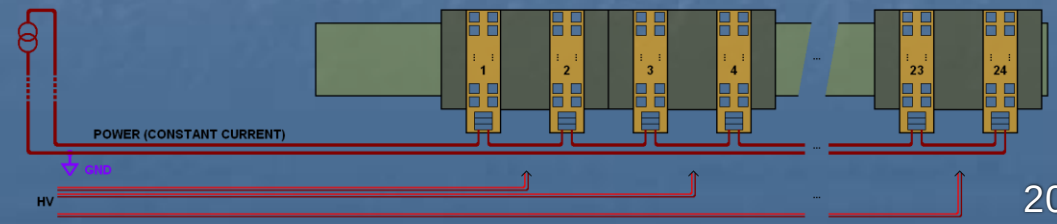
On-detector power distribution

- Distributing low voltage power in large experiments, without local power conversion, impractical/impossible
  - Voltage drops -> power loss –> large cables -> material
- Modern technologies use lower supply voltages: 5V, 3.3, 2.5, 1.2, 1.0V (down side of new low power technologies)
  - Upgrades: Assume same total power (as more channels) the power supply currents will increase and power loss in cables increases with I^2
  - Local power conversion becomes a must.
  - Power conversion must occur in very difficult environment: Radiation + magnetic field + minimal power dissipation + minimal mass.
- DC/DC: Inductive (module), Capacitive (on-chip)
  - High input voltage (low cable currents), high efficiency
  - IC technologies that can stand high voltage are not radiation tolerant
    - Compromise: Medium voltage (10v) but still problematic
  - CERN develops Inductive and capacitive DC/DC conversions
    - Radiation tolerance of technology a critical issue (two promising technologies used)
    - Shielding and appropriate EMC handling critical but have been successfully verified on silicon strip detector modules
- Serial powering: Distribute current and generate locally voltage. Tested by ATLAS SCT.
  - Grounding and fault isolation delicate
- Power pulsing: significant gain possible for certain experiments (ILC/CLIC)



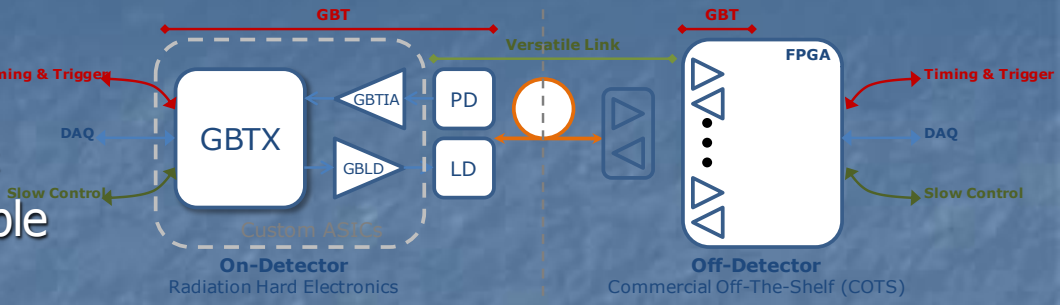


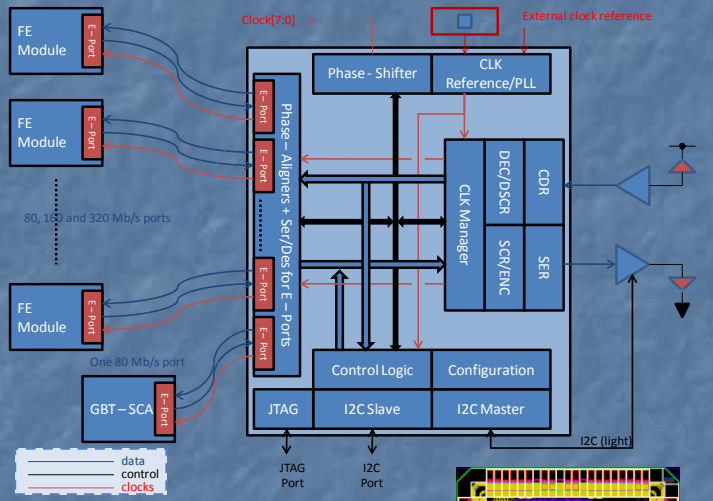


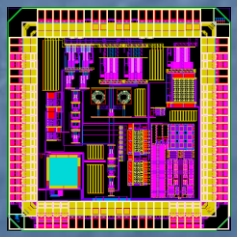


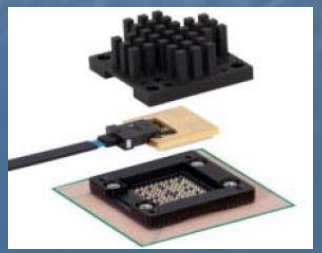
Optical links

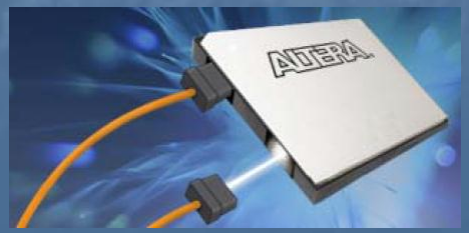
- Information types :
  Readout, Trigger, Timing, Slow control,
  - Past/current: Separate links
  - Future: Merge all in one bidirectional optical link
- Must be high speed and highly reliable
  - Redundancy in critical cases
- Radiation problems:
  - Laser deterioration
  - PIN receiver deterioration
  - Induced multi bit error signals in PIN by particles. Use of extensive forward error correction.
  - SEU's in electronics circuits
- Versatile / GBT link project
  - Identify and qualify appropriate Lasers and PINs
  - On-detector rad hard chip set:
    Laser driver, Pre-amplifier, interface chip (GBTX), control chip.
  - Off-detector: Commercial Opto and FPGA's
- Parallel links for high data rates
  - Custom array transmitters/serializers (ATLAS)
  - Fiber ribbons
  - Commercial array receivers (optical engines)
  - FPGA deserializers

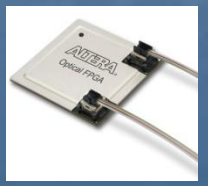










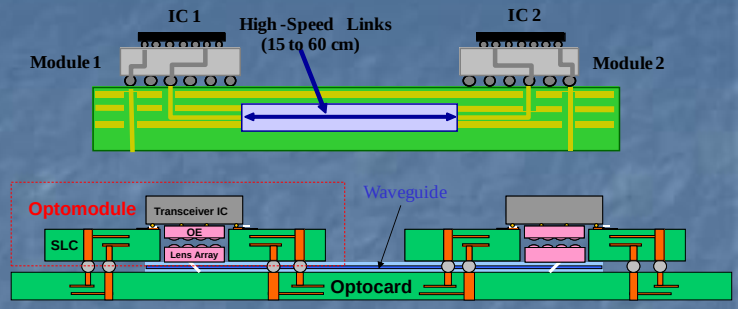


CMOS photonics

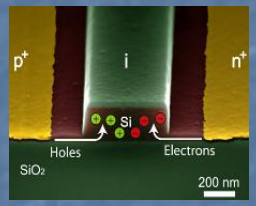
- IO is becoming critical bottleneck for high end multi-core CPU's servers (CPU <–> Memory)
- Now: High speed electrical serial connections
- Future: Hybrid optical chips/links
- Dream: Integrating opto electronics in (on 3D) Integrated circuits
  - On-chip optical modulators, waveguides and receivers (laser source problematic in Si)
  - Available when ?.

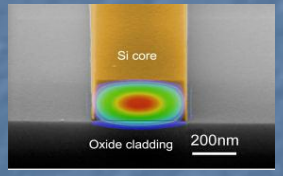
Electrical links are still more cost efficient (power) for short connections

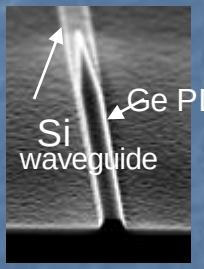
- Dream for HEP: Each Front-end chip has an optical output. Many challenges
  - Radiation
  - Access to technology
  - Cost of technology
  - Design complexity of such mixed technology



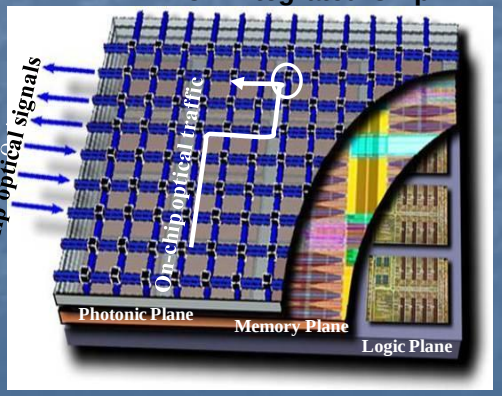
Has been demonstrated
(Sophisticated 3D packaging)







3D Integrated Chip

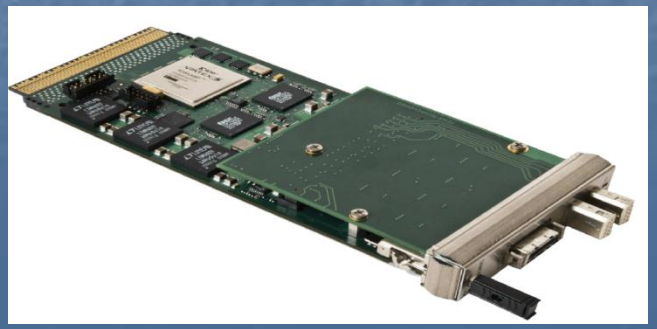


Dream

M. Ritter, IBM, TWEPP2010

Off detector

- FPGA's: Fast, flexible , , , The perfect devices for HEP when no/limited radiation.
- CPU's/DSP: Mainly for DAQ interfaces
- Mixing FPGA's, DSP, CPU's on one module
  - Can give very high performance and very flexible modules but implies a huge investment in firmware (FPGA, DSP, CPU, operating system, , ,)
- Crate based
  - Not (slow) shared parallel bus (e.g. VME)
  - Switch fabric: Multiple high speed serial links on backplane to centralized switch/controller
    (High speed LAN on backplane)
  - Power, cooling, front-panel, standardization but flexible, hot swap, reliable, affordable
  - ATCA, uTCA, VXS (VME with extra serial link connector) are major candidates for HEP
  - ATCA and uTCA gets increasing interest by HEP community (uTCA for physics standardization)
  - Trigger systems, DAQ interfaces
- Plugged into computer: PCIe, ,
  - Can in certain cases skip crates (e.g. link to front-ends)
  - Poses a challenge to keep up with changing PC's



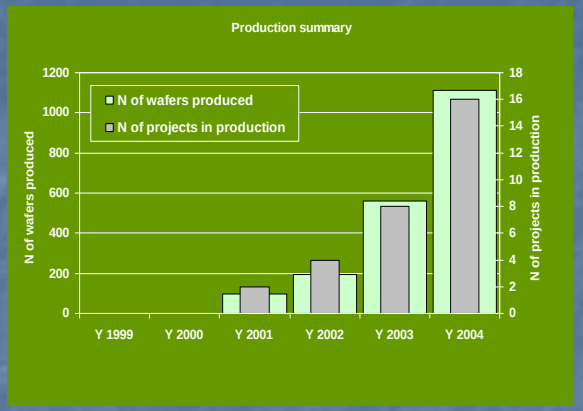
IC technology for HEP

- Critical to make required front-end systems
- What we want:
  - High integration level
    - This exists (e.g. 22nm) but hard for us to access because of problems below
    - The most sophisticated technologies may not even be technically appropriate for us.
  - Appropriate for mixed analog/digital designs
  - Radiation tolerance: >100Mrad
    - Non trivial and requires significant effort to find and qualify technology
    - Use special design approaches (and special libraries).
    - Rad hard IC's may have very strict export restrictions.
  - Affordable access
    - Sophisticated technologies have very high masks costs but is relatively cheap to produce in very large quantities (exactly the opposite of what we need)
    - We may even not be allowed access ,as too small a client.
    - Regular MPW runs vital to share mask costs for prototypes and small scale production
  - Easy to use for relatively small HEP IC design groups
    - Modern technologies and tools get more and more complicated
  - Extensive libraries and IP
    - IP blocks often exists, but may be unusable to us because of radiation (& "too" expensive)
    - Our community has a tendency to make all our selves (limited funding in R&D phase, manpower available, must keep students occupied , ,)
  - Available for long time (+10years)
    - This may not be the case for certain technology nodes (select strong nodes, bet on the right company)

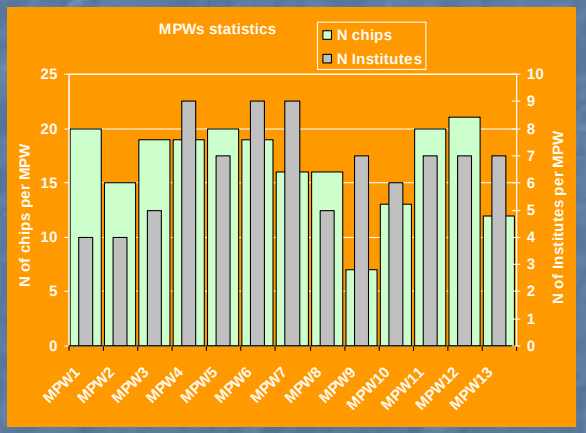
IC technology

- HEP options
  - Use easily accessible, cheap and mature technologies (e.g. AMS). Life time ?, rad tol ?, Limited integration)
  - The community gets together (e.g. via CERN) to use one "modern" technology from a strong technology node, radiation qualify this and get/develop required libraries and tools.
    - LHC: 250nm CMOS (IBM)
    - LHC phase 1 upgrades: 130nm CMOS (IBM)
    - LHC Phase 2 upgrades: 65nm CMOS

    Skipping every second node because of long HEP project schedules and limited resources to import/qualify technology.
  - Join with similar communities (e.g. EU Europractice)
  - (Specialized technologies: "HV" for DC/DC, monolithic pixel, CMOS photonics, ?)
- Learning how to use these technologies
  - HEP/CERN community
    - Training sessions in use of technology and related tools
    - Micro Electronics User group
    - Micro electronics User exchange (yearly 2 day event)
  - Euro-practice has extensive training program on tools and technologies

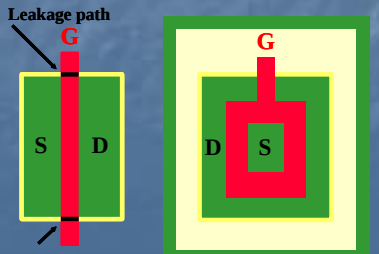


250nm CMOS

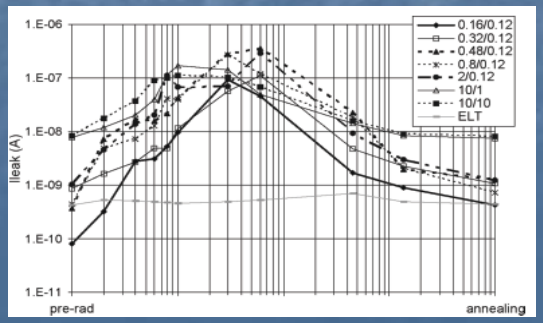


Next IC technology for HEP

- 65nm seems to be a promising/realistic technology for future long term HEP developments (e.g. LHC phase 2)
  - Well established ~10 year old technology
  - Confirmed to be a strong node
    - Extensively used for many long term components (Industrial, Automotive, Space, etc.)
  - Affordable
    - Small MPW submissions: 50 – 100k CHF
    - Dedicated engineering run: ~2 x 130nm = ~1M CHF
  - Still uses classical "SiO_2" as gate insulator
  - Excellent radiation characteristics
- To be finalized
  - Appropriate Libraries & tools for HEP institutes
  - Frame contract (team up with Euro-practice)
    - Access conditions: MPW, production
- Do we need and can we afford/manage more modern IC technologies ?

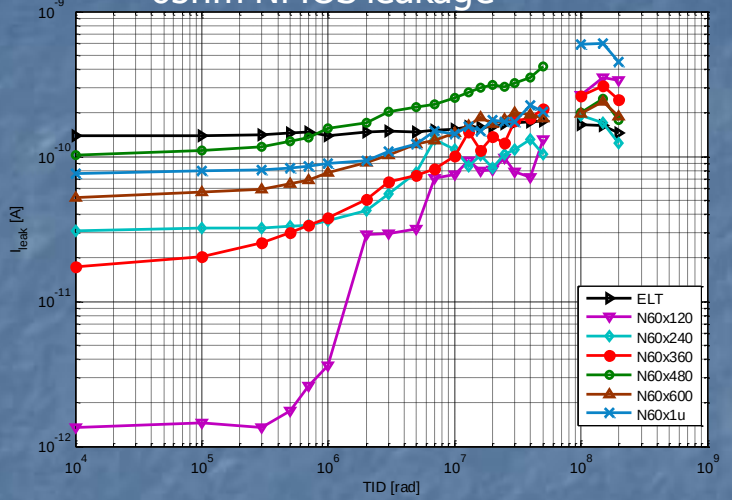


Edgeless transistor (ELT)
Used in 250nm CMOS

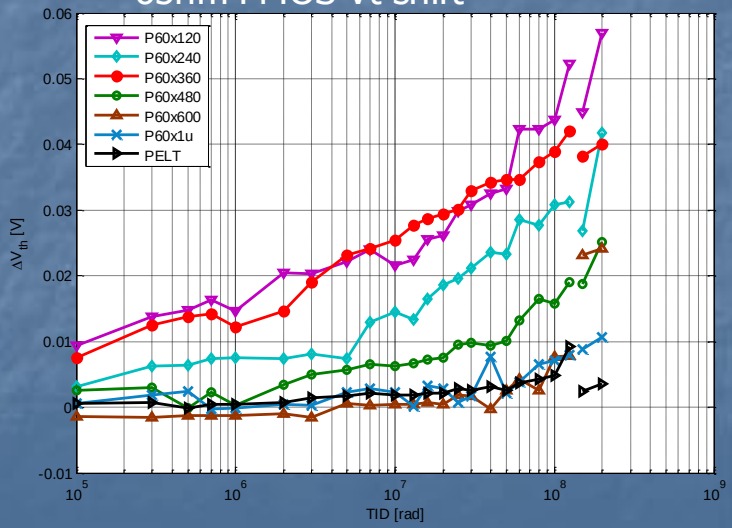


130nm NMOS leakage

65nm NMOS leakage

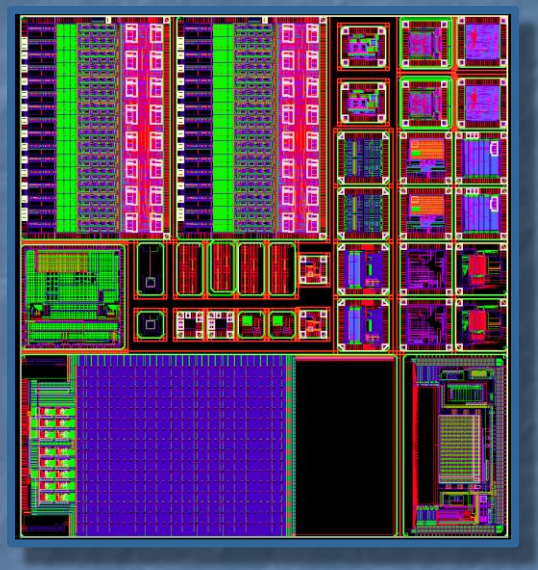


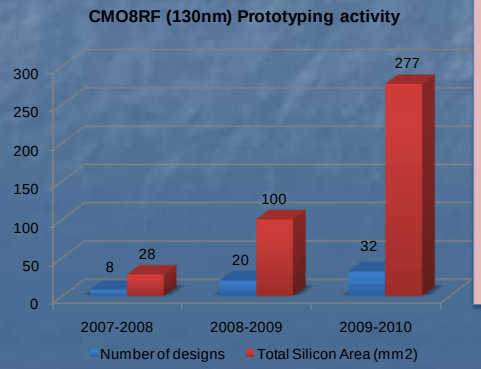
65nm PMOS Vt shift

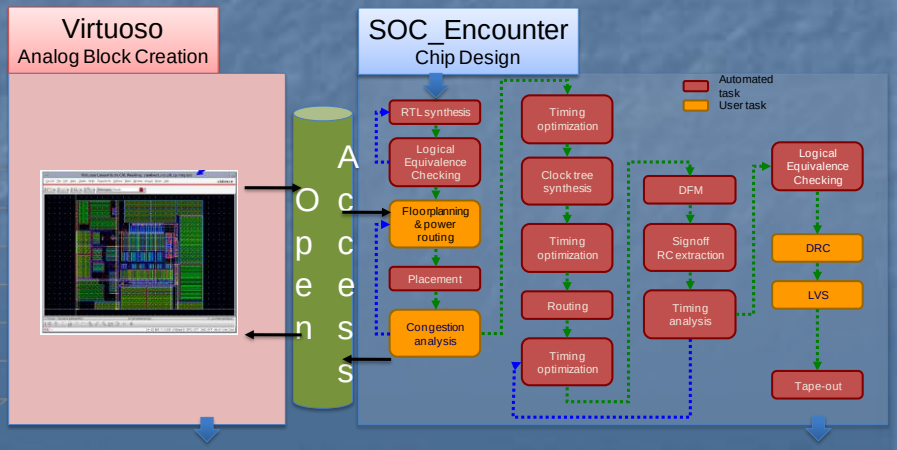


IC tech from CERN

- 250nm, 130nm, (90nm) and 65nm coming
  - 250nm: workhorse for all rad hard circuits in current LHC experiments
  - 130nm: LHC phase 1 upgrades
  - 65nm: LHC phase 2 upgrades .
- CERN supplies/organizes:
  - Technology selection and rad qualification
  - Frame contract and MPW access
  - Design kit, Libraries
  - HEP users: ~50 world wide institutes
  - 5 day training, 7 courses, 70 Engineers

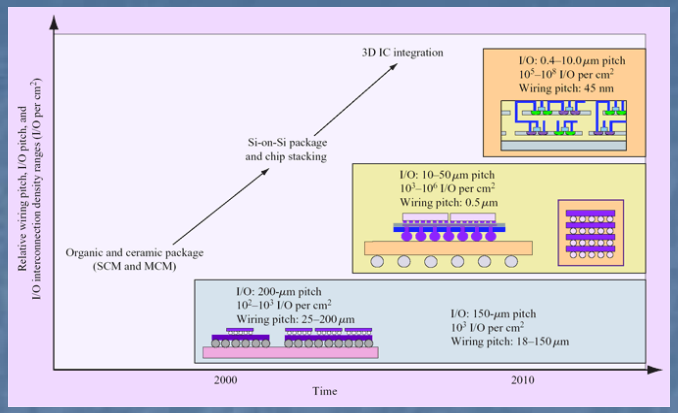


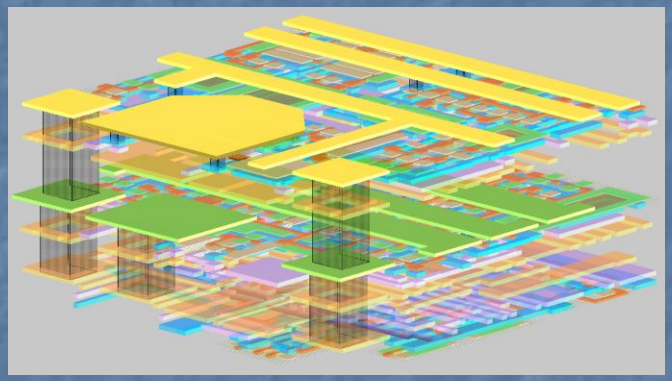




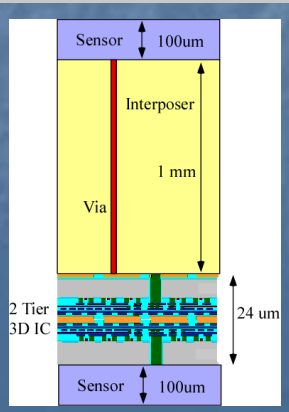
3D IC technologies

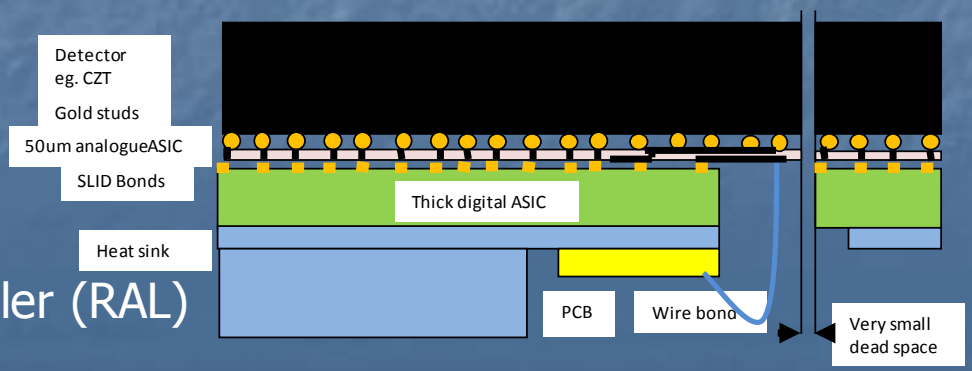
- Dreaming about the perfect 3D IC technology
  - Affordable, Accessible, Reliable, High yield, ,
  - Mixing technologies (Analog, digital, sensor)
- Several HEP institutes teamed together to get access to Chartered/Tezzaron process
  - Chips have been in the pipeline for several years
  - Very low yield
  - TSV Technology have now been modified
  - We may still need to wait for this to mature
- Will 3D IC become available (to us) ?
  - Before IC technology hits a technology wall (10nm ?)
    - Why use 3D in 130nm when one can "easily" migrate to 90/65nm ?
    - Yield is a major problem
  - One obvious candidate: Stacking of memory chips
    - This is more 3D packaging as only coarse TSVs needed at boundary
    - Memory chips have redundancies





Fermilab

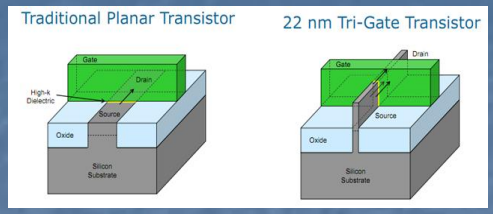


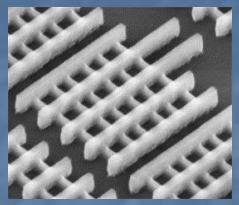


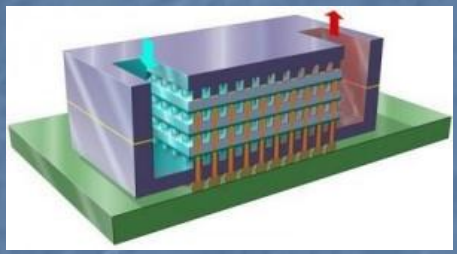
Paul Seller (RAL)

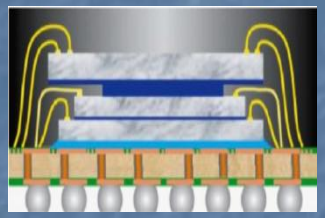
3D technologies

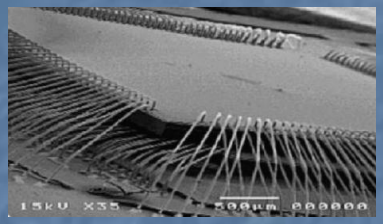
- 3D is fashion, but be careful with confusion between different 3D's
  - 3D transistors (Intel 22nm technology)
    - To be capable of continuing Moore's law without excessive transistor leakage.
      - Controls current flow from ¾ sides of transistor
      - 37% speed improvement from previous technology (32nm) or half power at same speed
      - Expected to scale down to <10nm
    - We can not get access or afford this for many years
    - Alternative: Fully depleted SOI (Silicon On Insulator)
  - 3D IC's
    - Multiple active layers connected with (small) TSV
  - 3D packaging/integration
    - Stacking chips on top of each other using:
      - Wire bonding
      - Bump bonding
      - TSV + bump bonding
  - 3D detectors

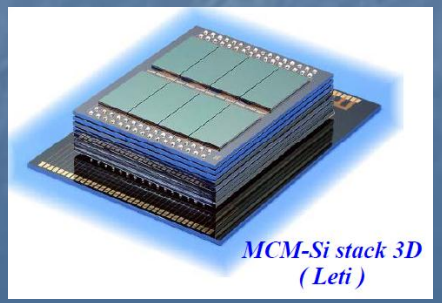


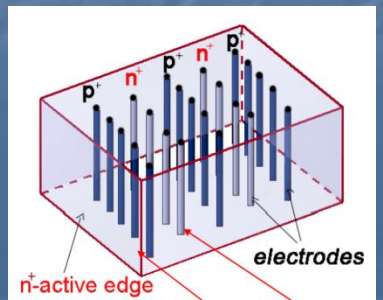






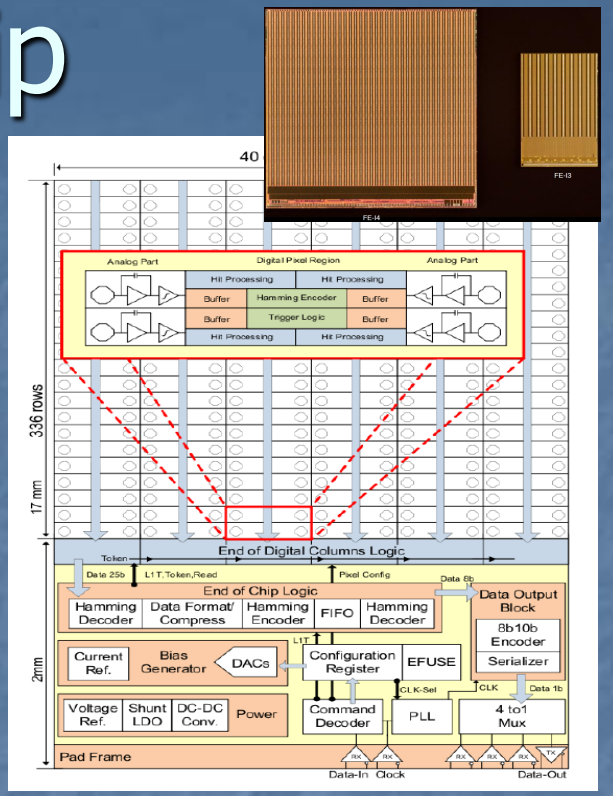


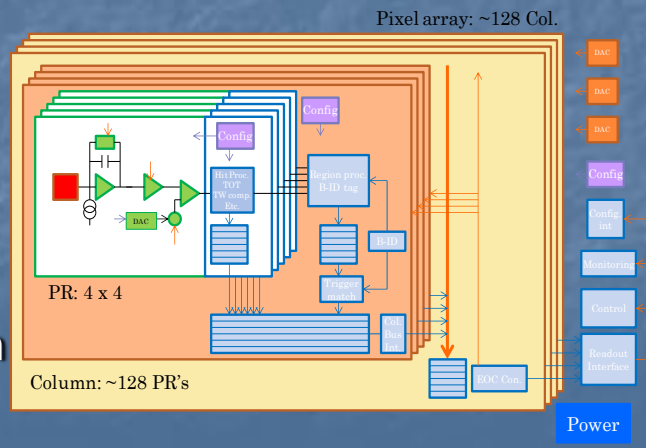




System on chip

- Large design effort required to design complicated system on chip implementations
  - Large and well integrated design team
    - Intel makes the office floor plan equal to the chip floor plan
  - Significant design time
  - Significant funding
  - Any small mistake makes the design fail
  - Efficient use of modern high level (digital) and low level (analog full custom) design tools
    - But these tools are complicated
- Example: FEI4 collaborative effort
  - Large mixed signal pixel chip (19 x 20 mm)
  - Developed in collaboration across multiple institutes (~5) spread across the world
  - Used dedicated tools to monitor/control status and changes of each block
  - Handling radiation effects and SEU.
  - Successfully made first prototype and only few minor corrections required for final chip.
- Things will get more complicated for future complex chips in 65nm: We put a whole "experiment" on a single chip

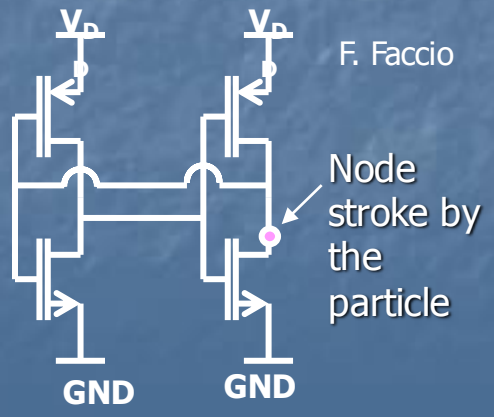


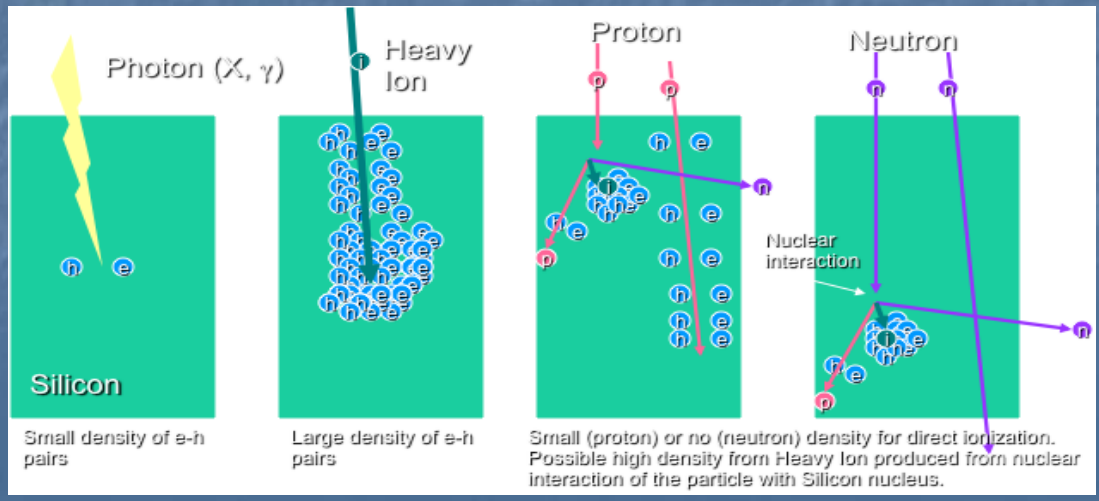


Pixel chip today = Whole detector 20 years ago

SEU

- Radiation induced SEU's is a major worry in our front-end chips
  - New technologies get more sensitive (and we get multi bit errors)
- Different types of data must be protected differently:
  - Hit data (loss of single hit, or noise hit)
  - Data flow control (system synchronization)
  - Configuration (chip malfunction until reconfigured)
  - PLL, etc.
- Appropriate design methodologies required (TMR, Hamming)
- Design, test, fault injection, design verification, production testing, etc.
- SEU's provoked by background radiation now becomes "visible" in high complexity high availability commercial applications
  - Cosmic's, Radioactive isotopes (e.g. from materials used in electronics packaging)
  - Automotive, Telecom and network infrastructure, Computer servers (e.g. centralized banking/ reservation systems)
  - They also start to apply special techniques to resolve this and some tools start to appear.





COTS

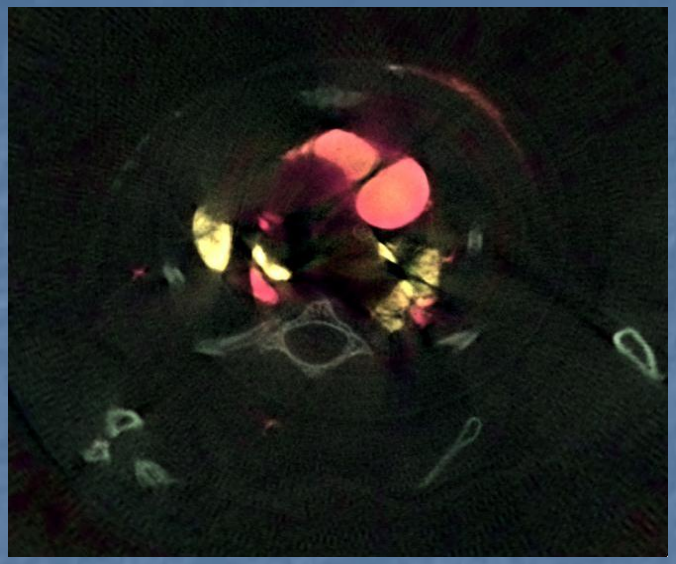
- Use COTS (Commercial Of The shelves) where ever possible (when no radiation !)
- In radiation environments
  - Radiation qualification (TID, SEL, SEU) of a component is a significant workload
    - Predictions from similar circuits can be misleading
  - Difficult to assure that circuits purchased later will have same radiation tolerance (change of process, different fab. , second sourcing, etc.)
  - Mill/Space qualified components will often be hard to get or too expensive (hermetic packaging and qualification)
  - FPGA's: Many HEP applications would like to use FPGA's in moderate radiation environments
    - Many modern FPGA can work in modest radiation (TID: 10k – 100krad)
    - Single event latchup has been seen to be OK in several modern FPGA families
    - Single events upsets is the major worry for reliable functioning
      - Antifuse: Normal SEU protection schemes (TMR, Hamming coding, etc.) can be used (can not be reprogrammed)
      - Flash: Normal SEU schemes can be used (do not reprogram when radiation is present)
      - SRAM: SEU is a major issue but tools improving on this is appearing. Partial reprogramming
    - Special space qualified FPGA's exist but are very expensive and have strict export restrictions

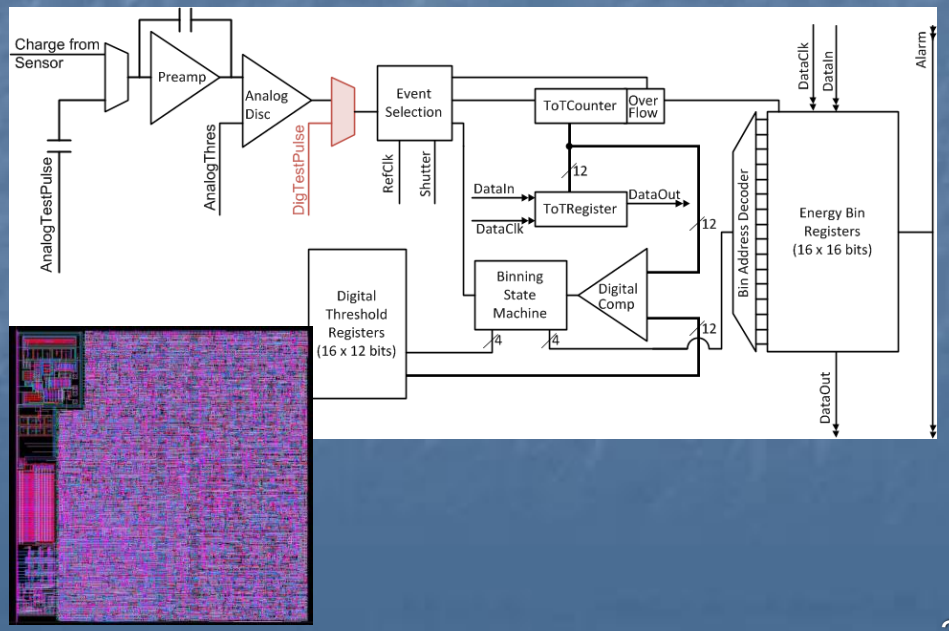
Synergy

- HEP electronics/detectors can/could have good synergy with several domains
  - Medical: Scanners, Xray
  - Material science: Synchrotron Xray detectors
  - Home security: Scanners, detectors
  - Space: rad tolerant electronics
  - [Military]
- In practice the synergy on electronics is to a large extent limited to exchange of information and experience.

Pixel detector spin off

- High resolution X-ray imaging with spectrum information
- Portable dosimeter
- In Schools !





Summary

- Ever increasing integration of detector and its electronics
  - **Pixels**, strips, calorimeter, muon, ,
- Use of modern IC, interconnect, opto and power conversion technologies vital to built significantly improved HEP experiments.
- Modern technologies are expensive to get access to and design with but offers unique opportunities and allows cheap large scale production.
- Our community must profit from available technologies the best possible:
  - Use common/shared technologies when possible
  - Exchange of experience across groups: TWEPP, FEE, NSS, MUX
  - We can "never" afford using the latest IC technologies
    - Only when using commercial IC's but they do "not like" our radiation environment
- Assure sufficient electronics engineering expertise in HEP is vital.
- Building complex electronics systems across so many groups requires efficient use of modern simulation and verification tools at all levels (system, sub-system, links, module, ASIC, analog front-end) and efficient communication and coordination.
- Certain basic technologies/functions are needed by all HEP experiments/sub-detectors and is better made as common efforts
  - IC technology qualification, libraries, IP's, Tools
  - Radiation hard optical links
  - Radiation hard and magnetic field tolerant Power conversion
  - Other ?

If you want to know more on electronics for HEP then come to TWEPP 2012