The EndoTOFPET-US front end & data acquisition system

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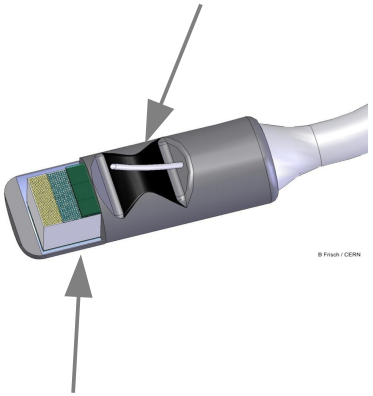
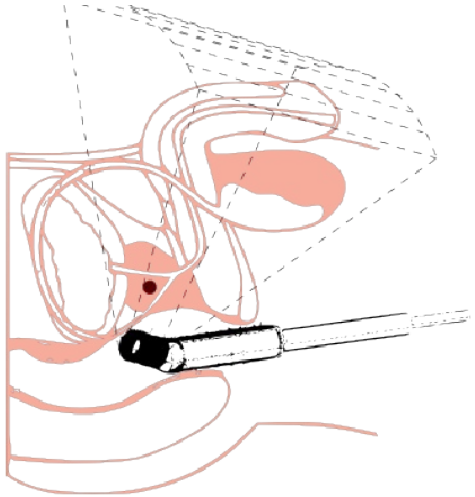
Jornadas LIP, April 22nd 2012

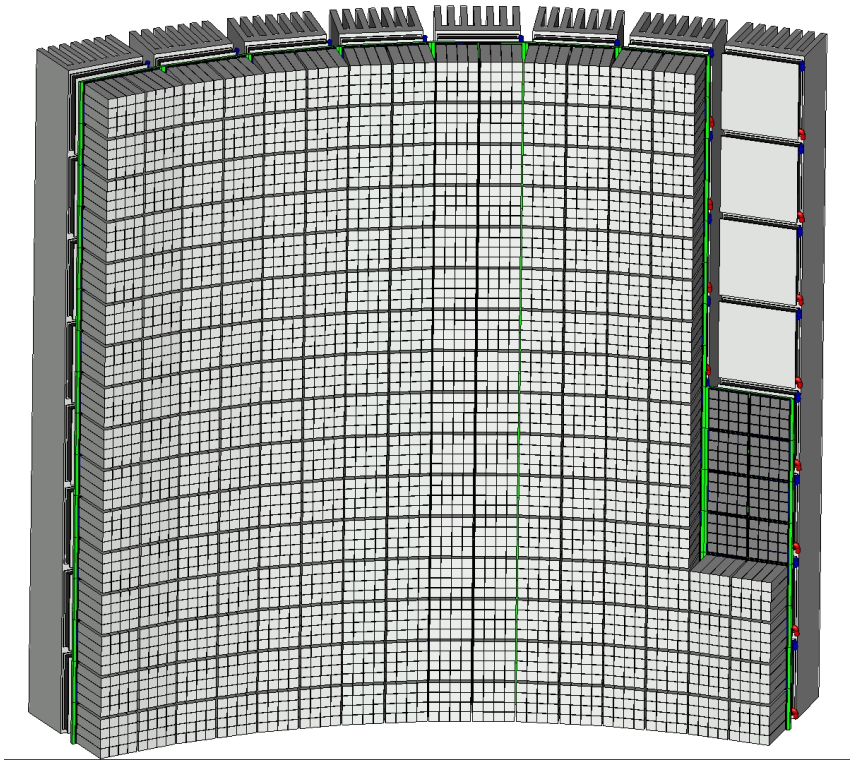
What is EndoTOFPET-US?

Ultra-Sound transducer



PET head
0.8x0.8x10 mm³
crystal filbers coupled
to digital SiPMs





External 20.5x20.5 cm² PET plate
4096 3x3x15 mm³ crystals coupled to SiPM

Very high background event rate (40 MHz)
200 ps time resolution required for background rejection

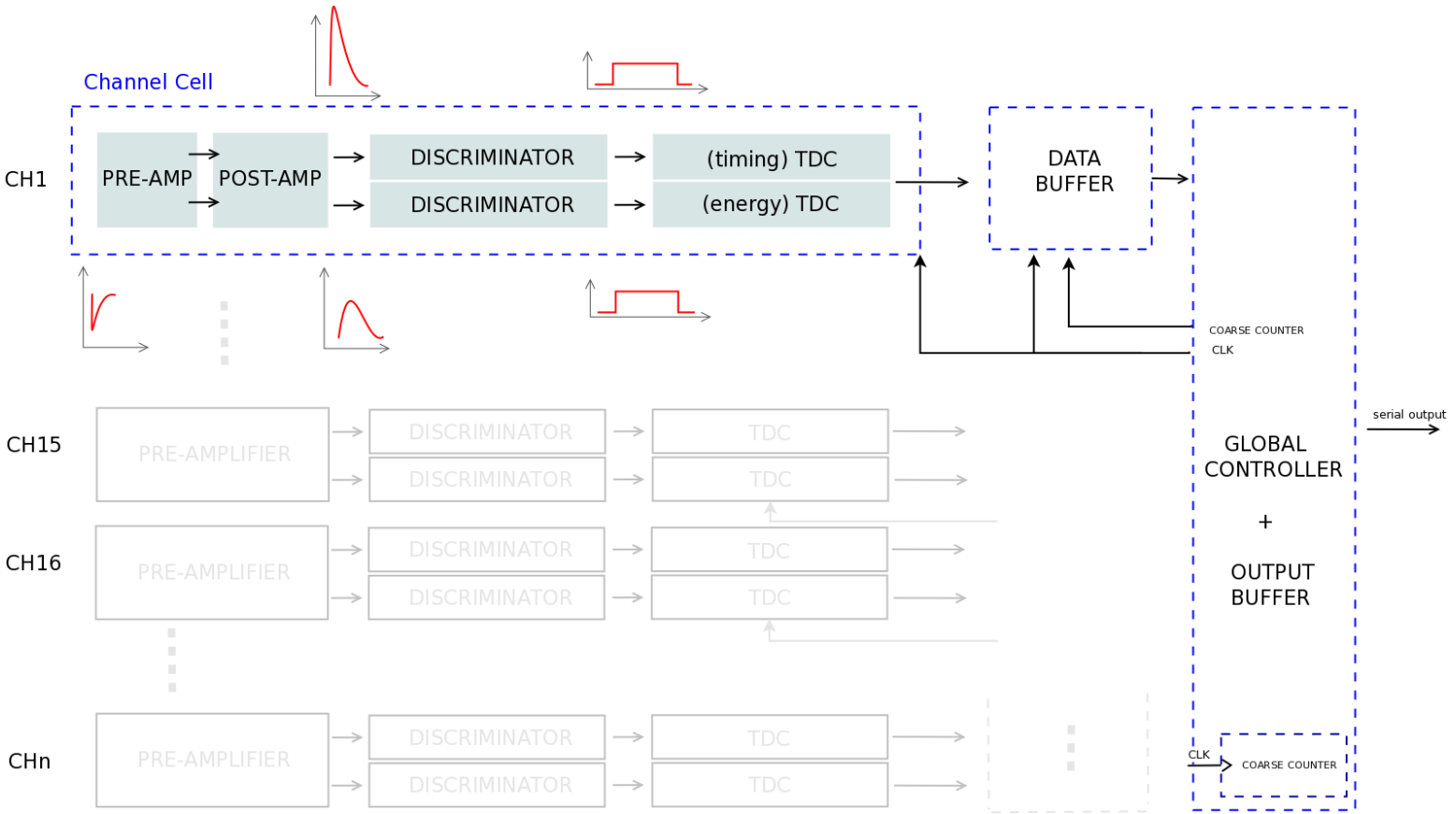
LIP's contribution

- External plate front end
  - A suitable ASIC – in collaboration with INFN
  - Front End Boards
- Data Acquisition System

ASIC requirements

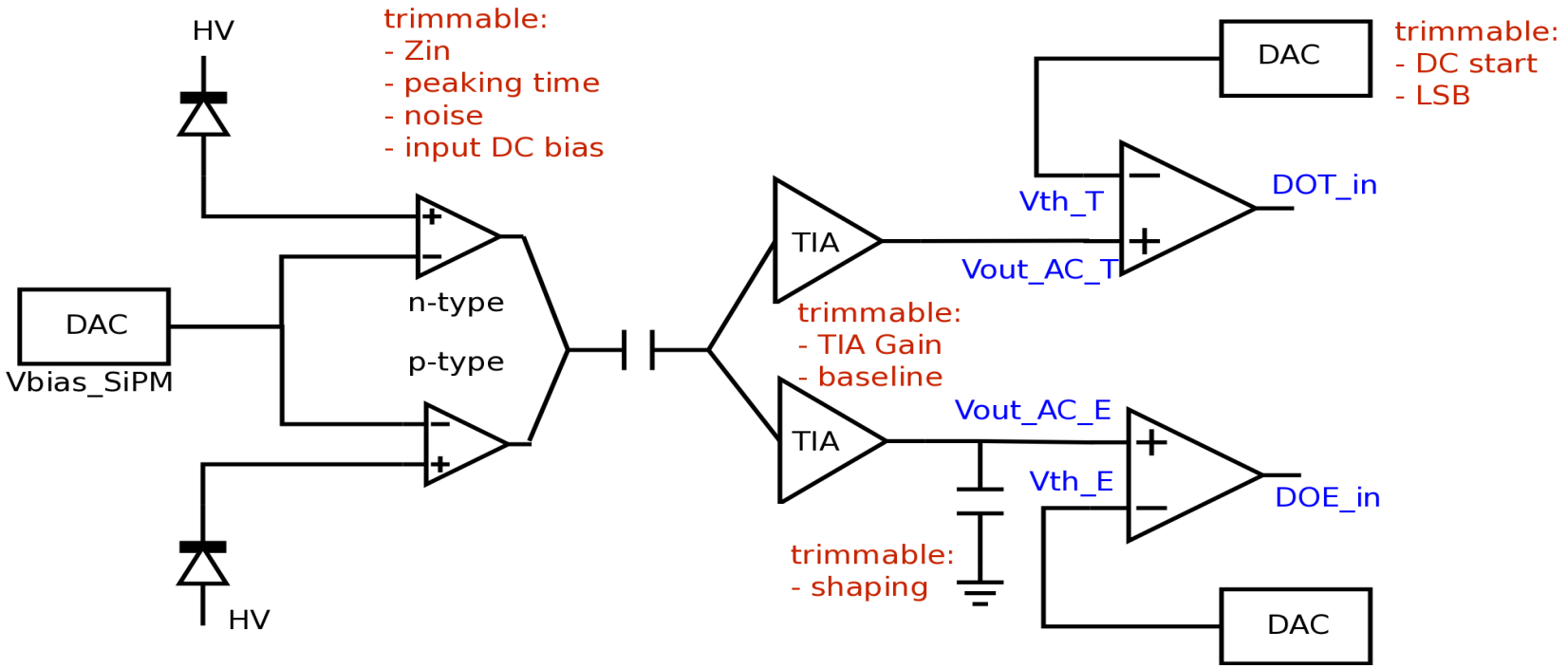
- SiPM readout
- <200 ps time resolution
- Suitable for dense systems (10 channels/cm^2)
  - Monolithic
  - Fully digital Time & Energy readout
  - < 10 mW/channel

Two transimpedance stages generate two replicas for time and energy measurement; respectively, a fast trigger and a shaped signal.
The low noise front-end allows setting the threshold of the discriminator at 0.5 photoelectrons for the time stamp DOT_in.
Energy is calculated after calibration of the time-over-threshold of DOE_in.
Both measures are based on a low-power analogue time-to-digital converter with 50ps time binning.
Expected power consumption per channel is 7mW.

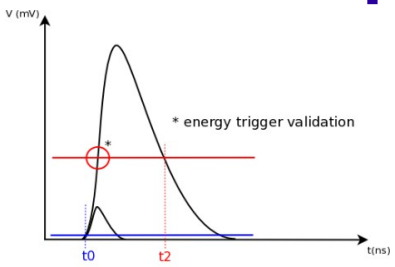


Low input impedance stage (Input resistance trimming to match line impedance) allows fine adjustment (6-bit over 500mV range) of the HV bias of the SiPM*. Two independent input stages permit the use of devices with different polarities: h-collection (bottom left) or e-collection (top left).

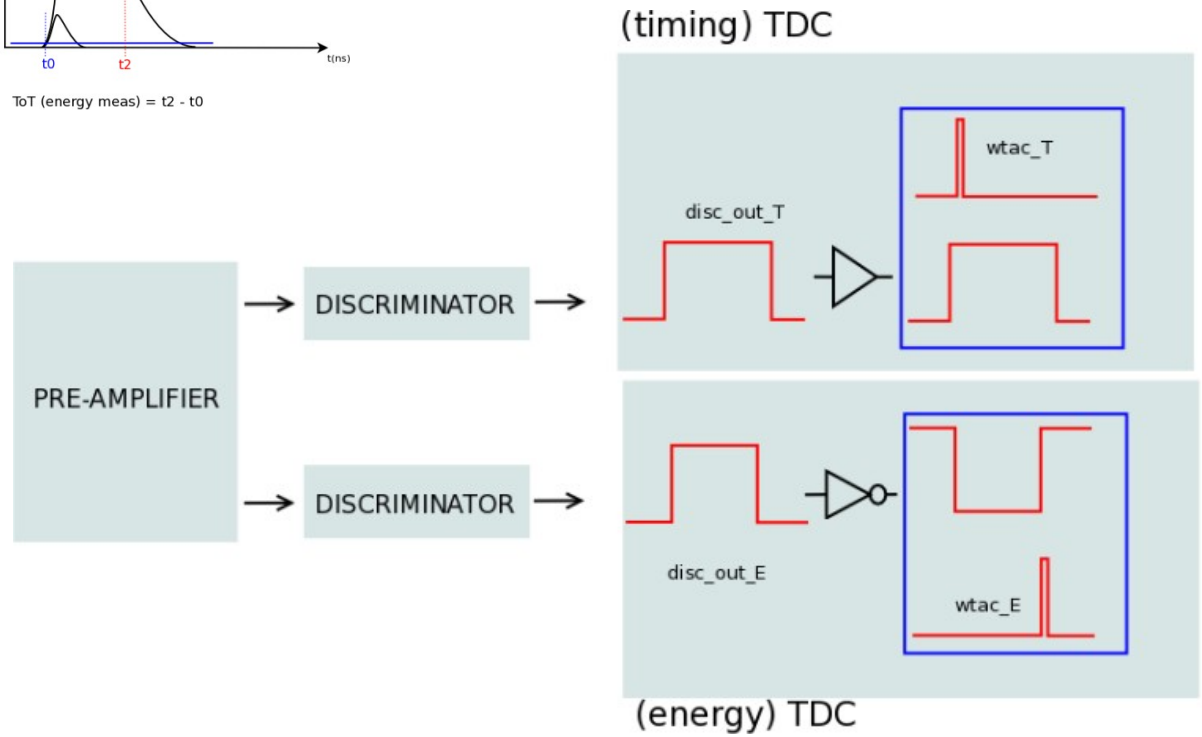
* Each 16 SiPM array has a common, but adjustable bias (14-bit over 0-100V).



TDC operating principle



ToT (energy meas) = t2 - t0



data per event (TIMING TDC)
coarse time
- 10 bit + frameID
fine time
- 10 bit soc (coarse time stamp)
- 10 bit eoc (coarse time stamp)

data per event (ENERGY TDC)
coarse time
- 10 bit
fine time
~~- 10 bit soc (coarse time stamp)~~ *
- 10 bit eoc (coarse time stamp)

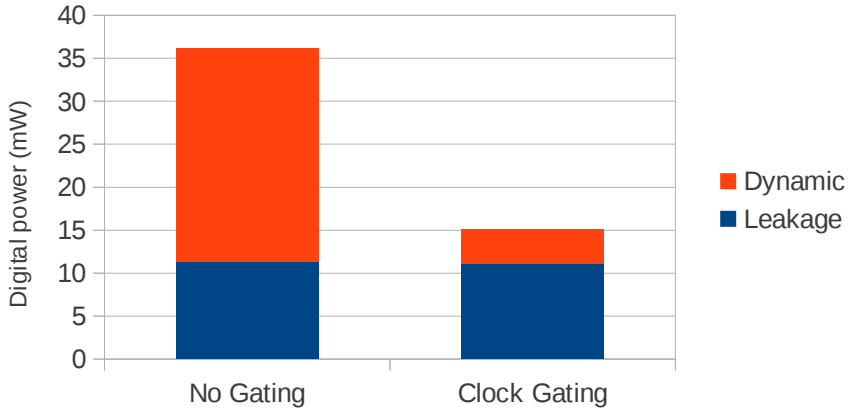
* redundant, since the conversion starts simultaneously in both branches

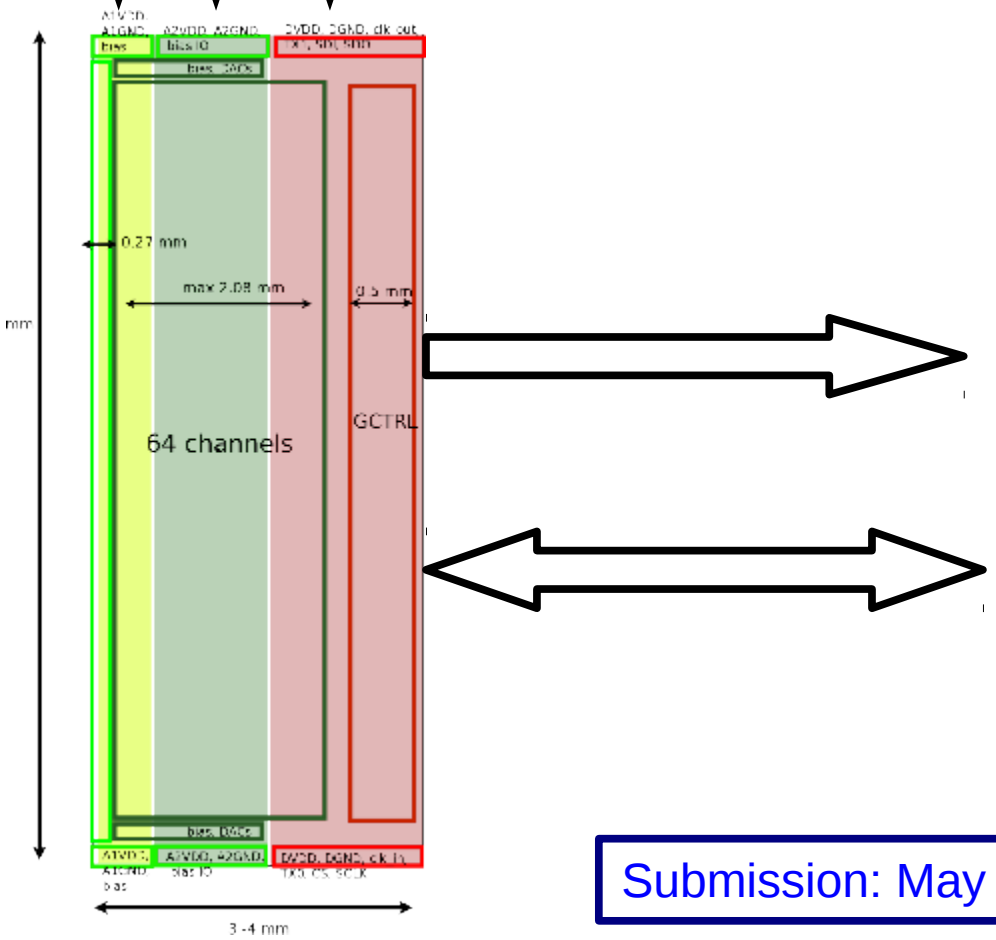
wtac_* start at the edge of the discriminator edge but stop at a (known) clock edge
wtac_* control the charging of a capacitor with a current source
⇒ voltage in the capacitor reflects phase between discriminator edge and clock edge

Afterwards, voltage in capacitor is discharged 128x more slowly
⇒ phase between event and clock is measured in 1/128th clock (48 ps for a 160 MHz clock)

Front end
TDC analog
Digital

Power domains



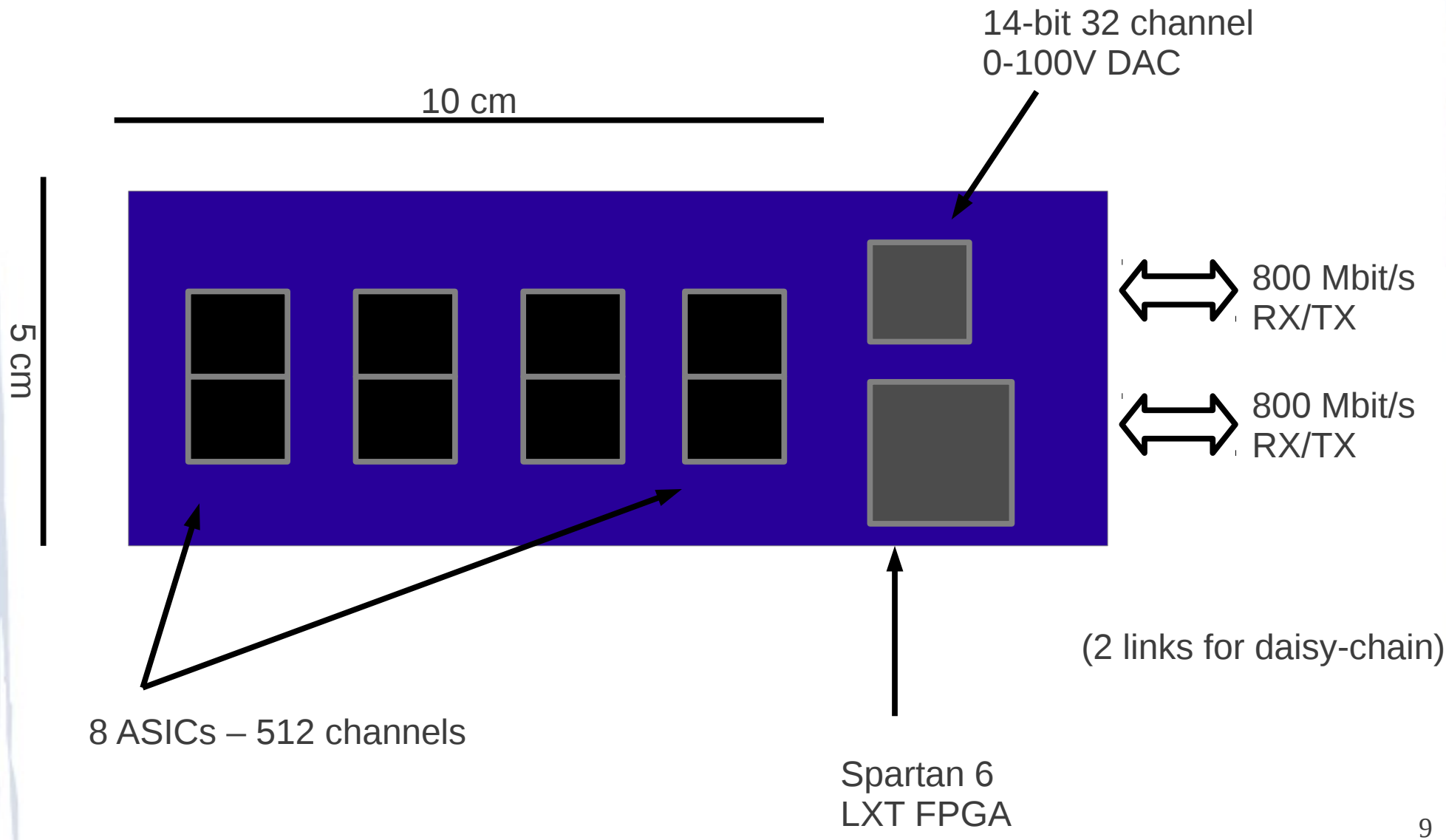


Serial data out
- Configurable width (1 or 2 bit), SDR/DDR
- 160-640 Mbit/s (2.5-10 Mevent/s)
- Events are grouped by 1024 clock frames

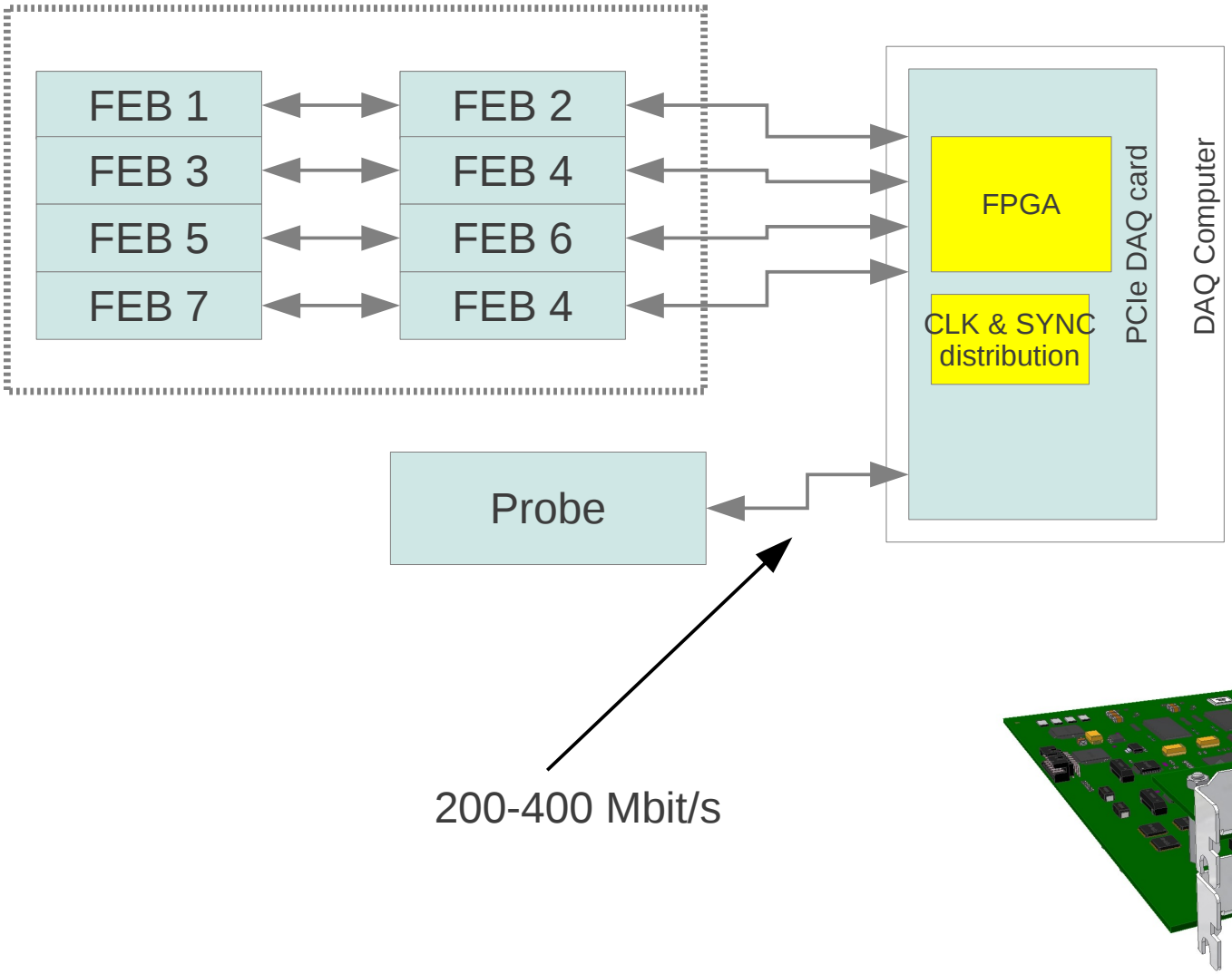
Configuration link
- 10 MHz
- 4 signals
- ~4 kbit configuration!

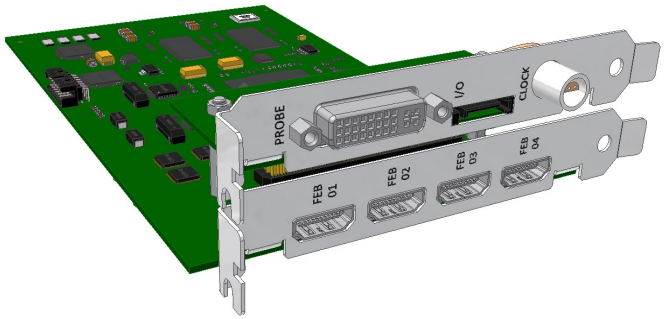
Submission: May 21st 2012

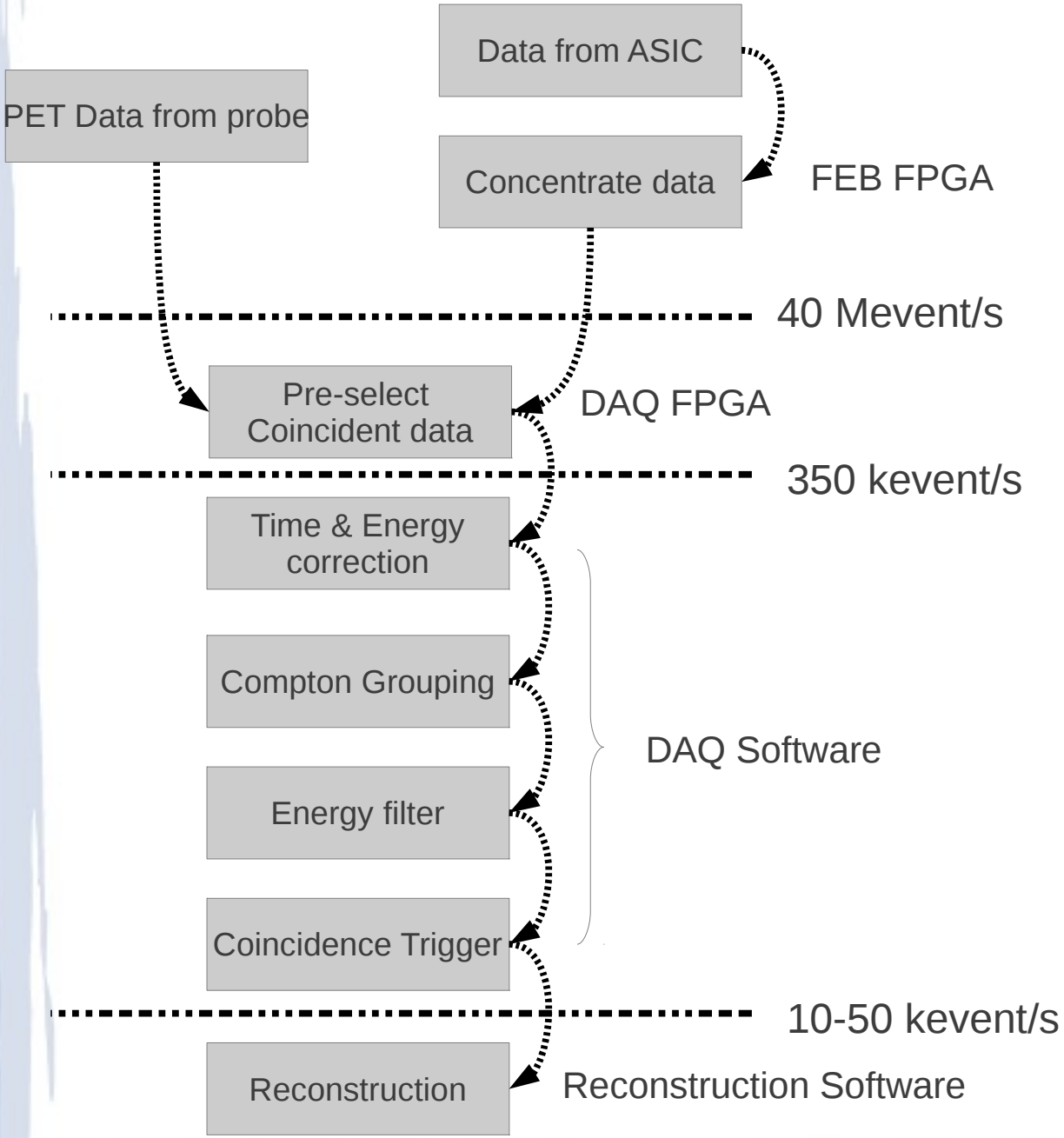
Front-end


14-bit 32 channel
0-100V DAC
10 cm
5 cm
800 Mbit/s
RX/TX
800 Mbit/s
RX/TX
(2 links for daisy-chain)
8 ASICs – 512 channels
Spartan 6
LXT FPGA

Data Acquisition System







Use hardware only to reduce data rate to a manageable value.

Put sophisticated processing in software!

Re-use ClearPEM DAQ software, which already implements a suitable processing chain.

Lots of calibration algorithms to be developed...

Summary

- ASIC design is almost complete
  - Submission May 21st 2012
  - Validation in 3rd quarter 2012
- Front-end Board design pending
  - ASIC pinout
  - Plate geometry decisions
- DAQ card design is done
  - Under assembly
- Firmware & Software will start in July

Thank you for your attention