Progress on the MICE LLRF System

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Collaboration Meeting 33

25th 29th June 2012

University of Glasgow

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Introduction

- In the last MICE RF meeting, it was decided that we would use a LLRF control system. (it wasn't entirely clear that this was needed.)
- The Daresbury RF group has begun a study into how we might achieve a suitable system for MICE.

LLRF Basics

- The primary function of the LLRF system is to stabilise the amplitude and phase of the RF field within the cavities within a given tolerance. This is typically achieved using fast feed back
- Secondary tasks
  - Feed Forward (for controlled cavity filling)
  - Monitoring transmission line power
  - Cavity protection
  - Cavity Tuning
  - Other stuff!

Hardware options

- Analogue Vs **Digital**
- Commercial systems
- Open systems
  - LLRF4 board / Larrys new system in development
  - CERN OHWR open source system.

Analogue Vs Digital

Analogue

- **Very** low latency
- Low complexity
- High reliability
- Low Upgradability
- Low(er) cost
- Few diagnostics

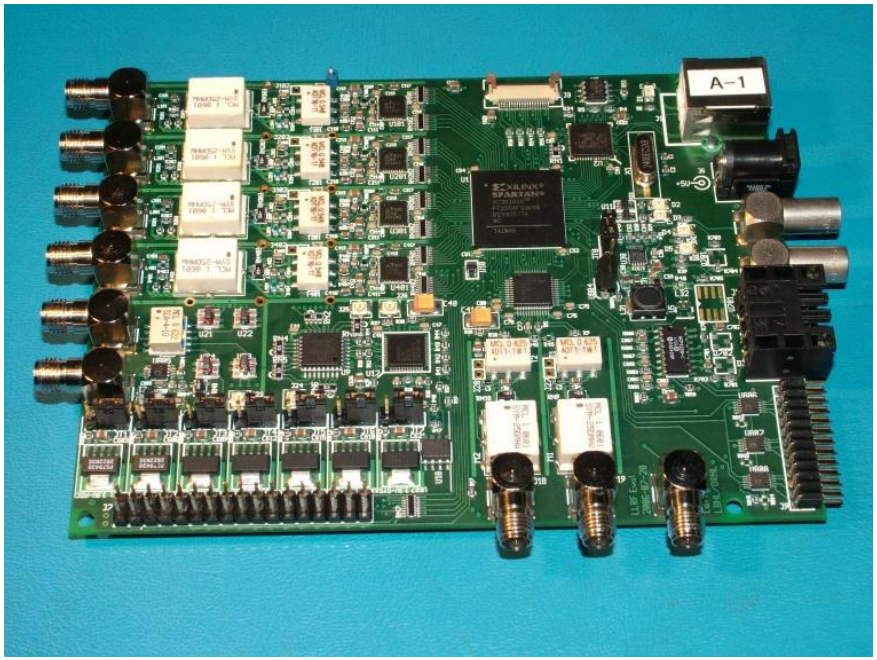
Digital

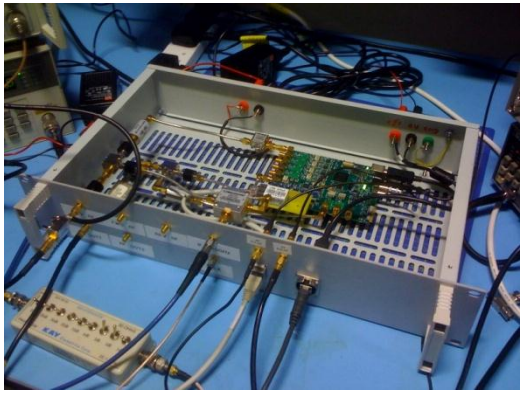
- More easily reconfigured
- Loop parameters tuneable in the field.
- Possibility of Adaptive feed-forward
- Diagnostics built in

Digital Wins!

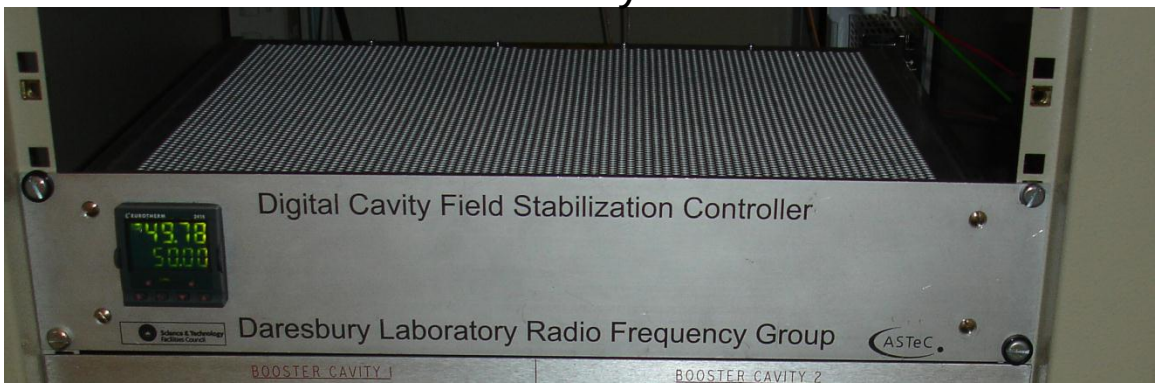
LLRF4

- Designed by Larry Doolittle LBNL
- 4 IF/RF inputs
- 2 IF outputs
- Xilinx spartan 3 FPGA
- Other stuff
  - Slow DAC outputs
  - Programmable clock dividers
  - USB communications
- Used at DL





1.3Ghz feedback system on ALICE



Firmware

- Most development cost lives here.
- But- everything we need to code for MICE is mature technology, nothing new or controversial.
- We can use lots of recycled code. Expect there is plenty that LBNL can add to the project.

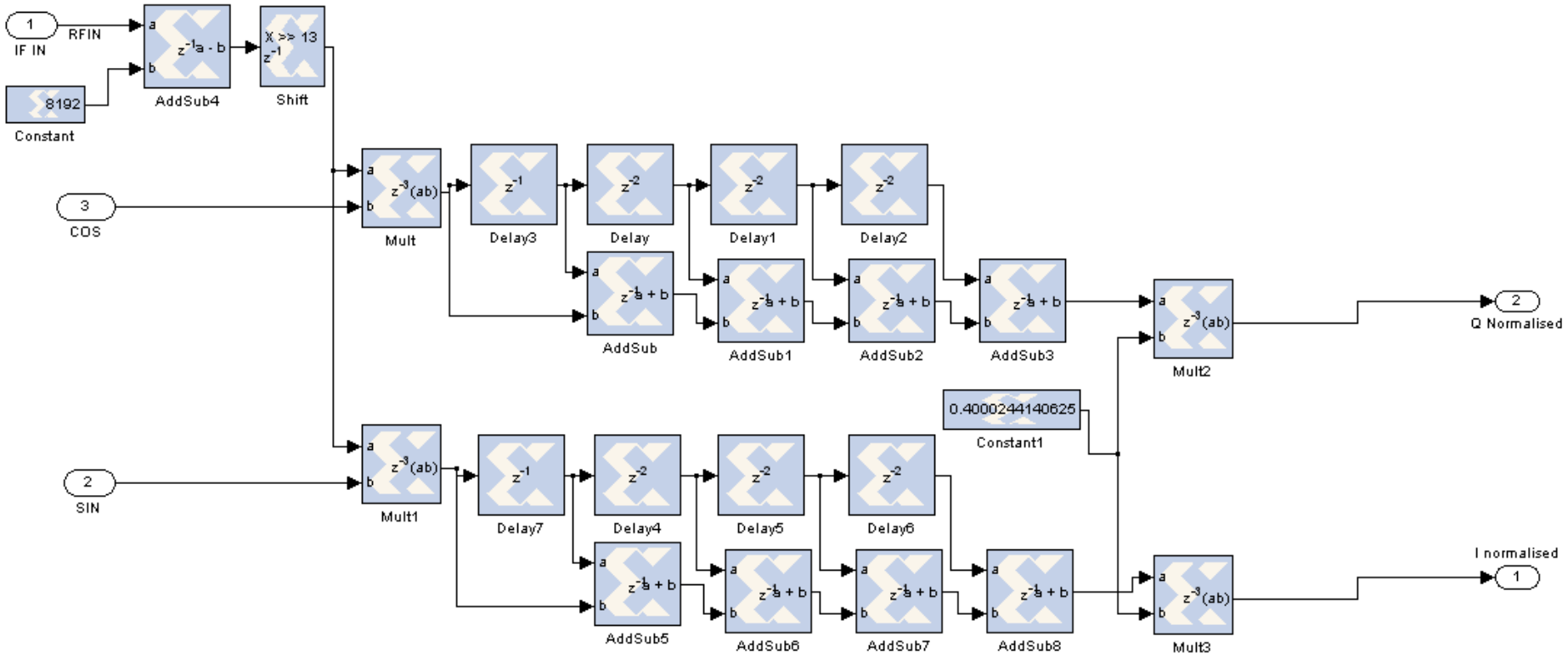
Non- IQ Demodulation

- Sampling clock is set at a rate N/M RF frequency.
- I and Q are then obtained from :

$$I = \frac{2}{N}\sum_{i=0}^{N-1} y_i \sin(i.\Delta\phi)$$

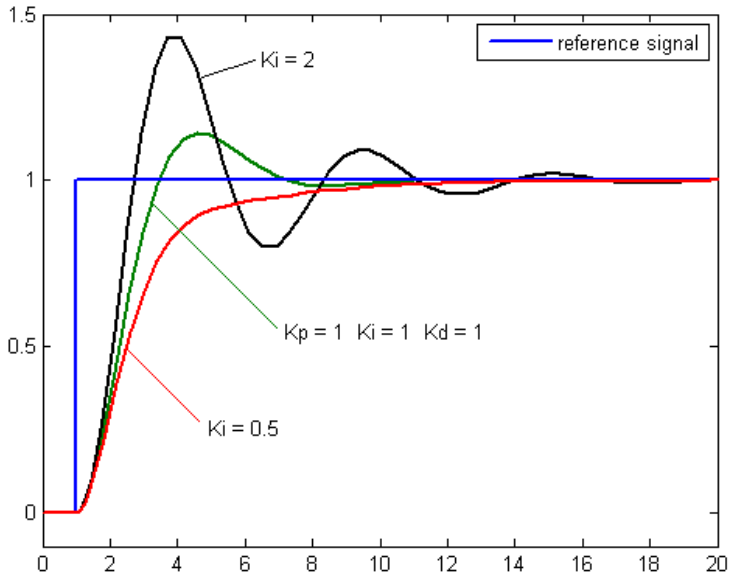
$$Q = \frac{2}{N}\sum_{i=0}^{N-1} y_i \cos(i.\Delta\phi)$$

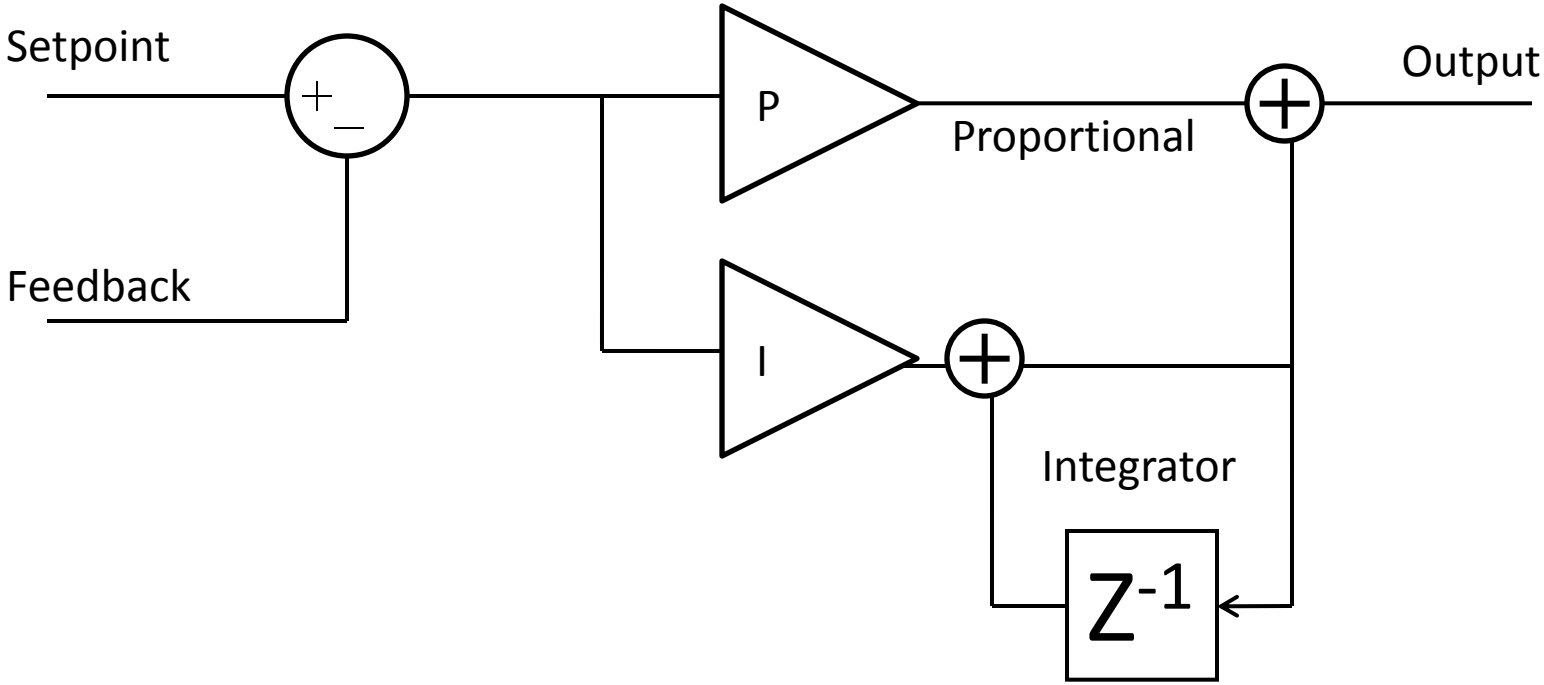
- Where
  - N is the number of samples in the constellation
  - Φ is the phase advance per cycle
  - Yi is the ADC input



Fast Feedback control

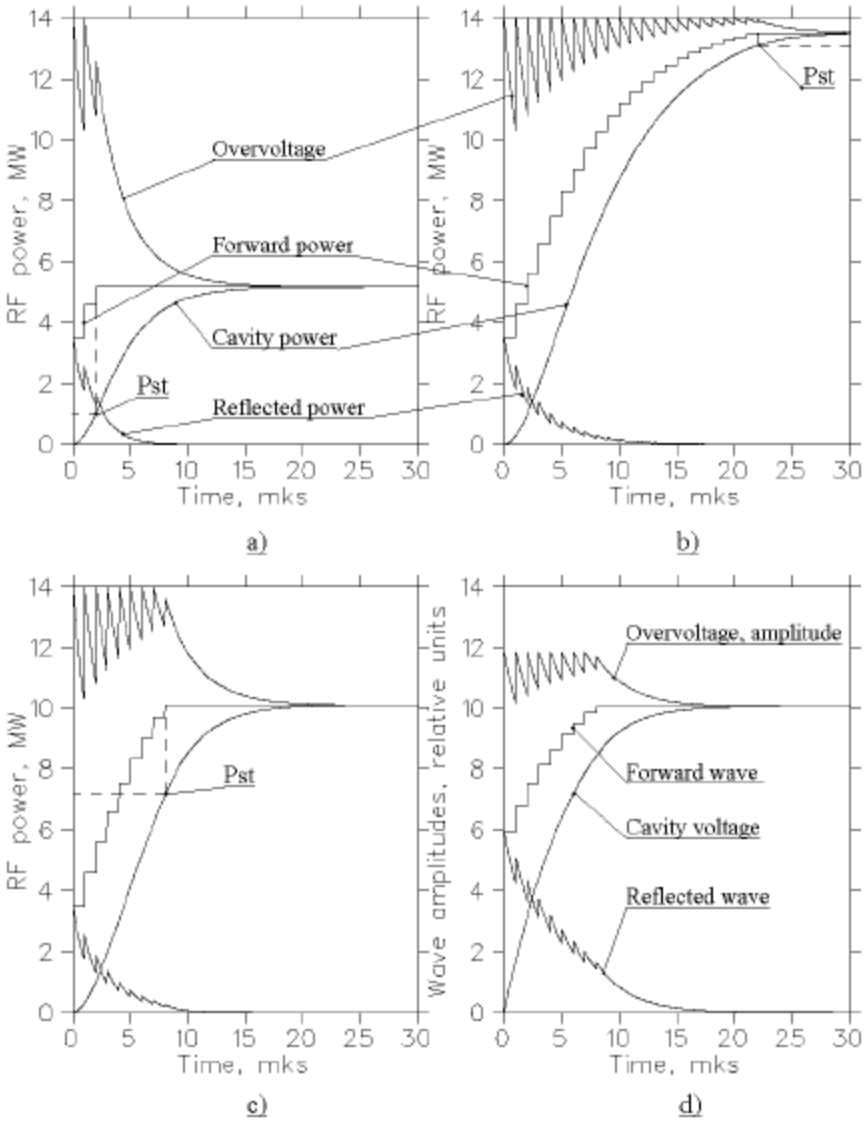
- The I & Q feedback values are each fed into a separate controller.
- Controller is a PID loop (without the D – we are already damped enough by the cavity!)
- The PI controller is a simple, robust, proven technology used everywhere.





Cavity Filling (feed forward)

- Because MICE does not use circulators / Isolators to protect the amplifiers, large reflections can cause damage.
- Large reflections may occur during initial cavity filling.
- This can be eased by ramping the input power using constant reflection condition.
- On the FPGA, we need to code a programmable ramp with variable duration, so that we can use the shortest ramp length possible, whilst still avoiding overvoltage in the coax.



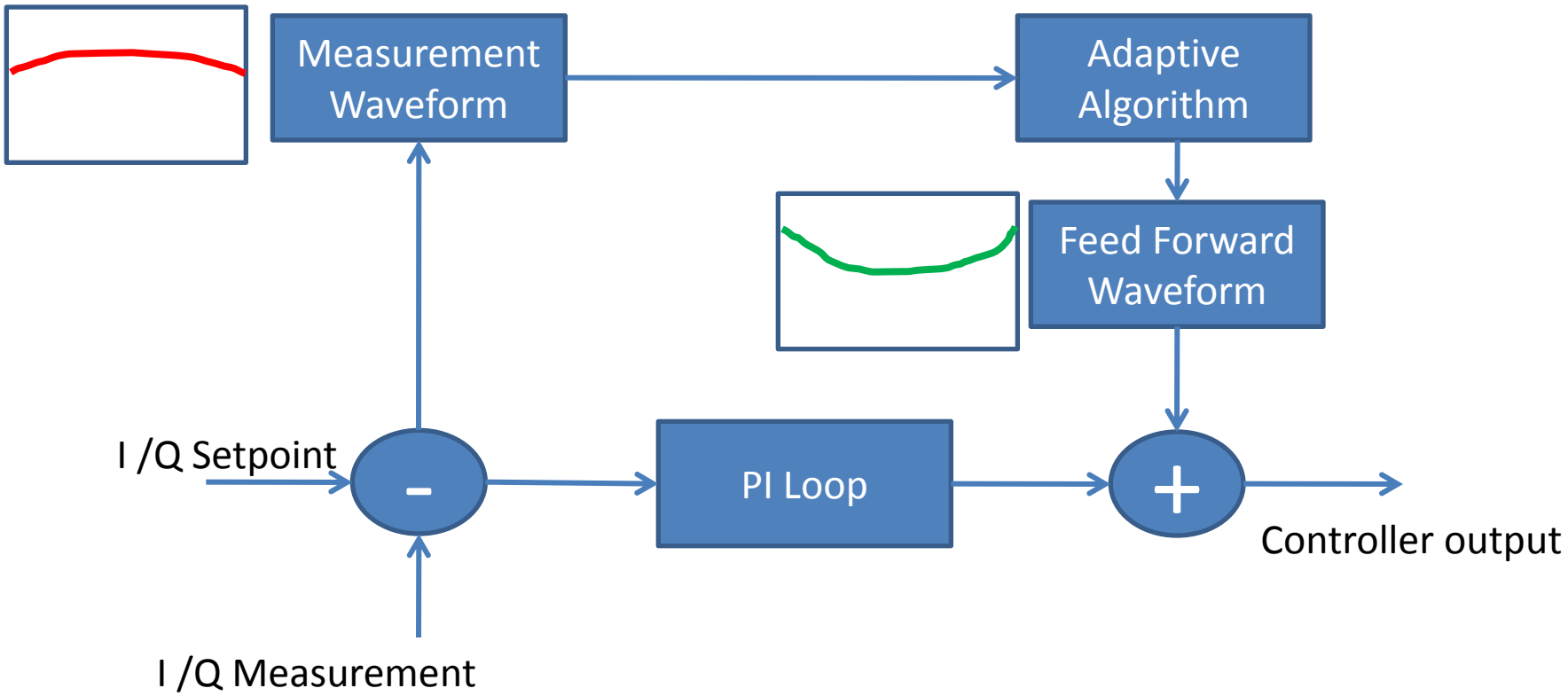
Adaptive Feed Forward Control

•Pulse to pulse compensation for predictable, repeated disturbances.

- Power supply / triode droop
- Mains noise
- Lorenz force Detuning (probably not an issue for us)
- Other disturbances which are the same for each RF pulse

Sequence of events

• A measurement of the pulse flat top is taken and measured against the setpoint.
• A corrective waveform is calculated for this error waveform.
• On the next pulse, this corrctive waveform is applied to the modulator output, in addition to the feedback.
• The sequence is repeated for each pulse
• An adaptive algorithm performs calculations to reduce the flat top error over the full pulse.

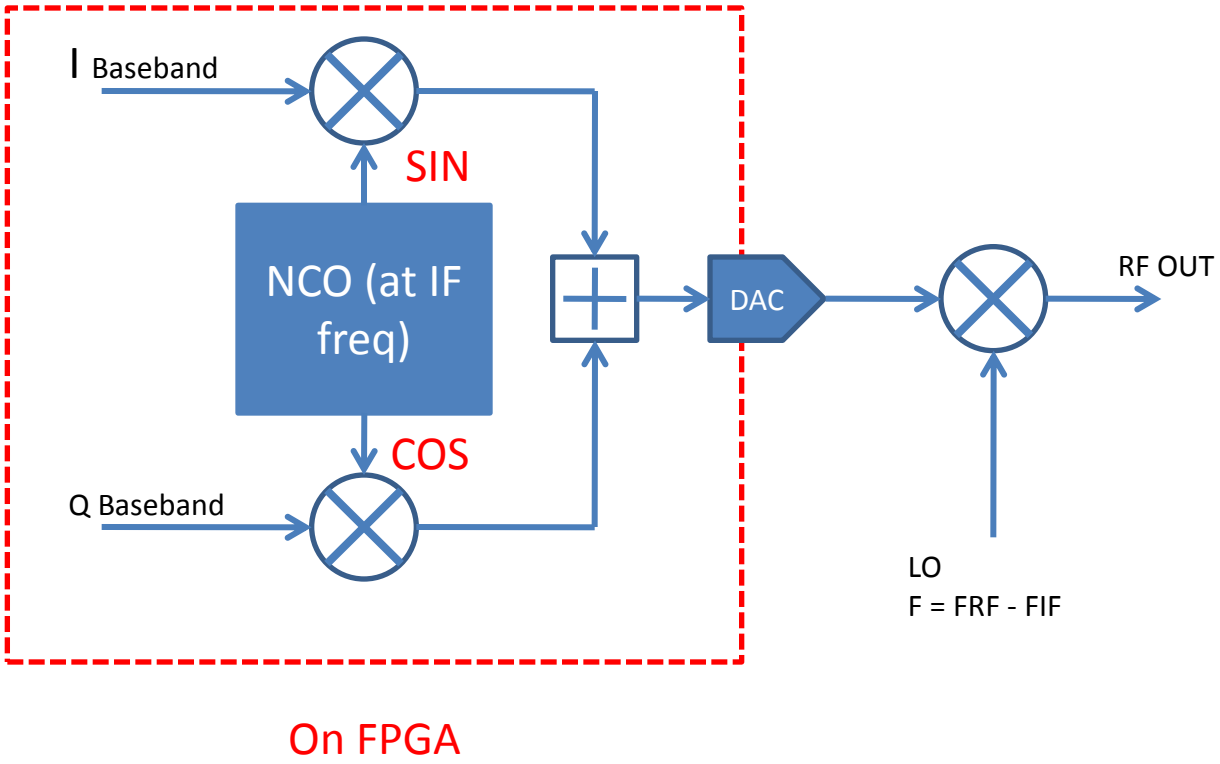


Modulation

- Conversion from baseband I & Q values to IF output.
- IF output is calculated as :

$$IF_{OUT} = I \cdot sin\varphi_i + Q \cdot cos\varphi_i$$

- Where the sin and cosine values can be obtained from
  - NCO
  - DDS
  - Look up table
- The output IF waveform contains a wide spectrum of components due to it discrete time nature. It requires band pass filtering to remove the digitisation noise.



Proposed system

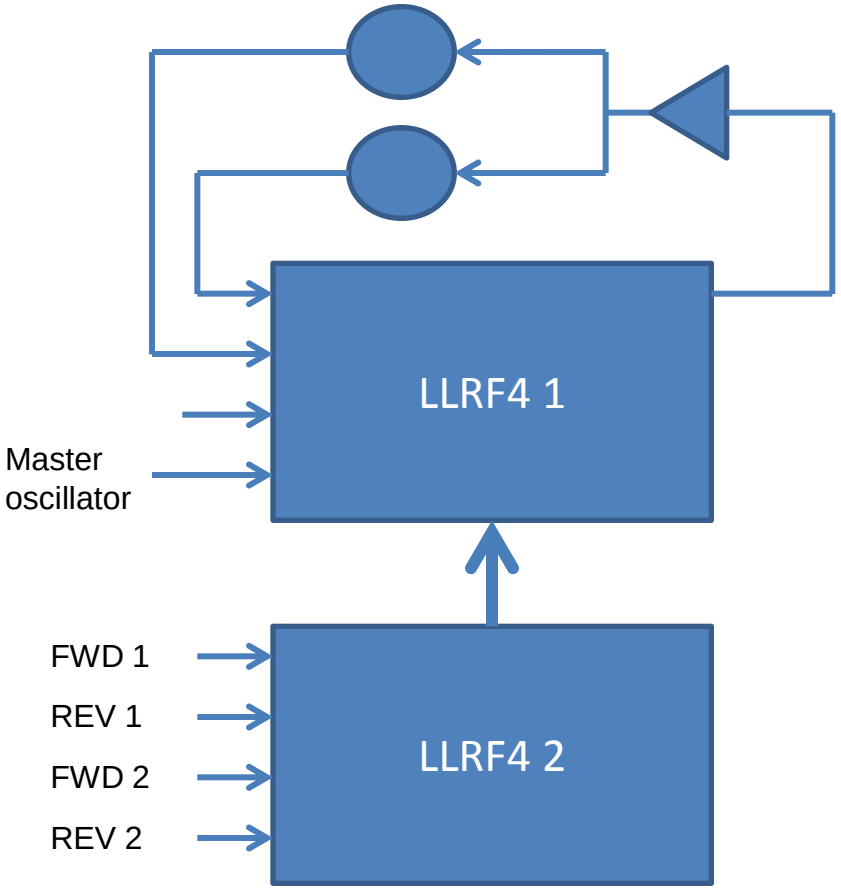
NOTE!

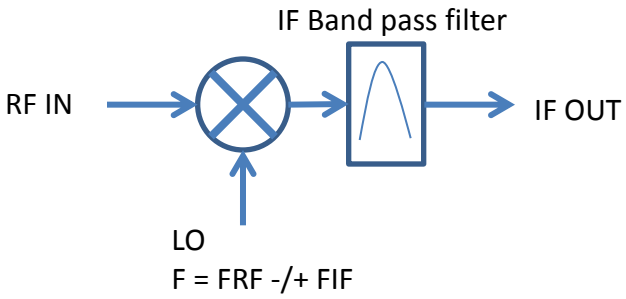
Everything is up for discussion

Comments / advice welcome!

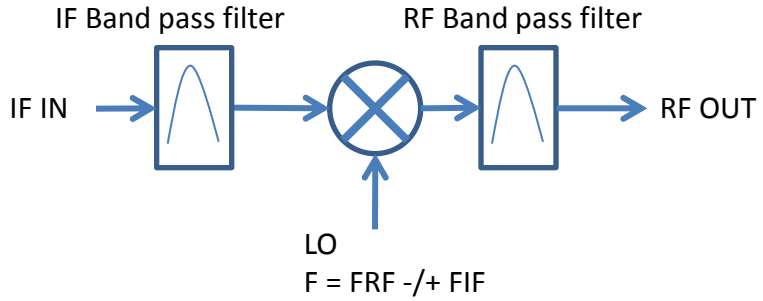
Proposed Hardware

- For each cavity pair, we use 2 x LLRF4
  - One board samples the 2 cavity probes, plus the reference oscillator.
  - Second board samples the FWD and REV powers for each cavity.
  - Sample data is continuously streamed from the second FPGA to the first.
  - All clever control is performed by the first LLRF4 card.
- Inputs are mixed down to an IF frequency
  - Somewhere between 30 and 60 MHz
- Outputs are mixed up from the same IF frequency.
- Analogue Up/Down conversion components are temperature stabilised.



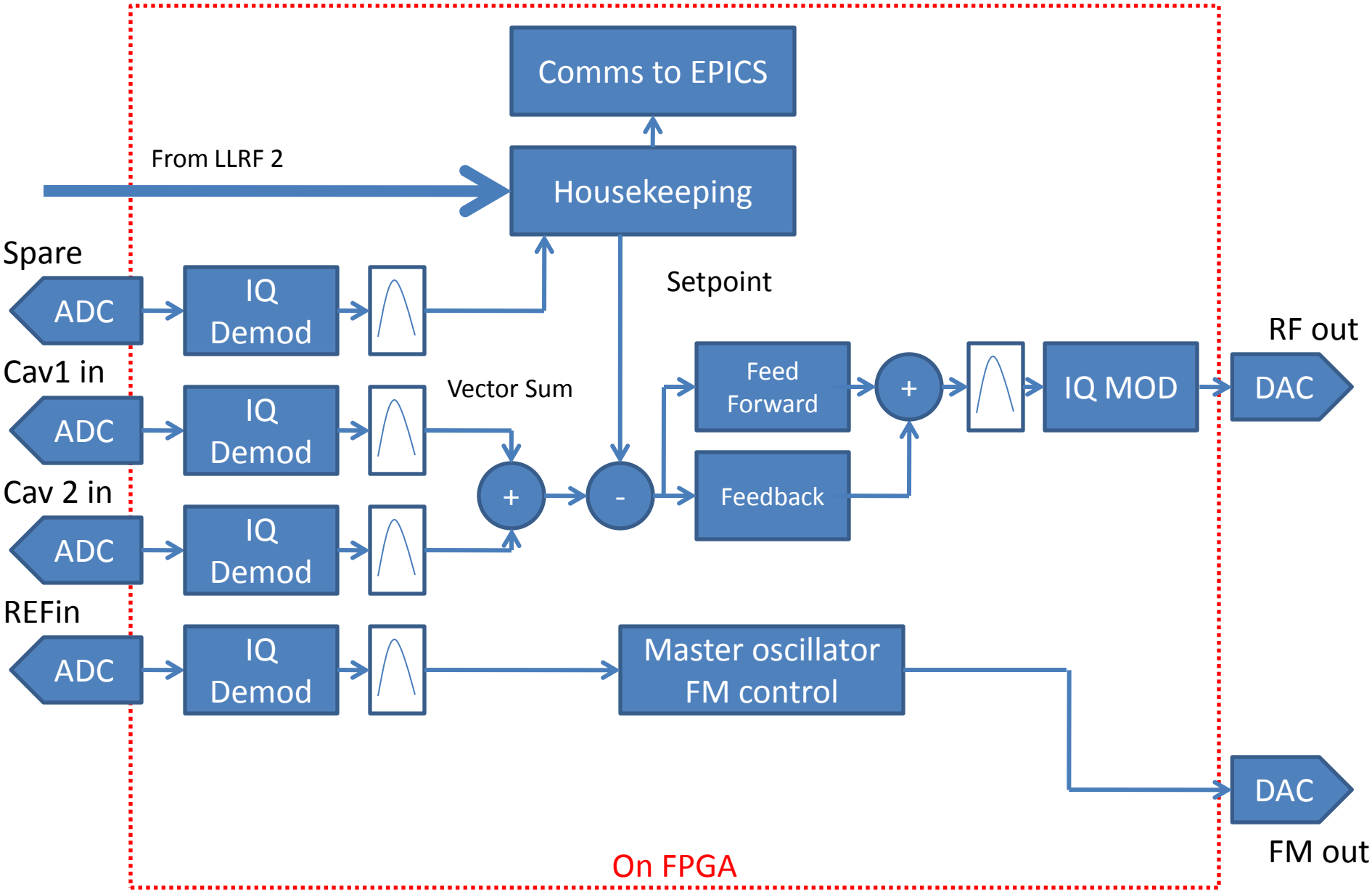


INPUT DOWNCONVERSION

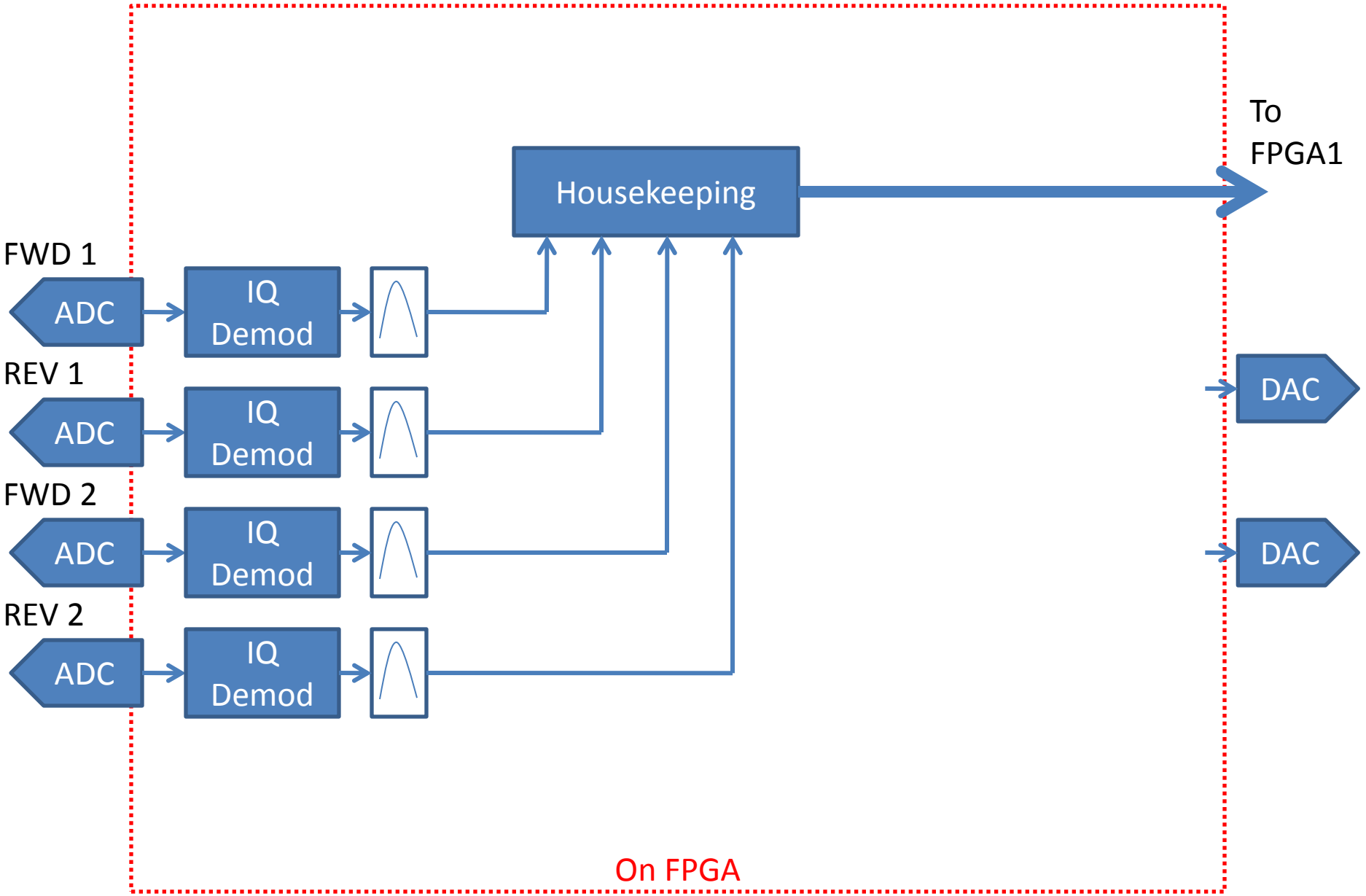


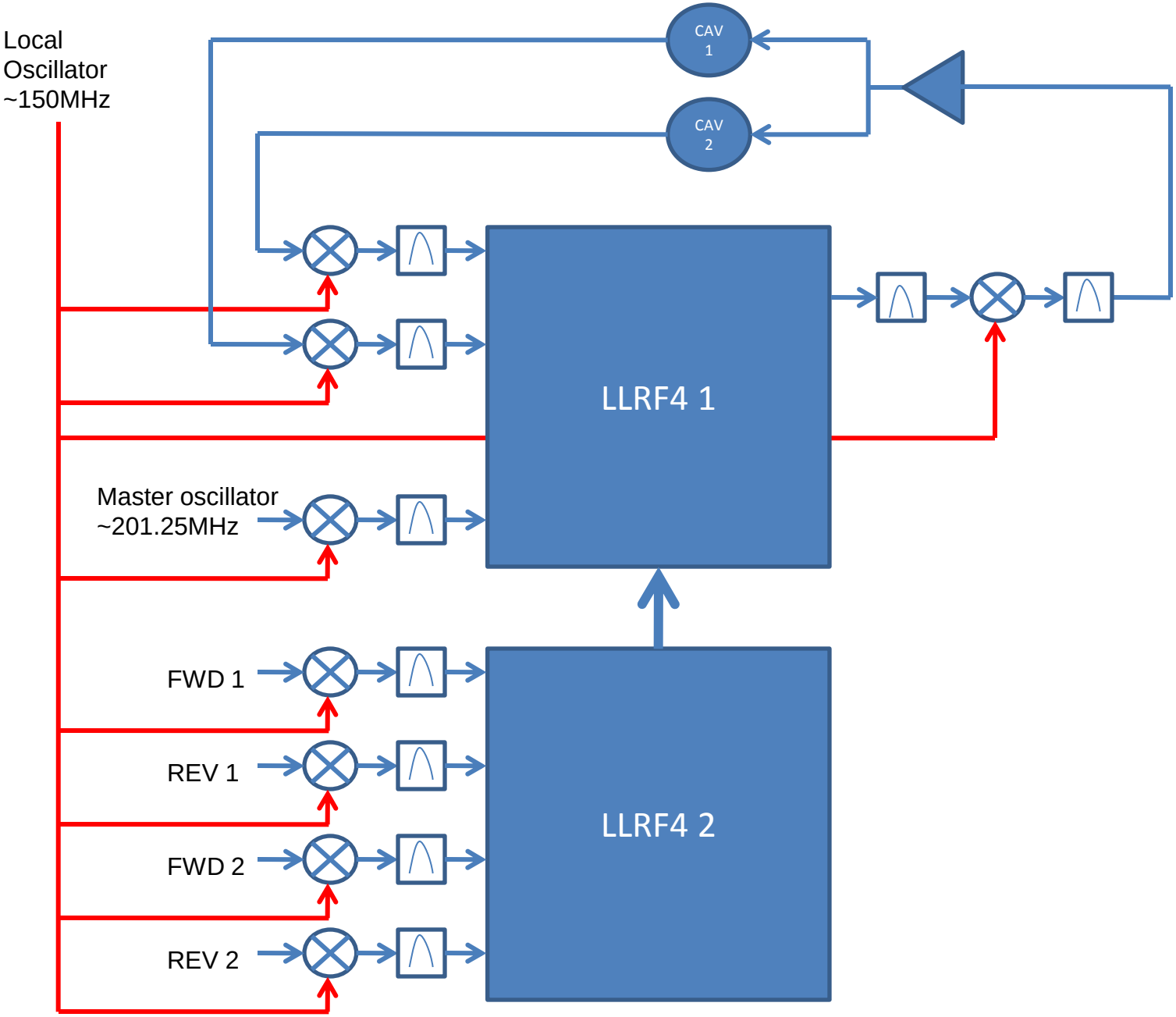
INPUT DOWNCONVERSION

Firmware structure (FPGA1)



Firmware structure (FPGA2)




Local
Oscillator
~150MHz
CAV
1
CAV
2
LLRF4 1
Master oscillator
~201.25MHz
FWD 1
REV 1
FWD 2
REV 2
LLRF4 2

Milestones

- Specification agreed ?
- Hardware platform decision ?
- Agreement on firmware architecture ?

All to be agreed

Summary

- Basic design philosophy being worked on
- Nothing that technically challenging in the MICE RF system, all been done before, we can use standard firmware routines for much of the code
- Will require help of LBNL for ramp fill software and the choice of which hardware to use
- Can be built at DL electronics workshop