FEI4 is a novel pixel detector readout chip designed in a CMOS 130nm feature size process. The chip is able to cope with high hit rate and withstand the harsh radiation environment in close proximity to the interaction point at LHC. FEI4 will find its first application with ATLAS IBL, an additional innermost pixel layer scheduled for installation in 2013, but is also suited for the intermediate radii pixel layers for future upgrades. I will discuss the modular concept of FEI4, array and pixel size, analog performance, readout architecture, powering options and radiation hardness. I will focus on the development of FEI4B, the production version of the chip for IBL, and show test results obtained since the chip has become available in December 2011.