3D Integration with TSV

Outline

3D integration and TSVs

Motivation in industry

Motivation for pixel detectors in HEP

Current R&D projects

Conclusions

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3D interconnection

Two or more layers (=“tiers”) of thinned semiconductor devices interconnected by vias to form a “monolithic” circuit.

- Different layers can be made in different technology (BiCMOS, deep sub-\(\mu\) CMOS, SiGe,…..).

- 3D is driven by industry:

- Long Connection
  - Low Density
  - Poor Heat Dissipation
  - RC Delays
  - High Impedance
  - Large Area
  - Challenging Interposers
  - I/O Pitch limitations

- Short Connection
  - High Density
  - Good Heat Dissipation
  - Reduced RC Delays
  - Low Impedance
  - Smallest Area
  - Simple Interposers
  - Less I/O Pitch limitations

Source: Fraunhofer-IZM

James Lu, RPI, Peaks in Packaging, 2003

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Vertex 2012, Jeju, Korea, Hans-Günther Moser
Motivation

Will this continue?

Excessive costs of smaller feature size

Smaller metal lines: Penalty in speed and power

Going 3D can increase transistors/area without reducing size

Or

Is there even ‘more than Moore’

Source: wikipedia
Not a new idea

William Shockley filed a patent in 1958 (granted 1962)
Describing TSV to connect two sides of a wafer

William B. Shockley
1910-1989
Nobel price 1956
Lecture by Richard Feynman, 1985: ‘Computing Machines in the Future’

“Another direction of improvement (of computing power) is to make physical machines three dimensional instead of all on a surface of a chip. That can be done in stages….  
- You can have several layers and then add many more as time goes on.”
Vias Last – Vias First

Two different concepts:

**Via last**: postprocess CMOS (and other) wafers with vias
- any technology can be used (in principle)
- via area has to be reserved designing the chip
- area for vias introduces dead area in CMOS chip
- complicated process flow
- only low temperature processes can be used for via processing

**Via first**: Vias etched before CMOS processing
- integrated part of the CMOS process
- vias don’t add much dead area
- high temperature processes for vias possible
  (e.g. poly-silicon)
- limited to few producers and technologies

And, there is via middle…. 
3D sensors (like for cameras) seem to be not (yet) of interest

J. Lau 3DIC2011
Interposer (2.5D)

Assemble state-of-the-art 2D chips on interposer

Interposer: passive silicon with TSV and redistribution layers

Basically an advanced packaging technology

Efficient I/O contacts (standard bump bonding)

Efficient (but not yet optimal) inter-chip connectivity

Low via density (~ 200µm pitch) and large diameter vias

=> easy and cheap
Die Stacking

Samsung
8 layer flash memory
Individual dies have
55-70µm
(still) used in Apple’s Iphone4

Intel

Shortest chip to chip interconnect

TSV

Wider bandwidth
Lower power consumption
⇒ Better performance at high speed
However: costs
(wire bonding is a mature technology, cheap and reliable)

Only few vias needed in periphery: Large pitch, large diameter vias do the job
3D Vision for HEP Sensors

Key technologies:
- Multi tier ASICs
- TSV
- High density interconnect

Do the main drivers for industry apply for HEP Sensors?

- **Speed/Power**: we are not yet in the GHz range

- **High density/Pixel Area**: presently pixel area seems rather large
  - ATLAS FEI4: 50 x 250 μm², MEDIPIX/TIMEPIX: 55 x 55 μm²
  
  What is the benefit of smaller pixels (also taking into account power and bandwidth)?
  
  May be an issue for ILC/CLIC or for XFEL applications (memory)
  
  However, we can still profit from some generations of scaling
  
  Latest chips (ATLAS FEI4) use 130nm, 65nm on the horizon (CERN plans to offer 65nm in 2013)

What else?

- **heterogenous technologies** (advanced CMOS sensors, different technologies for analogue and digital part)
- **backside connectivity** (→ 4 side buttable)
Advantages for Module Design

Contact pixels through vias:
- > 4-side buttable.
- > No “cantilever” needed.

Larger module with minimal dead space.

Less support structures & services.
Substantial material savings.

Large pitch of I/O connections allows use of large diameter/low aspect ratio vias
=> Rather mature technology, several vendors
‘no dead space’

- move periphery in between pixels (can keep column logic)
- backside contacts with vias possible
- no cantilever needed, 4-side abutable
- needs to be supplemented by ‘edgeless’ sensors (or: cover large area sensor)
- very interesting for x-ray imager at synchrotron light sources
R&D Activities

1) FERMILAB’s 3DIC
   Tezzaron, MPW, (mainly) 2-tier readout ASIC

2) AIDA WP3
   Network of several projects (mainly) heterogeneous sensor/ASIC assembly
Fermilab: 3D MPW by Tezzaron

- In late 2008 FERMILAB organized a consortium of 15 institutions to fabricate 3D integrated circuits using the Tezzaron/Chartered process.
  - Chartered uses a via middle process to add vias to 130nm CMOS process
  - Tezzaron performs 3D stacking using Cu-Cu thermo compression bonding

I
After FEOL fabricate 6 um super contact (via)

II
Complete BEOL processing

III
Assume identical wafers
Flip 2nd wafer on top of second wafer
Bond 2nd wafer to 1st wafer using Cu-Cu thermocompression bond

IV
Thin 2nd wafer to about 12um to expose super via
Add metallization to back of 2nd wafer for bump or wire bond

TSV: Additional wafers/sensors can be stacked on top of 2nd wafer
Tezzaron Experience

- **Design approach**
  - Two tiers with a single mask set
  - Top tiers on left side and bottom tiers on right side of frame

- **More than 25 two tier designs** (circuits and test devices)
  - ATLAS pixels
  - CMS strip ROIC for track trigger
  - X-ray imaging (VPIC)
  - B-factory and Linear Collider pixels
  - Test circuits

Many problems:

Submission delayed by design and design check problems
Fabrication Problems (some due to transition chartered -> global foundries)
misalignment (1.2mm) made bonding impossible for many wafers
incomplete bonding due to carbon residuals on wafer surface

only few wafers left for 3D bonding
2D devices on these wafers work fine
Working 3D devices delivered recently (talk by Piotr Maj, this session)

Now Tezzaron MPW are offered by CNP/Mosis
EU Supported Projects

- Advanced European Infrastructures for Detectors at Accelerators (AIDA)

**WP1: Project management and communication**
Scientific coordinator Laurent Serin, LAL-CNRS, Deputies: T. Benhe (DESY) & P. Soler (STFC)
Svet Stavrev, CERN administrative coordinator

**Networking**

- **WP2: Common software tools**
  (Frank Gaede, DESY, Pere Mato, CERN)

- **WP3: Microelectronics and interconnection technology**
  (Hans-Gunter Moser, MPG, Valerio Re, UNIBG)

- **WP4: Relation with industry**
  (S. Stapnes → JM Le Goff)

**Transnational access**

- **WP5: Transnational access DESY**
  (Ingrid Gregor, DESY)

- **WP6: Transnational access CERN**
  (Horst Breuker, CERN)

- **WP7: Transnational access European irradiation facilities**
  (Marko Mikuz, JSI)

**Joint research**

- **WP8: Improvement and equipment of irradiation and test beamlines**
  (Michael Moll, CERN)

- **WP9: Advanced infrastructure for detector R&D**
  (Marcel Vos, IFIC Valencia, Vincent Boudry, LLR-CNRS)
AIDA WP3 workpackage on 3D interconnection

The aim is to build demonstrators of 3D vertically integrated pixel sensors, which provide tools to qualify the technologies that are involved in 3D integration and makes them accessible to the community.

WP3 plans to follow a “via last ” approach to 3D integration to build a 2-layer devices in heterogeneous technologies, where the two layers are fabricated independently, and TSVs (Through Silicon Vias) and interconnections are made as the last steps of the process.

1) Bonn/CPPM: Interconnection of the ATLAS FEI4 chips to sensors using bump bonding and TSVs from IZM (large diameter TSV, large interconnection pitch).

2) CERN: Interconnection of MEDIPIX3 chips using the CEA-LETI process.

3) INFN/IPHC-IRFU: Interconnection of chips from Tezzaron/Chartered to edgeless sensors and/or CMOS sensors using an advanced interconnection process (T-MICRO or others).

4) LAL/LAPP/LPNHE/MPP: Readout ASICs in 65nm technology interconnected using the CEA-LETI or EMFT process.

5) MPP/GLA/LAL/LIV/LPNHE: Interconnection of ATLAS FEI4 chips to sensors using SLID interconnection and ICV (high density TSVs) from EMFT.

6) Barcelona use a 2-tier approach to increase the fill factor of APD-sensors (based on Tezzaron/Chartered).

7) RAL/Uppsala: 2-Tier Readout Chip for CZT X-ray sensor using EMFT-SLID technology.
Improve performance of CMOS sensors by 3D

NMOS transistors in CMOS sensors act as parasitic charge collection nodes

⇒ Restricted circuitry
⇒ Inefficient charge collection

Solution:
Place (most) of the complex circuitry in a second tier

20µm pitch monolithic sensor
Digital tier with sparsification and time stamp.
Interleaved readout (matched to ILC beam structure)

Fabricated by Tezzaron

Successfully tested (Threshold scan)
SLID & TSV by Fraunhofer EMFT

- SLID interconnection replacing solder bumps
- Small pitch (limited by alignments precision of flip chip)
- Stacking possible
- Pitch < 20 µm in view

ICV (Inter Chip Vias)

Tungsten filled vias
Aspect ratio: 8:1
VIA diameter > 2 µm
0.3 Ohm for 2x2x20µm³

Etching (Bosch process)
Insulation, filling with tungsten
Electroplating, metallisation
Back thinning
3D demonstrator (aimed for ATLAS pixel upgrade)
Based on ATLAS FEI3 chip
Thin sensors made at MPI HLL
SLID interconnection by EMFT
TSV by EMFT

1st step: SLID only (no TSV)

Successful (however, problems with alignment & interconnection yield in some chips)

2nd step: SLID & TSV

Trials on dummy FEI3 wafer ok
Now: full process on hot wafers & sensors
Problems with FEI4

FEI3: pads clear of active structures (luckily!) No problem to etch via from front side

FEI4: metal structures below I/O pads Not possible to etch from front side

Would be ok, since M1 is connected to I/O pad

Etching from the backside:

For narrow, high aspect ratio vias: Not possible to open contact to copper Without destroying TSV wall insulation & barriers

Large (40µm diameter) low aspect ratio vias are possible (especially tapered ones)

⇒ Ok for large pitch I/O pads
⇒ Excludes high density vias (pixel to pixel)

⇒ Be careful with chip design and layout!
Bonn: TSV in ATLAS FEI3/FEI4

Similar to MPI project, in collaboration with Fraunhofer IZM

- use very thin (~100 µm) FE-I4 (2x2 cm²) chips
- use TSV for the routing of signals on the chip backside

Fraunhofer IZM

Tapered vias
90 µm diameter (outer)

Bump bonding
60 µm pitch
Medipix 3: TSV friendly

Normal connection:
Wire bonds pads at top and bottom

TSV area behind pads

Metal 1 connected to I/O pad

If connected with TSV, wire bond area can be diced off

TSVs processed by CEA-LETI
Via diameter 40-80 µm
Minimum pitch 80 µm
Conclusions

3D technology with TSV is now being pushed by industry
2.5 D interposer & memory stacking

large pitch, large diameter vias with low aspect ratio (via last) is
offered now by many vendors:
e.g. in Europe: CEA-LETI, Fraunhofer IZM, VTT, IMEC

High density TSV (via first) still on the roadmap
(no large volume products yet)

Several R&D projects in HEP (and photon science) exist
(FERMILAB 3DIC, AIDA WP3)

Most do post processing (via last) with large diameter TSV (~ 50 µm,
aspect ratio 3:1) for backside connectivity

⇒ can be used in the near future

Some work on high density, small diameter vias (<5µm, > 10:1)
Tezzaron (via first, ROC only)
Fraunhofer EMFT (via last)
T-Micro

⇒ more technical difficulties, will take more time (and money!) to
reach maturity