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Fast, granular and ultra-light pixelated double sided ladders based on CMOS sensors for an ILC vertex detector adapted to the ultimate collision energy

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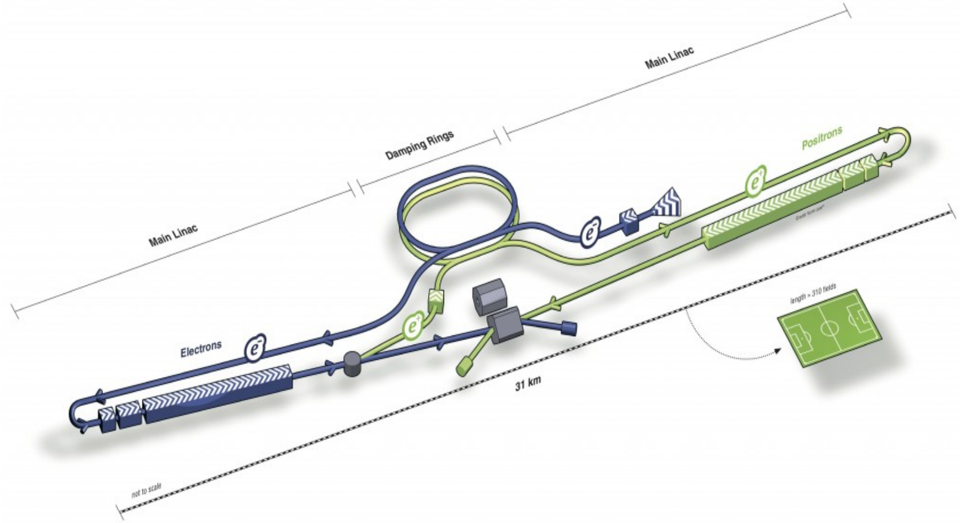
dépasser les frontières

Outline

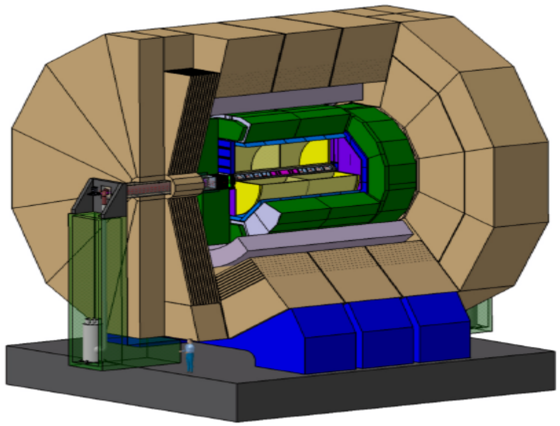
- ILD Vertex Detector (VXD)
  - Physics motivation & requirements
- CMOS baseline architecture
- CMOS sensors based VXD
  - Design for $\sqrt{s}$ = 500 GeV
    - Inner layer sensors
    - Outer layers sensors
  - Design for $\sqrt{s}$ = 1 TeV
    - Moving to 0.18 µm CMOS technology
    - MIMOSA 32 test beam results
- Conclusions – perspectives

ILC & ILD

- Future linear e^+e^- collider, $\sqrt{s}$ = 500 GeV – 1 TeV
- Main motivations
  - Study of EWSB
  - Search and detailed study of new physics



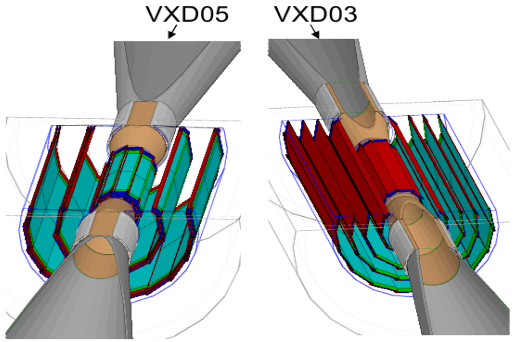
- 2 general purpose detectors, ILD & SiD
  - Letter of Intent (LoI) delivered in 2010
  - Detector Baseline Document (DBD) under preparation
    - To be delivered by the end of 2012

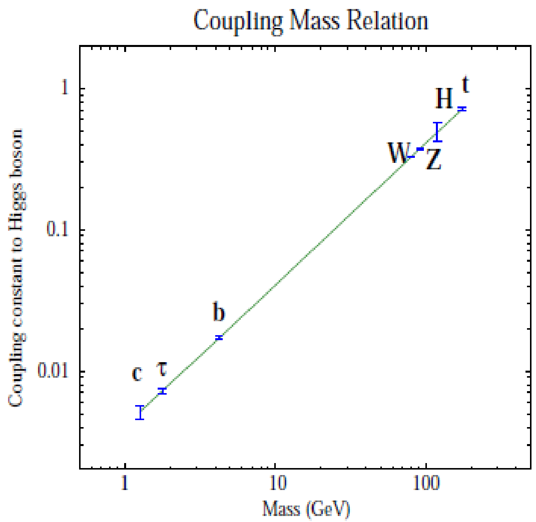


Japanese HEP community approved ILC (August 2012)

VXD physics motivations

- Excellent “heavy” flavour tagging
- Standalone track reconstruction (low mom. tracks)





ILC expected sensitivity

- Prominent example: measurement of the Higgs couplings
  - Requires excellent flavour tagging capabilities (b, c, τ)
  - Main challenge, tag c – hadrons ($c\tau \sim O(100\ \mu m)$) and τ leptons ($c\tau = 87 \mu m$)
  - Required Impact Parameter (IP) resolution ~ 10 μm

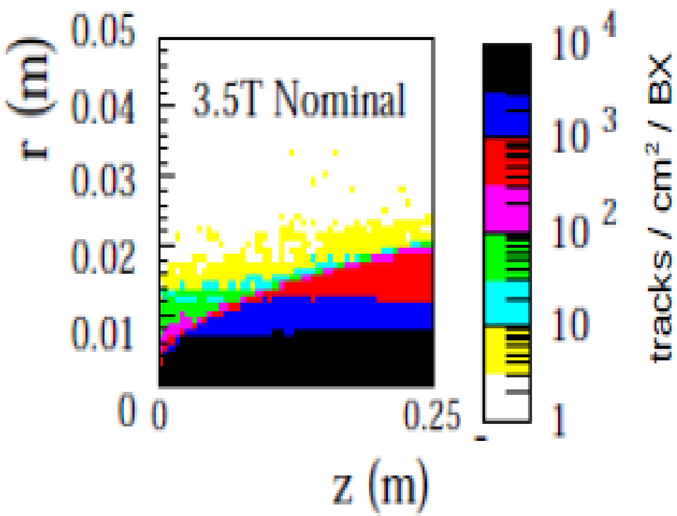
$$\sigma_{IP} = a \oplus b/p \cdot \sin^{\frac{3}{2}}(\theta)$$

- → $a \leq 5\ \mu m$
- → $b \leq 10\ \mu m\ GeV / c$

Accelerator	a (μm)	b (μm·GeV/c)
LEP	25	70
SLC	8	33
LHC	12	70
RHIC-II	13	19
ILD	< 5	< 10

VXD Requirements

- ILD physics program needs sensors
  - Highly segmented (s.p. resolution ~ 3 μm)
  - Thin (ladder X/X_0 in the per mill level)
  - Low power consumption → less complex cooling strategy
- ILC running conditions impose also certain requirements
- Dictated by the beam induced background (e^+e^- pairs)
  - Swift readout
    - O(10 μs) for the innermost, O(100 μs) for the outer layers
  - Moderate radiation tolerance
    - Expected 150 kRad, 10^{11} n_{eq}/cm^2 per year, sf 3

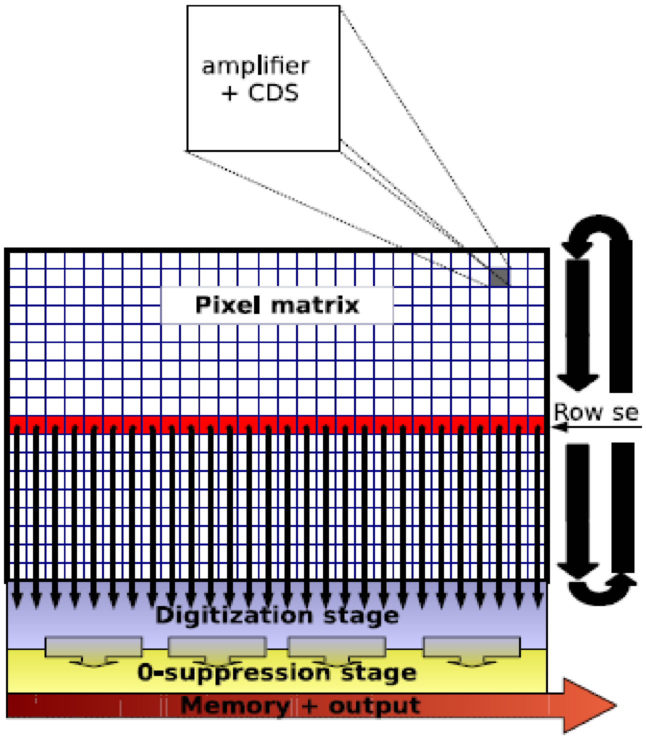


Beam bkg track density

- CMOS sensors is a candidate technology that can fulfill the VXD specifications

MIMOSA sensors baseline architecture

- Baseline architecture: rolling shutter approach
  - Only the selected row is switched on
    - Power saving!
  - Column parallel read-out, in pixel amplification & CDS
  - Column level discriminator + 0 suppression in sensor periphery
  - Integration time ~ to number of pixels / column
- Example: MIMOSA 26
  - Full scale digital sensor with integrated sparsified output
  - 1152 columns x 576 rows of 18.4 μm pitch pixels
  - Thinned down to 50 μm
    - 2 cm^2 - 660k pixels
    - 100 μs read-out
    - ~ 3 – 3.5 μm spatial resolution (charge sharing)
  - AMS 0.35 μm fabrication process (high resistivity)
  - Developed to equip the EUDET beam telescope

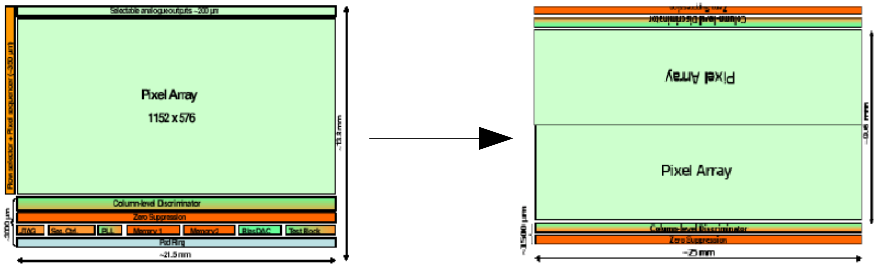


Challenges

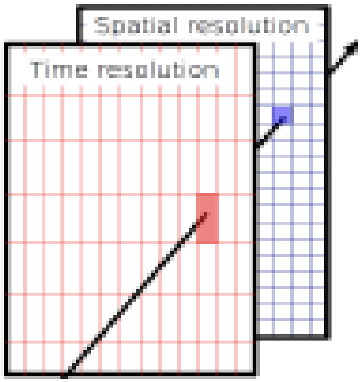
- ILD sensors requirements are in the physics dominated area
- But beam bkg → swift readout @ innermost layer
- **Challenge**
  - Swift readout while preserving spatial resolution
- **Conflict**
  - Spatial resolution → high segmentation
  - Time resolution → low number of channels
- MIMOSA sensors offer genuinely
  - High spatial resolution &
  - Low material budget
- R & D effort focus on running constraints requirements

Towards 10 μs readout time

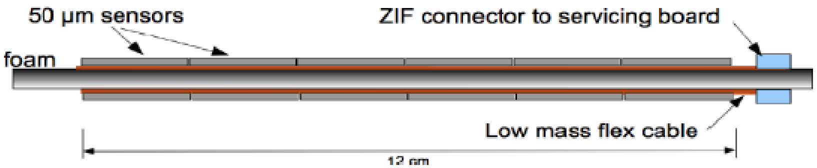
- How can we go from 100 to 10 μs readout time?
- Reduce the number of pixels / column
  - Apply a double sided readout
    - The insensitive area is double but
    - Going to smaller feature size CMOS technology → decrease of the overall insensitive area



- Then exploit double sided ladders benefits
  - Correlate hits of the same, traversing, particle on both surfaces (2 mm distant)



- Double sided ladders
  - Investigated by PLUME collaboration



  - First prototype with 0.6 % X_0 (6 MIMOSA 26 per side) properties tested in 2011 (mechanical, electrical, cooling)
  - Second prototype tests (0.35 % X_0) foreseen for late 2012

CMOS based VXD – proposal for $\sqrt{s}$ = 500 GeV

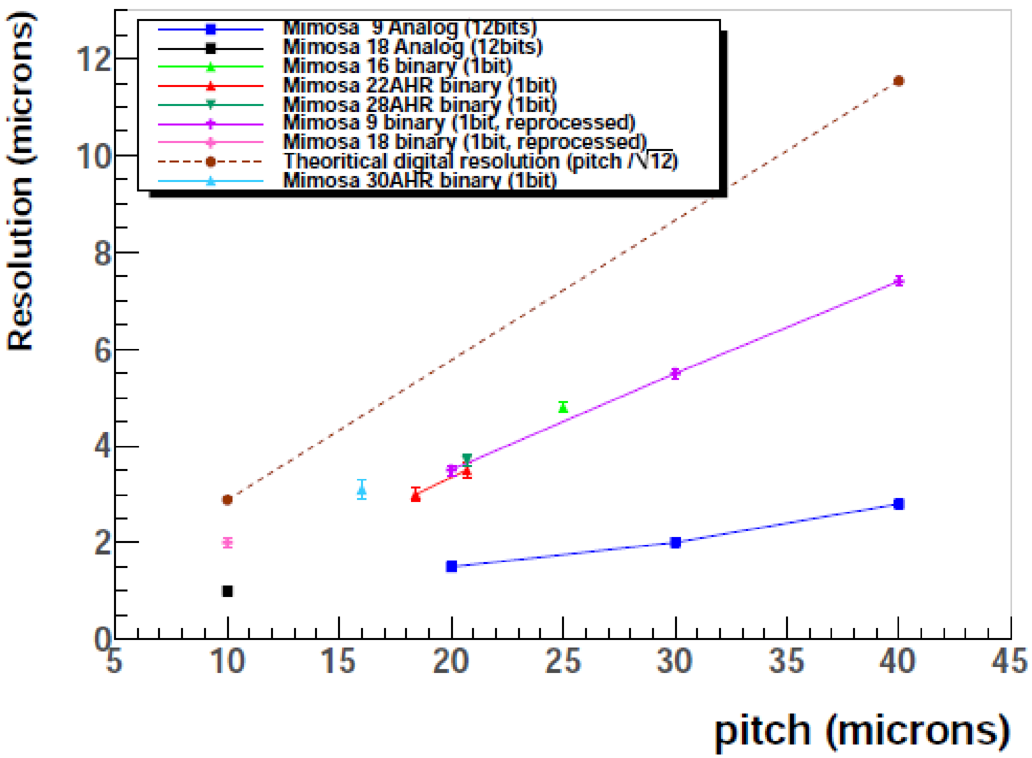
- Adopt rolling shutter approach
- Discrimination & data sparsification @ sensor's periphery
  - **Inner layers → priority to spatial resolution and readout speed**
    - One face: highly segmented digital square pixels sensors 16x16 μm^2
      - Spatial resolution < 3 µm
    - Other face: elongated pixels in column direction 16x80 μm^2
      - Time resolution ~ 10 µs
  - **Outer layers → priority to power saving**
    - Larger pixels 34x34 μm^2 → reduced power dissipation, data flow
    - Columns ended with 3-4 bits ADCs
      - Expected spatial resolution ~ 3.5 µm
  - Average power consumption of whole VXD < 15 W
    - Compatible with moderate air flow cooling
    - Take advantage of the beam time structure - 2 % duty cycle
- Three different sensors
  - Inner layer: square & elongated pixels (MIMOSA 30)
  - Outer layers: large pitch pixels (MIMOSA 31)

layer	$\sigma_{spatial}$ (µm)	σ_{time} (µs)
L1	3 / 6	50 / 10
L2	4	100
L3	4	100

Feasible today with 0.35 µm process

Spatial resolution

- Spatial resolution as a function of pixel pitch
    - Square pixels



- Resolution study of elongated pixels
    - MIMOSA 22 AHR
    - Pixel's dimensions 18.4 x 73.6 μm^2
        - Digital output
    - ~ 6 µm spatial resolution in each direction

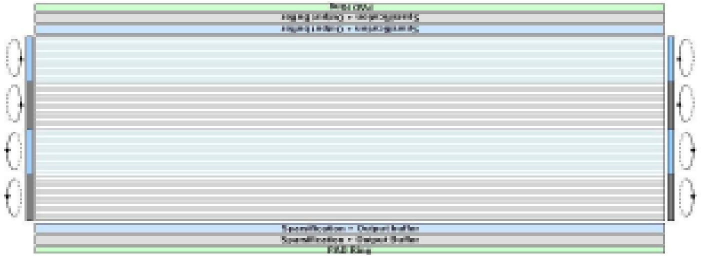
CMOS based VXD – proposal for √s ≥ 1 TeV

- √s ≥ 1 TeV → occupancy due to beam bkg increased ~ 3-5 times
- To account for uncertainties in beam bkg simulations
  - Increase the readout speed of the VXD layers →

layer	$\sigma_{spatial}$ (μm)	σ_{time} (μs)
L1	3 / 6	50 / 2
L2	4 / 10	100 / 7
L3	4 / 10	100 / 7

How can we further improve readout?

- **Move to 0.18 μm process**
- **In-pixel discriminator**
  - Don't have to drive the digital signal to the column end
    - Gain a factor of 2 in time resolution
  - 2 -4 rows readout simultaneously
  - Multiple rolling shutters



→ More rows switched on → higher power consumption: **but**

→ 0.18 μm process offers reduced power dissipation

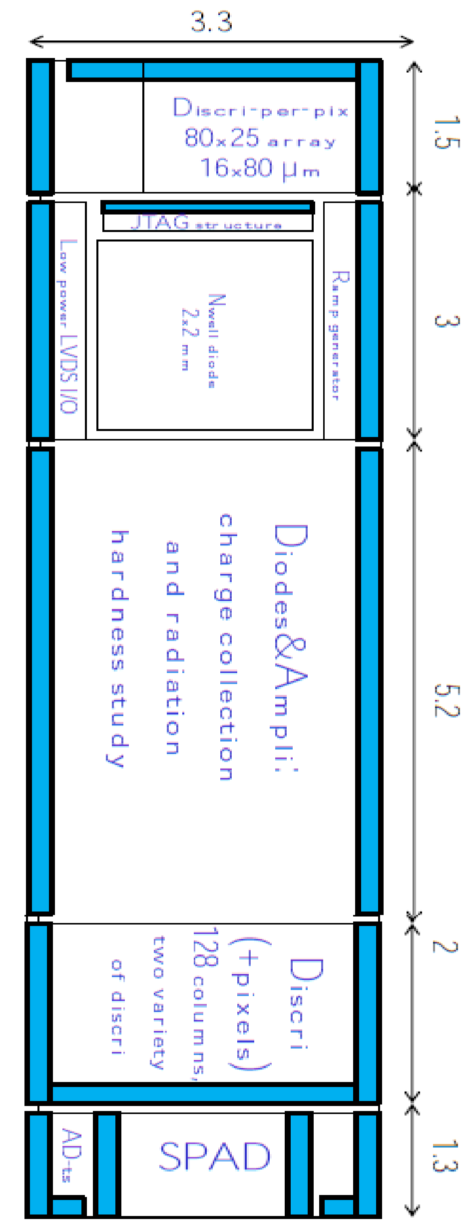
→ Still complies with a passive cooling system

- time resolution < 2 μs can be achieved

- **2 discriminators / column**
  - More conservative approach
  - Fit in 22 μm wide column
  - Readout of ~ 5 μs can be achieved
  - Feasible with 0.35 μm technology
    - Small ins. area in fiducial volume

0.18 µm prototype sensor

- Scope of MIMOSA 32: exploration of 0.18 µm process
  - High res. epi – layer (1 → 5 kΩ · cm)
  - Quadruple well (deep P-wells hosting PMOS transistors)
  - 4 metal layers
- Various pixel designs
  - Squared or elongated pixels (with 1 or 2 charge coll. diodes)
  - Pixel matrices with column level discr.
  - In – pixel discriminators
- Future steps
  - **<u>MIMOSA 32ter</u>**
    - In – pixel amplifier + discriminator + 6 ML
    - Submitted July 2012
  - **<u>MIMOSA 22 THR</u>** (ALICE ITS upgrade prototype)
    - Full analog chain + 2 discr. / column
    - 128 columns readout in parallel (1 cm long)
    - 8 – 10 diff. in – pixel amplifiers
  - **<u>AROM 1</u>**
    - In – pixel discr, 4 rows read – out simultaneously
    - Submission: 2013

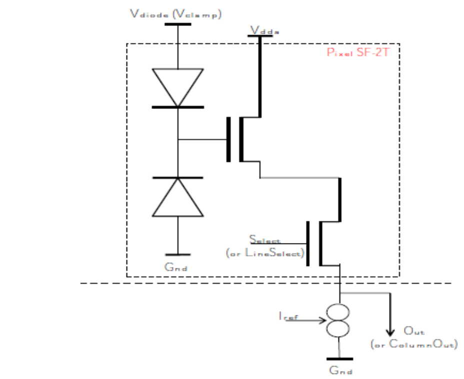


MIMOSA 32 test beam results

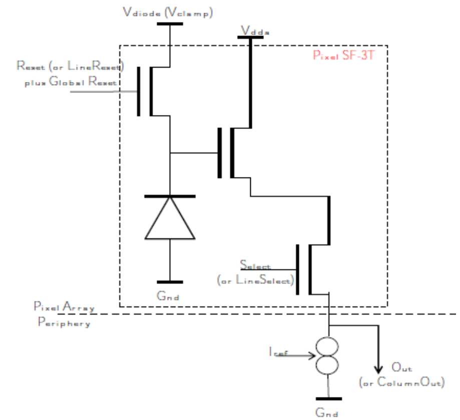
T = 15^{0}C

Pixel design	Irradiation	S / N	Efficiency (%)
P1	0	35.1 ± 0.4	99.97 ± 0.03
P1	1 MRad + 10^{13} n_{eq}/cm^2	25.4 ± 0.3	99.67 ± 0.12
P6	0	32.3 ± 0.4	99.84 ± 0.07
P6	1 MRad + 10^{13} n_{eq}/cm^2	22.3 ± 0.3	99.87 ± 0.08
P9	0	30.9 ± 0.4	99.91 ± 0.06
P9	1 MRad + 10^{13} n_{eq}/cm^2	22.6 ± 0.4	99.92 ± 0.08
L4_1	0	22.6 ± 0.2	99.86 ± 0.06
L4_1	1 MRad + 10^{13} n_{eq}/cm^2	13.9 ± 0.3	99.51 ± 0.25
L4_2	0		
L4_2	1 MRad + 10^{13} n_{eq}/cm^2	13.3 ± 0.2	99.0 ± 0.2

- P1 (SB) →



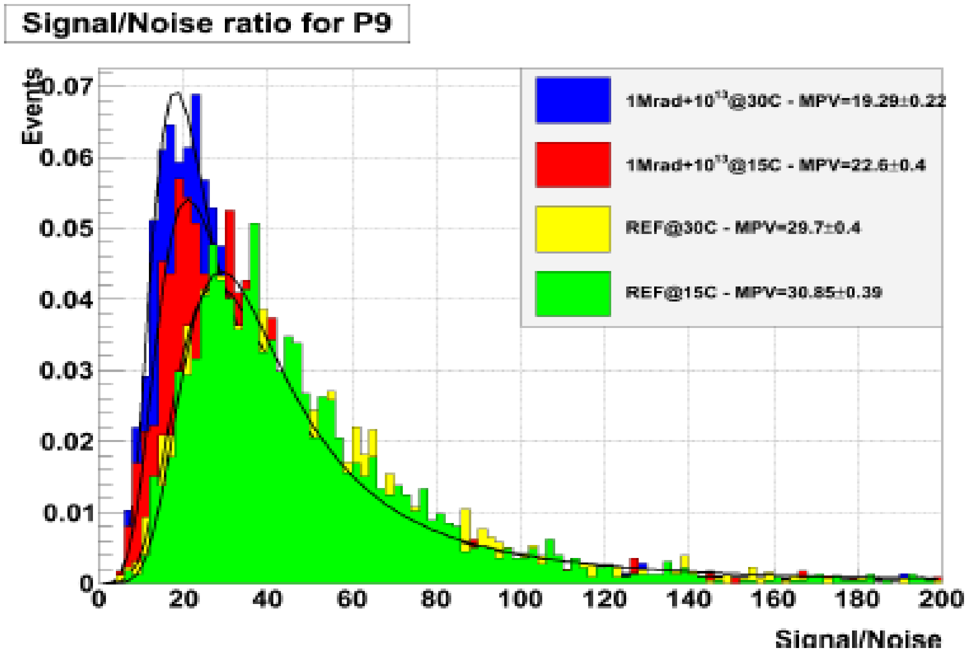
- P6 (3T) →



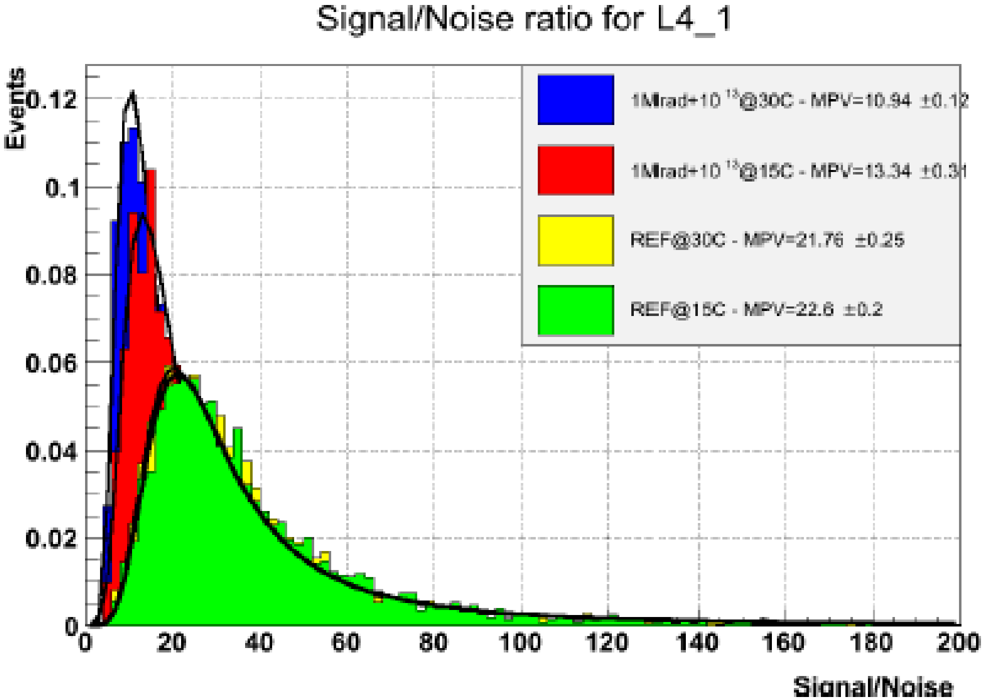
- P9: quadruple well
- L4_1: elongated (20x40 μm^2), 1 diode / pixel
- L4_2: elongated (20x40 μm^2), 2 diodes / pixel

- Square pixels: S / N, efficiency satisfying for irradiation levels >> ILC environment
- Elongated pixels: validated for ILC

MIMOSA 32 test beam results (S/N)



- P9: Quadruple well



- L4_1: 20x40 μm^2 dimensions, 1 diode / pixel

Summary

- ILD physics program requires a very granular, light vertex detector
  - CMOS sensors technology offers genuinely these qualities
  - Rolling shutter r/o → low power
- But due to beam bkg → swift readout for the inner layers
- **Approach for √s = 500 GeV**
  - Based on rolling shutter readout & exploit double sided structure of the ladders
  - Innermost layer
    - 10 μs time stamping, 3 μm spatial resolution
    - Status
      - MIMOSA 30 tests under way (square & elongated pixels)
      - Double sided ladder tests: late 2012
  - Outer layers
    - Large pixel pitch, spatial resoluiton ~ 3.5 μm
    - Status
      - MIMOSA 31 tests foreseen at beginning 2013
  - P_{avg} < 15 W for whole detector (0.35 μm process) → air flow cooling

Summary

- **Approach for $\sqrt{s}$ = 1 TeV**
  - Move to 0.18 µm process
    - In – pixel discriminator, r/o of multiple rows simultaneously, multiple rolling shutters
    - Time stamping improves by an order of magnitude
    - 0.18 µm process → less power consumption
  - Status
    - MIMOSA 32 under test
    - First techn. fully adapted to ILC VXD requirements
      - Exhibits satisfactory S/N (≥30), detection ε performances
        - Even for much higher irradiation level than expected in ILC
      - Resolution measurements under way
    - MIMOSA 32ter submitted
    - MIMOSA 22 THR to be submitted in Dec. 2012
    - AROM 1 @ 2013