TITLE:
Fast, granular and ultra-light pixelated double-sided ladders
based on CMOS sensors for an ILC vertex detector adapted to
the ultimate collision energy

ABSTRACT :

The ILC is a major option for the future of High Energy Physics.
Its precision, flexibility, and advantageous running conditions
provide the tool to investigate in detail the origin of EW symmetry
breaking and of the particle masses, as well as to unravel the
physics beyond the Standard Model. An experimental set-up with
unprecedented accuracy is however mandatory to exploit its physics
potential. This applies in particular to flavour tagging, which
relies on the achievement of a particularly granular and low mass
vertex detector.

CMOS pixel sensors are considered since long as an option for
a vertex detector of ILD, one of the two experimental concepts
developed for the ILC. The required, non-trivial, trade-off between
high granularity, fast enough read-out and low power is achieved by
combining a sensor rolling shutter architecture with a double-sided
ladder design.

The rolling shutter consists in reading the pixel matrix
sequentially, single row after single row, and in transmitting
the pixel analog signals to discriminators implemented at the
sensor periphery, where they get digitised. In this way, the
large amount of pixels consecutive to their small size (16-17 mum
pitch) generates a moderate pixel matrix consumption, restricted
to the row being read out. The read-out being sequential, it is
nevertheless close to a problematic regime in the detector innermost
layer if the beam related background happens to be higher than
expected from Monte-Carlo simulations. This weakness is getting
under control by equipping the detector ladders on each of their two
faces, one with sensors providing the necessary spatial resolution
and the other with another set of sensors, which are 5 times faster
but twice less accurate.

This approach is followed in the ILD Detector Baseline Document
(DBD), the step consecutive to the Letter of Intent submitted in
2008, to be handed over to the review committee IDAG by the end of
2012.

In its first part, the talk will expose the approach and show
that recent progress achieved with the sensor architectures and
with the double-sided ladder concept allow complying with the
specifications of the vertex detector of the ILD detector concept
running up to 500 GeV.

In its second part, the talk will address a faster sensor
architecture, based on in-pixel discrimination and highly
parallelised rolling-shutter read-out. Expected to accelerate
the read-out by nearly an ordre of the magnitude, it exploits a
newly addressed CMOS technology with 0.18 mum feature size (instead
of the 0.35 mum process used previously). The talk will overview
the perspectives and activities of this new step of the R&D, which
is expected to allow for vertex detector based standalone tracking
and to face the enhanced beam background foreseen at the highest
energy operation of the ILC (> 1 TeV). It will in particular summarise
beam test results obtained with the first sensor prototypes, focusing
on the charged particle detection performances of the technology.