First Three-Dimensionally Integrated Chip for Photon Science

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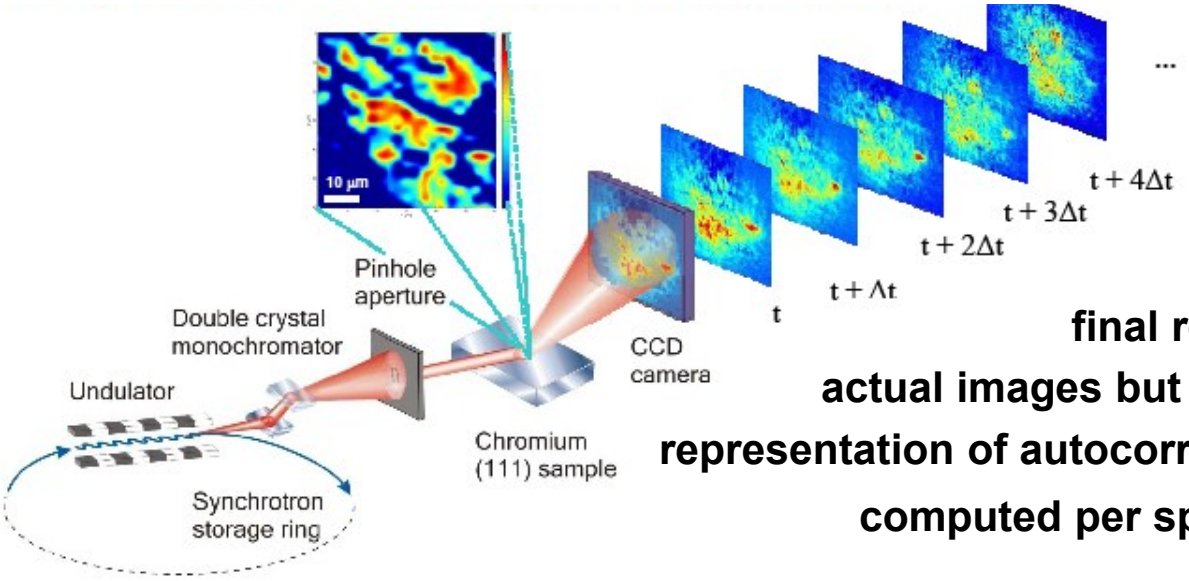
- **OUTLINE:**
  1) Application,
  2) Specification,
  3) Mounting options on the detector
  4) Architecture of Analog and Digital
  5) Testing Results of Digital and Analog part
  6) Summary.

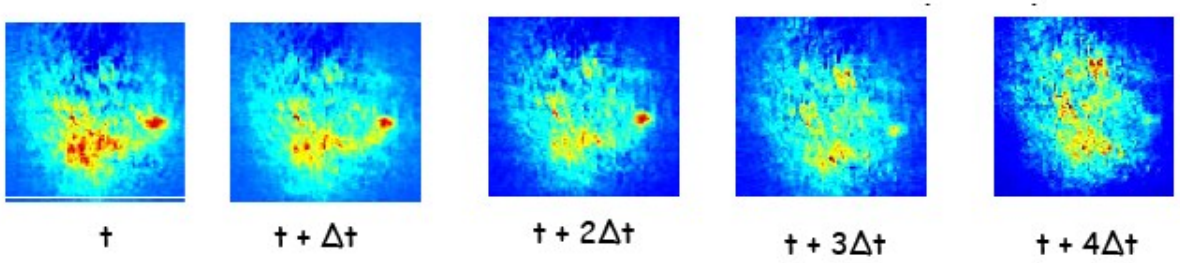
Application: X-ray Photon Correlation Spectroscopy

To study the dynamics of various equilibrium and non-equilibrium processes occurring in condensed matter systems



final results are not actual images but mathematical representation of autocorrelation series computed per spatial position

the speckle pattern changes



O. G. Shpyrko et al., *Nature* **447**, 68 (2007)

target is to output time stamped information Δt=10 μs for long exposure times; very low occupancy < 10 ph/mm^2/10μs

Design specification

Technology:

2 wafers with Cu-Cu thermocompresion BI by Tezzaron, **CHRT 130 nm** (6 metal layer) is supplemented by insertion of **TSV (6 um deep, min space 3.8 um)** after completion of FEOL

Geometry:

64 × 64 array of **80x80 μm² pixels,** 5120 × 5120 μm² active surface (Die size 5.5 × 6.3 mm²)
1st tier – analog part, **2nd tier – digital part**,

Analog part:

Architecture of single pixel: **CSA + shaper + discriminator** (trimming and testing options)
Optimized for **8 keV X-ray** photons (up to 3 × 8 keV with Si detector),
Shaping time **tp=250 ns, ENC <150 e-**, pwr **~25 uW** / analog pixel

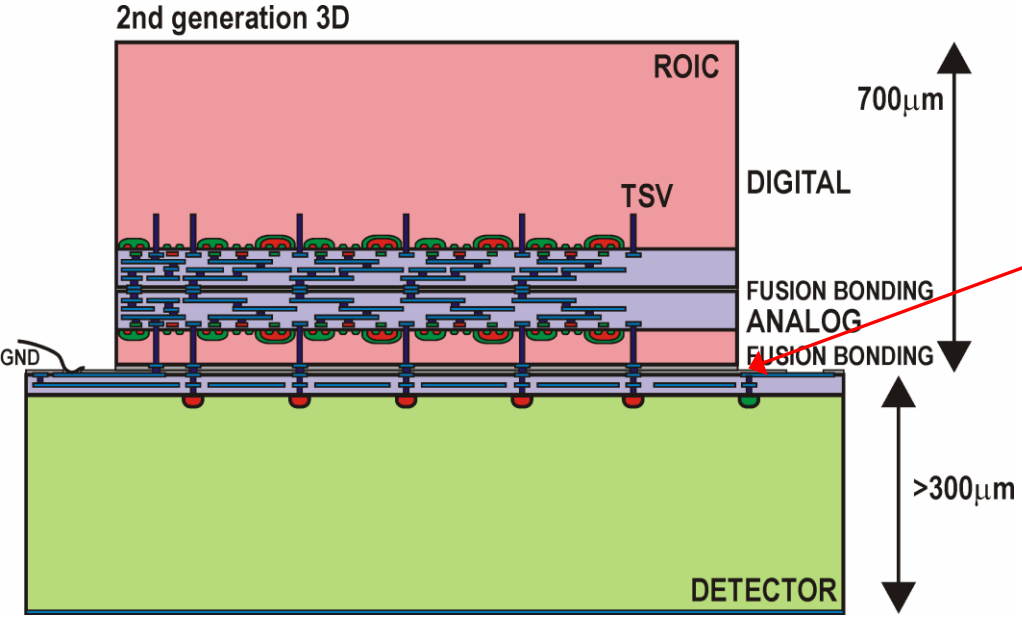
Digital part:

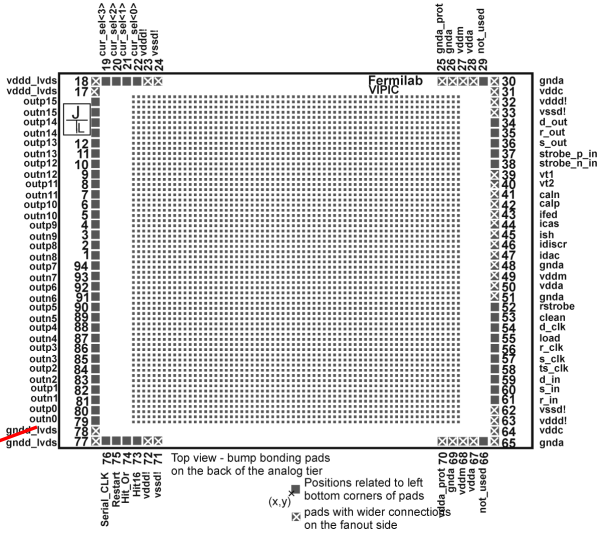
Two modes of operation:
1) timed readout of hits acquired at low occupancy (**address and hit count,**
10 μs frame readout time)
2) **imaging** (two 5 bit-long counters / pixel accumulates hits occuring in each time slot, readout uses sparsification mechanism but no readout of addresses)
Dead timeless operation (operation divided into time slots: hits arriving in time Δt_{n-1} are read out in Δt_n while simultaneously new hits are being acquired in time Δt_n).**Sparsified data readout** based on priority encoder circuit (binary tree) with automatic binary-coded generation of hit pixel addresses. **Hit pixel address readout only**.

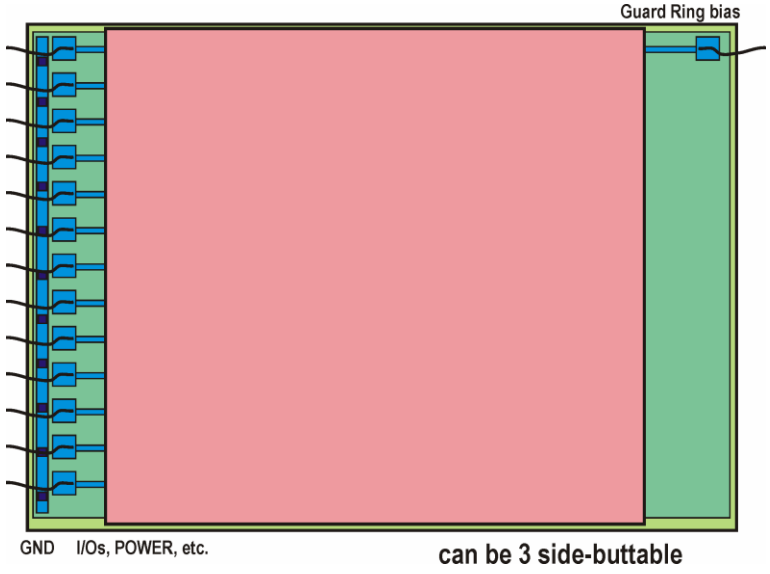
Mounting options on the detector

- OPTION 1

– LESS AGGRESSIVE MOUNTING







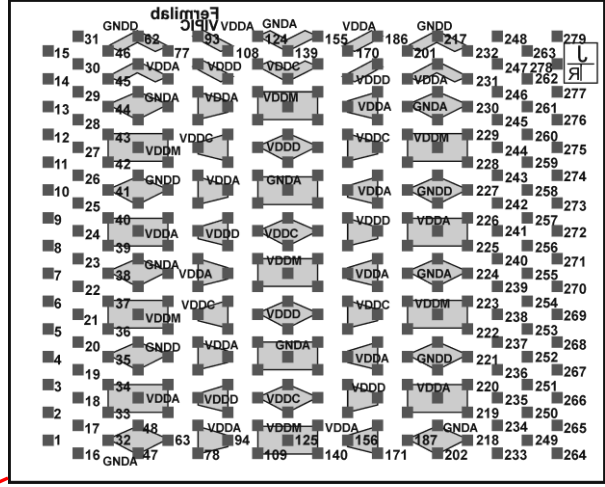
- Access to signals, power supplies and biases, etc. :

 - fanout/routing on the detector, pads created on the detector, wire bonding to mount in the system

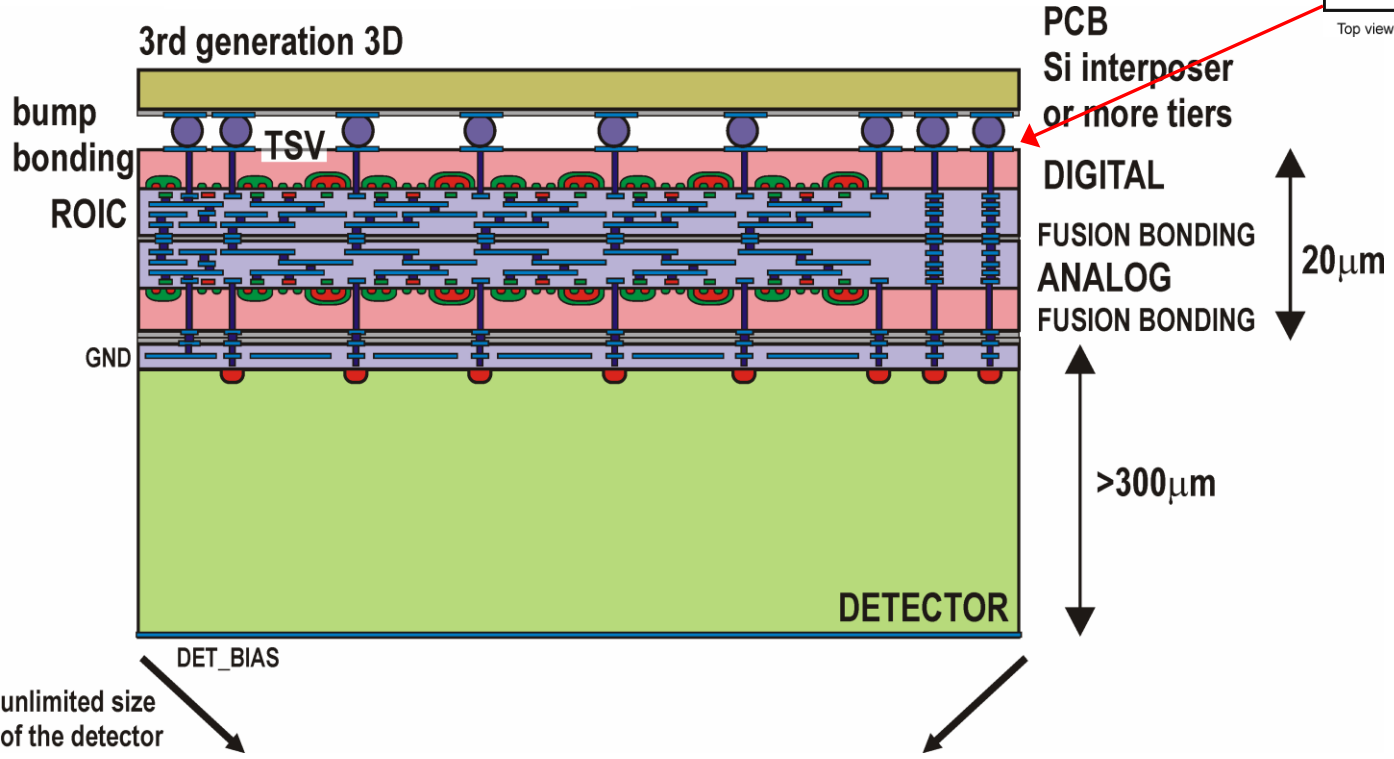
Mounting options on the detector

- OPTION 2

– MORE AGGRESSIVE MOUNTING for 4-side buttable sensor arrays and improved power distribution

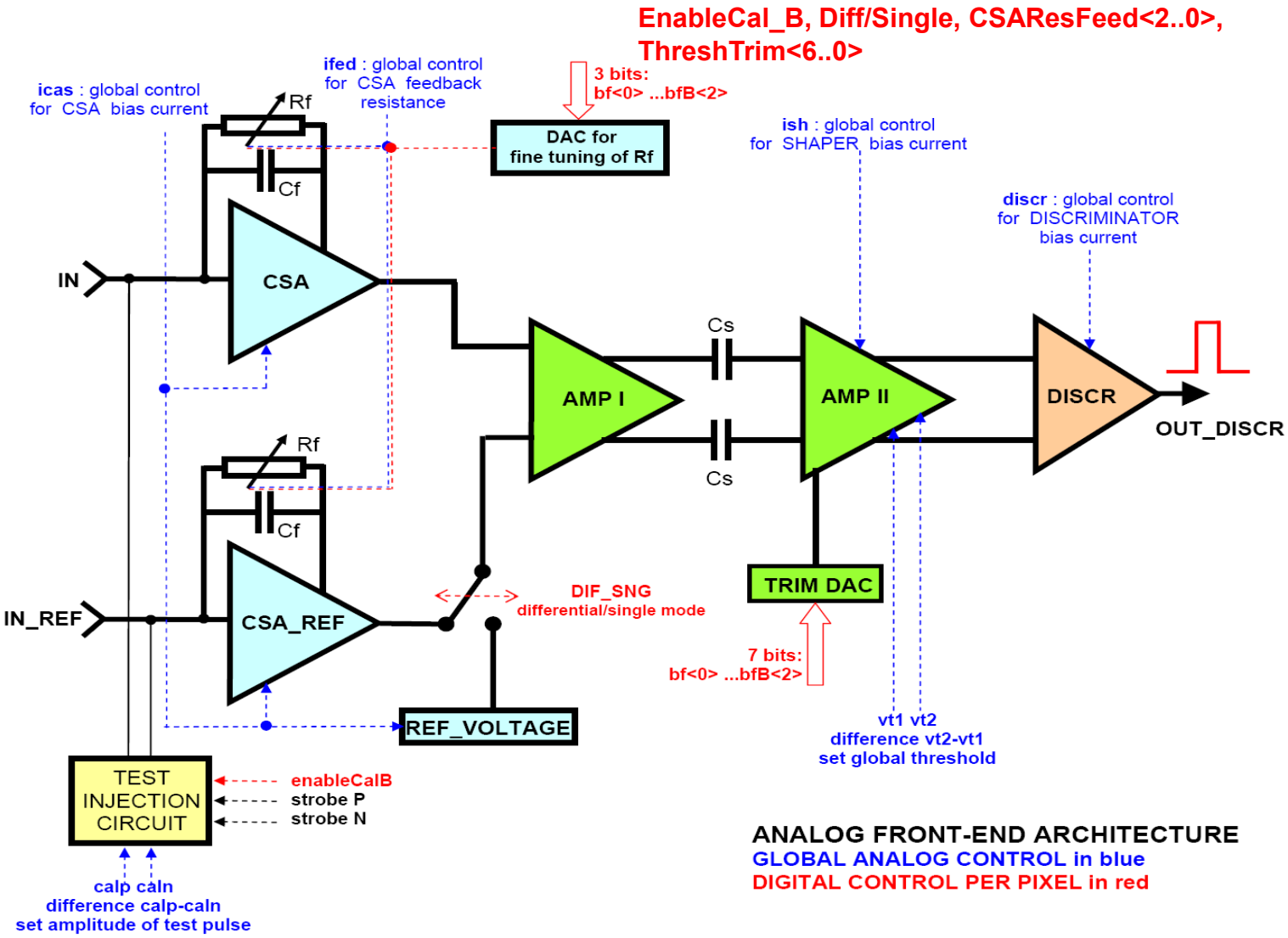


Top view - bump bonding pads on the back of the digital tier



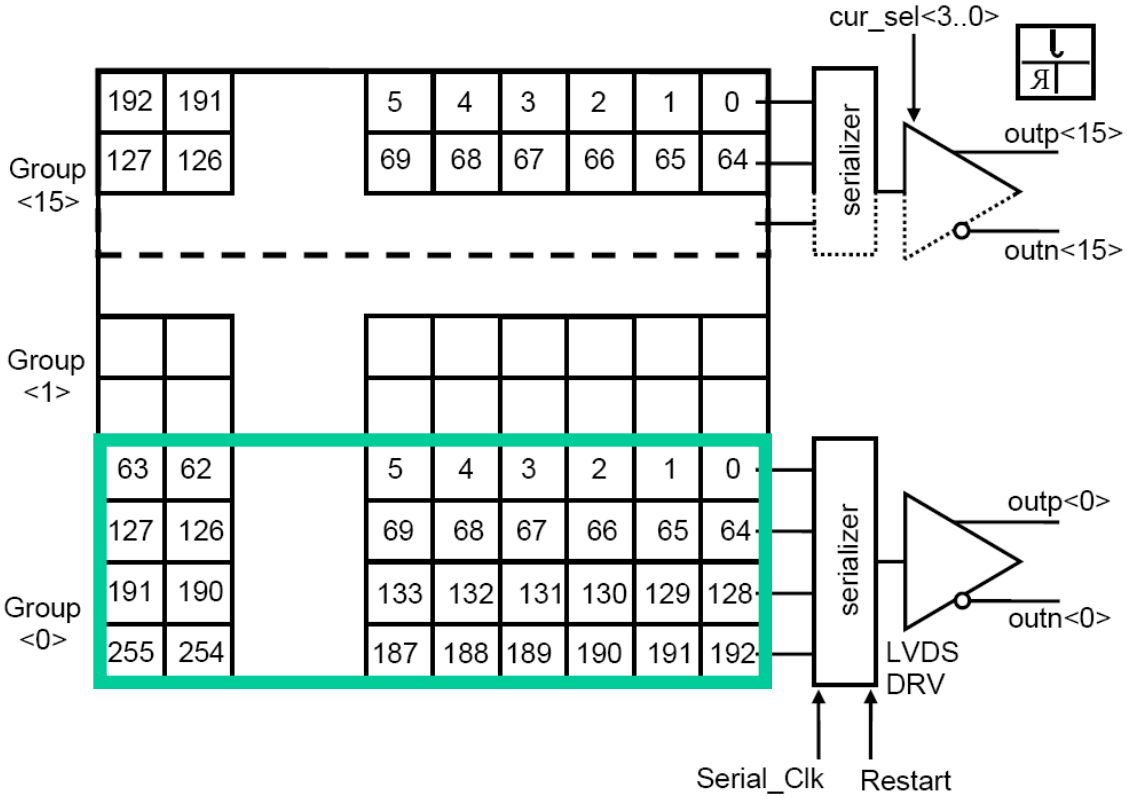
- both-side bonding (thinning, exposing TSV, deposition of bonding pads)

Analog circuitry



Digital circuitry

64 × 64 matrix divided in 16 submatrices of 4 × 64 pixels
– readout out LVDS with 100 MHz

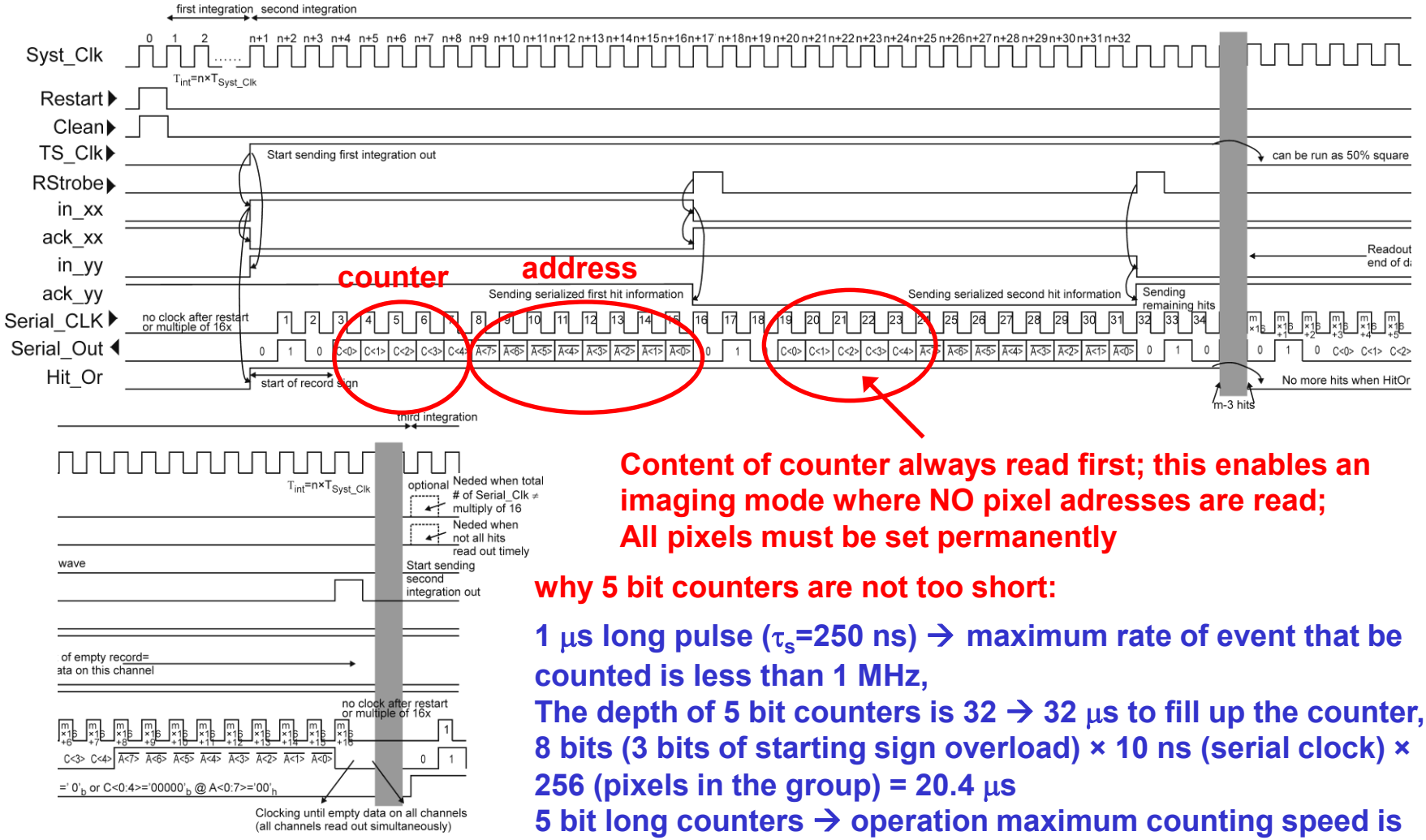


The chip is designed to yield 10 μs frame readout time at the mean occupancy of 3.8×10^8 photons/cm^2/s.

The data sparsification circuity is running simultaneously in each group. The sparsification circuity (Modified version of MEPHISTO chip – P. Fischer, NIMA461, 2001) is common for each group of 256 pixels. It is primary a multi-input logic OR gate integrated with priority encoder. The encoder selects pixels automatically in the binary code. The layout of the sparsification circuit is distributed into all pixel.

Details of circuitry - Digital

Full timing diagram of readout sequence

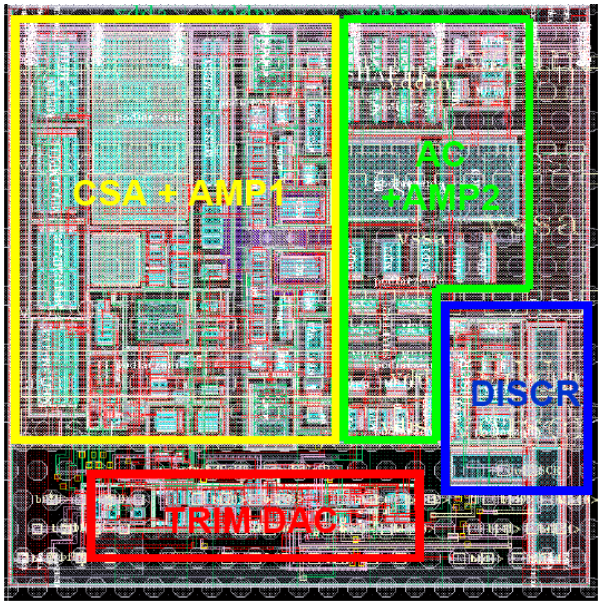


Content of counter always read first; this enables an imaging mode where NO pixel adresses are read; All pixels must be set permanently

why 5 bit counters are not too short:

1 μs long pulse (τ_s=250 ns) → maximum rate of event that be counted is less than 1 MHz,
The depth of 5 bit counters is 32 → 32 μs to fill up the counter, 8 bits (3 bits of starting sign overload) × 10 ns (serial clock) × 256 (pixels in the group) = 20.4 μs
5 bit long counters → operation maximum counting speed is dictated by the front-end circuitry. continuous readout 1000 hits/1ms/pixel (equivalent of 10bits counter depth)

Details of pixel layouts: 80 x 80 μm²



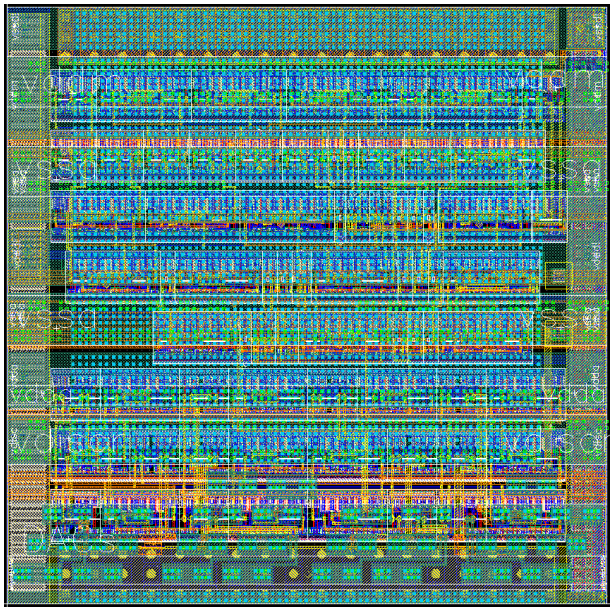
12-bit for configuration

7-bit trim offset, 3-bit trim RF,

single/dif mode, CAL enable

2-lines for CAL circuits

discriminator output



Analog part of pixel

Digital part of pixel

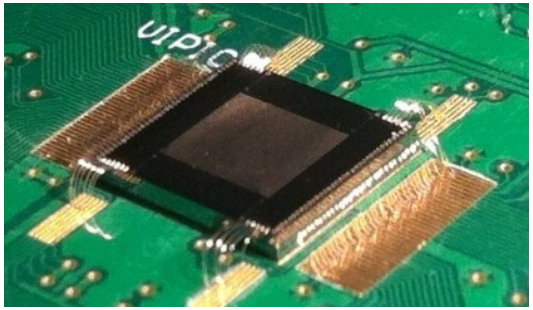
2 x TSV
for detector contact

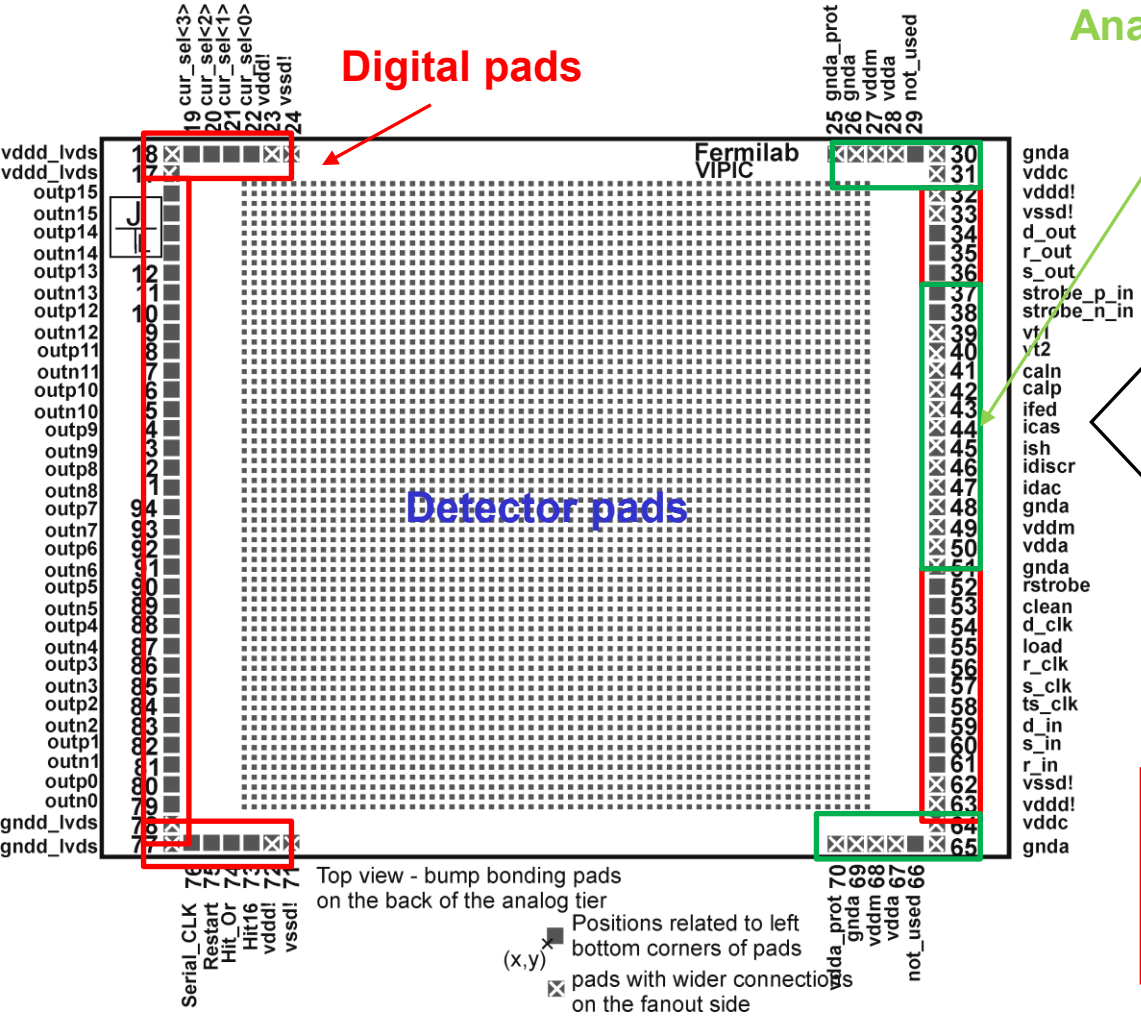
2 x 3D bond
pads for each signal

Power suplies lines tied between tiers

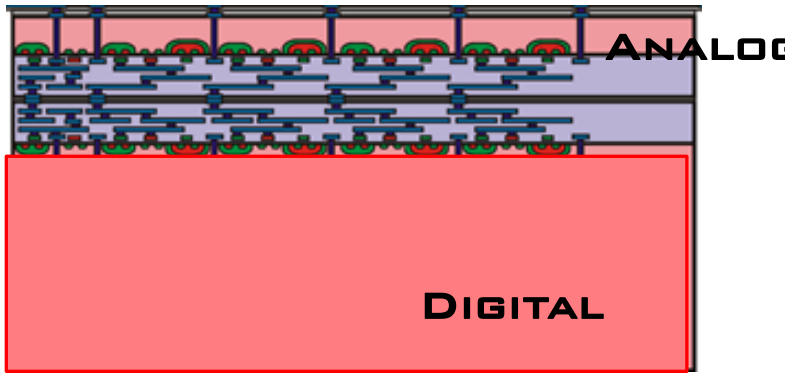
VIPIC IC - Tests of the 3D Pixel Chip

Two versions of VIPIC chips were made - tested only one

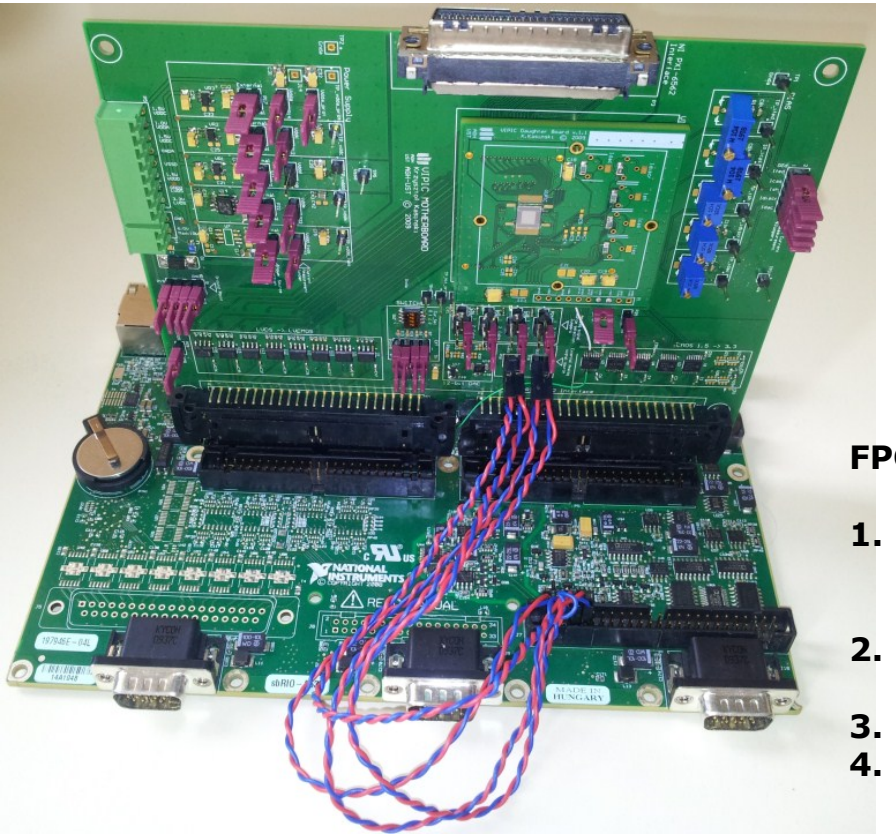


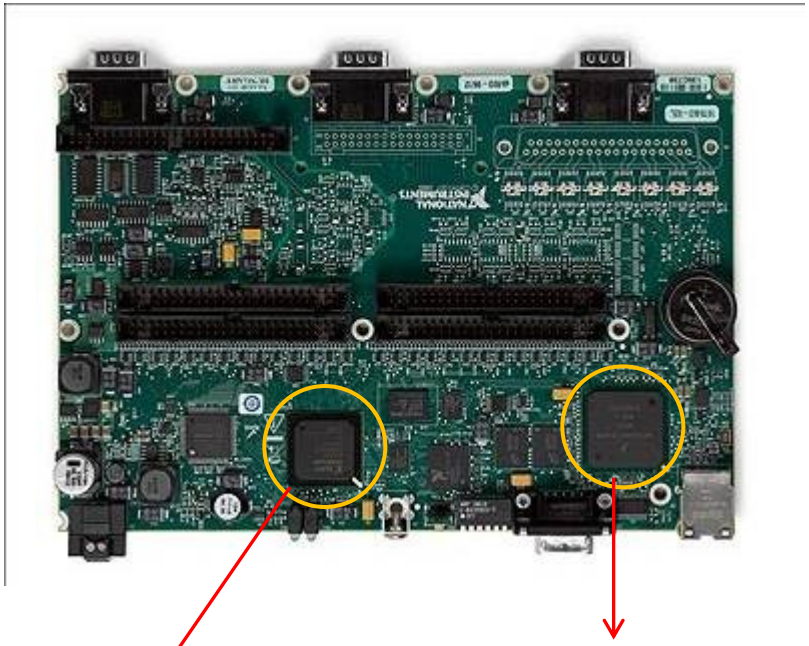


Top view of bonding pads



Testing Setup - photo





FPGA Tasks

1. **Load data to the registers (3 registers, 3 lies per register)**
2. **Control signals generation (4 DO lines)**
3. **Data readout (16 DI lines)**
4. **Implementation of the VIPIC Virtual Counters in the FPGA memory (Counters are incremented of the value read from the chip until operation is stopped)**
5. **Generate 4 analog outputs for calibration amplitude and threshold voltage**

Real Time OS Tasks:

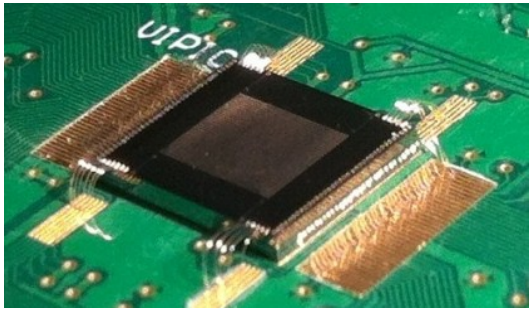
1. **Load Data to be send out to the chip**
2. **Set threshold voltage**
3. **Start FPGA operation**
4. **Read the Virtual Counters data summed in the e.g. 1 000 single readouts**
5. **Send the data to GUI over the TCPI / IP & save the data file**

NATIONAL INSTRUMENTS LabVIEW™ 2012

Performed tests (without detector)

1. Measured all bias currents for CSA, shaper and discriminator and reference current for trimming DACs
2. Measured overall power consumption in static and in operation
3. Tests of digital shift registers defining configuration of a pixel (pixel SET, Pixel RESET, reset, pixel SETTING)
4. tests of the whole digital readout chain (pixel 1-stage pipeline logic, sparsifier: 8 bit priority encoder, pixel readout selector, serializer, level adapters, LVDS drivers)
5. Readout chain including analog in acquisition of noise hits (dead-timeless operation with alternating counters)
6. Discriminator threshold scan with noise counts (full readout)
7. Tests of whole readout chain with internal calibration

Performed tests (3 operational chips out of 5 bonded)



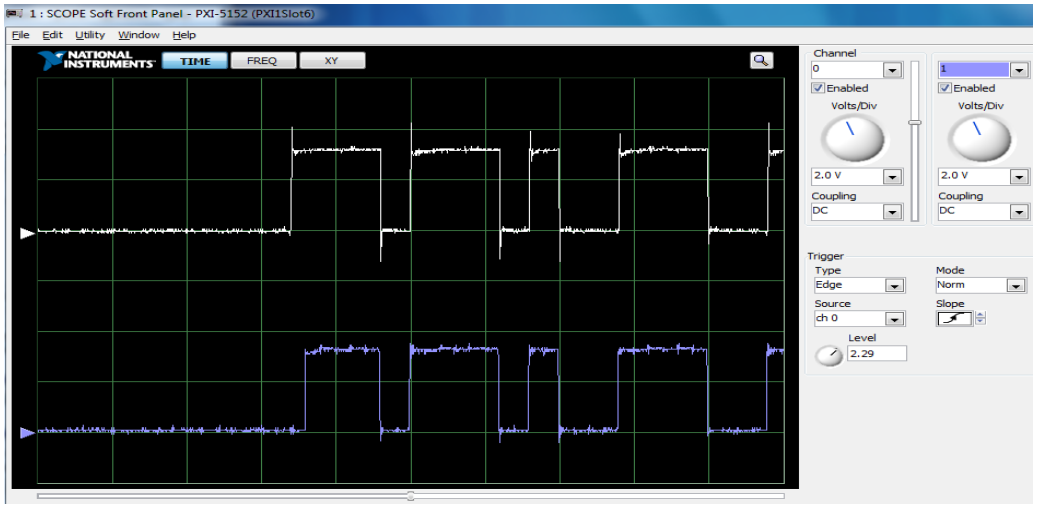
1. Power consumption and reference currents

Refrence analog currents (according to spec ~2%):

Reference line	Voltage	Current	Current (simulat.)
Vfed	830mV	7.16uA	7.2uA
Vcas	420mV	31.8uA	32uA
Vsh	680mV	14uA	14.2uA
Vdis	470mV	28.5uA	28.8uA
Vdac	760mV	9.82uA	10uA

Power consumption according to specification (no 3D influence on process values = expected from 2D processing)

2. Testing digital shift registers (communication to digital layer via analog layer)



Configuration Register Tests

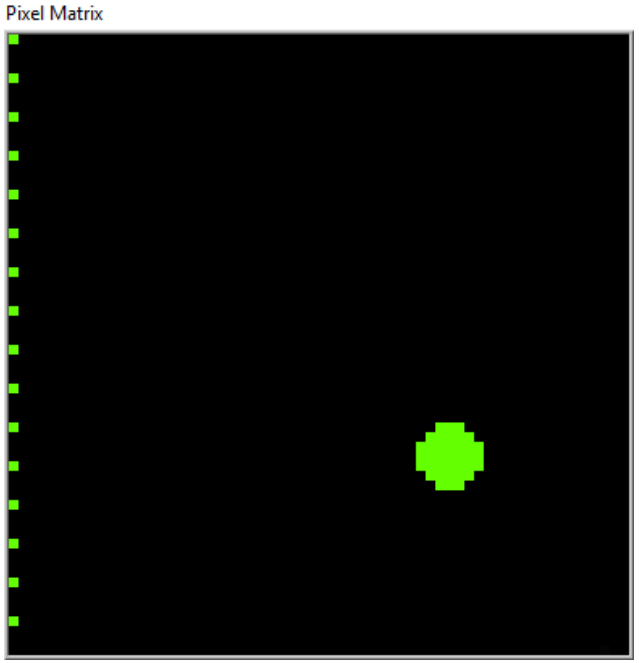
1. **Function of pixel SET is to make pixel acting hit permanently and feeding into the readout**
2. **All or certain pixels can be set for always being read out (feasible ROI)**
3. **Function of pixel RESET is to make pixel never allowed to feed into sparsifier**
4. **All or certain pixels can be disabled**

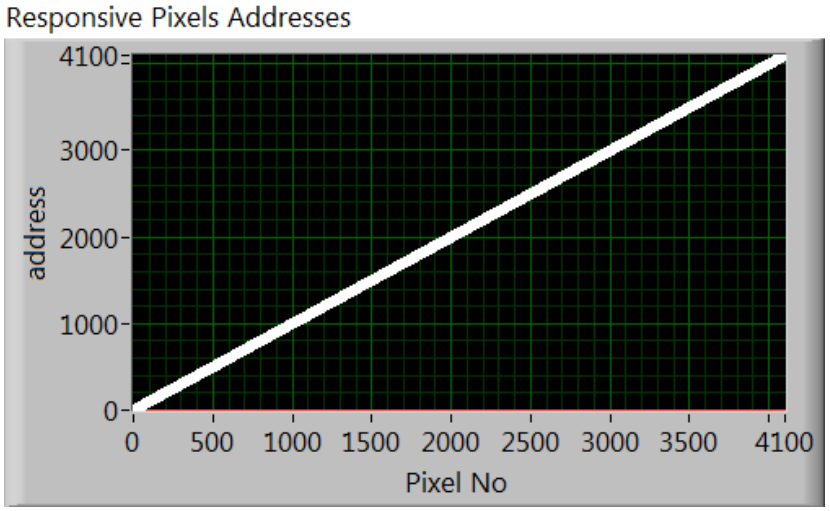
5. **Pixel SET and pixel RESET with 1-stage pipeline pixel logic work!**

1. **Pixels that were SET yield always addresses in the readout but their counter content depends if they were having noise or calibration hits**

pixel SET and pixel RESETproper operations on all bonded chips

Example of SET pattern





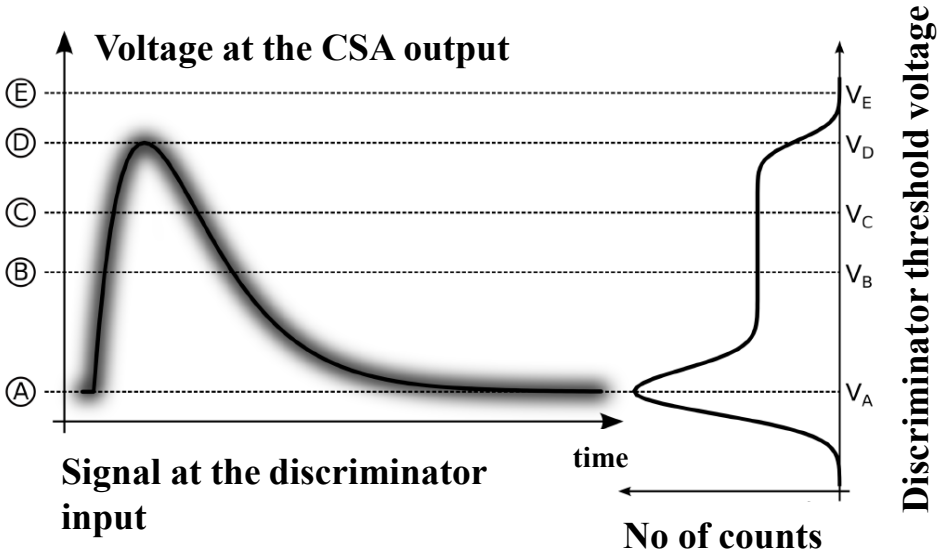
Threshold scan around the discriminator DC level and noise counts

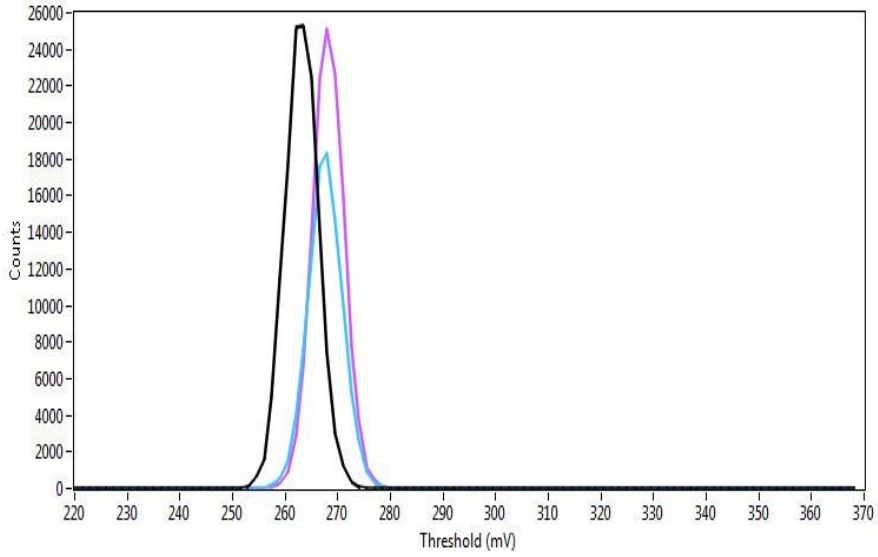
1. Single exposition time is equal 32 us (speed - analog limited). In this time we are able to count up to 32 counts from X-ray source/calibration/noise

2. To obtain higher statistic of noise we repeat the single step with certain threshold 1000 times and after each exposition (32 us) we add the counters' data together

3. Example of noise counts for 3 pixels is shown below

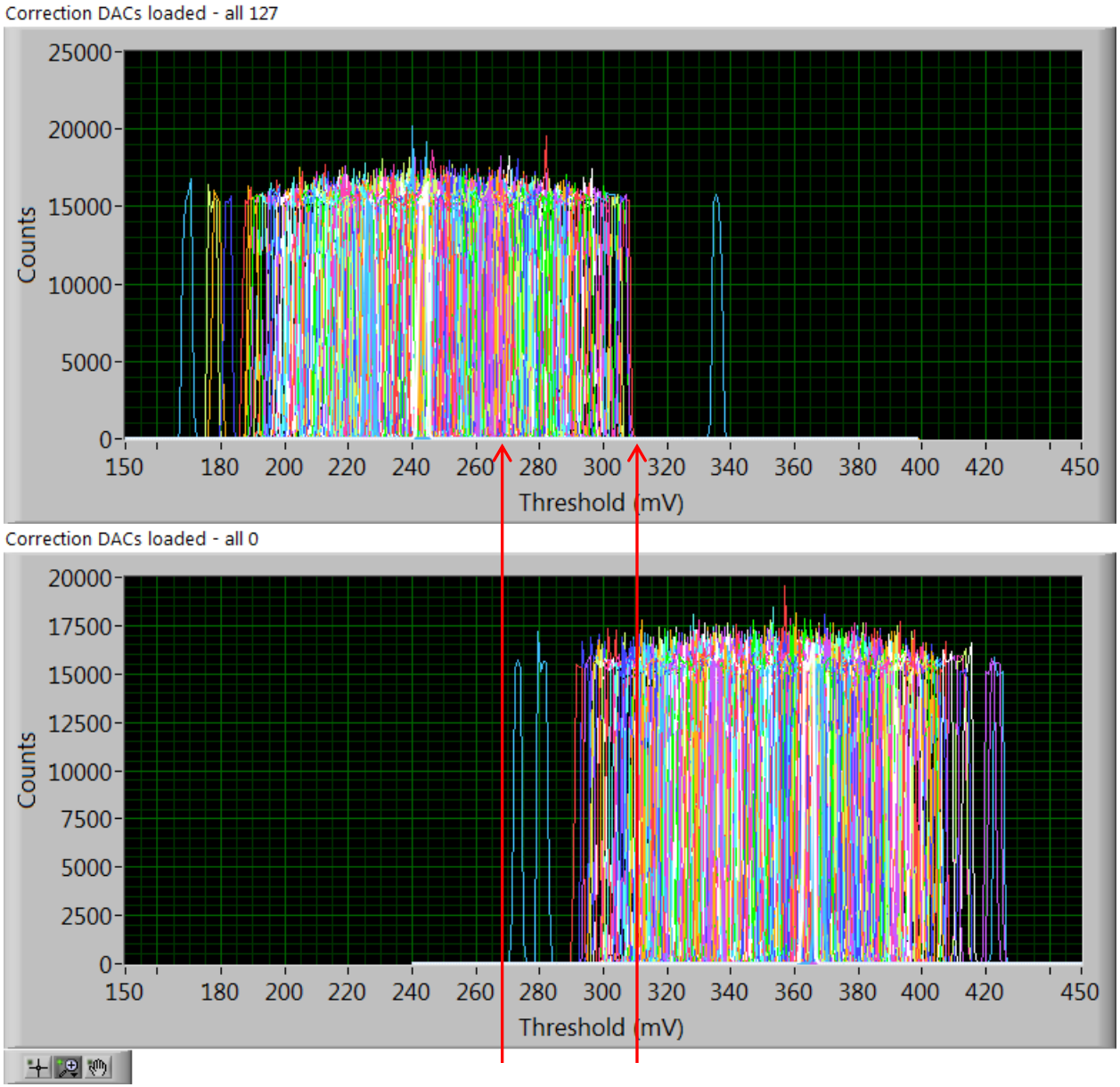
Remember: all results readout through whole sparsifier





two unambiguously resolving groups resulted from noise hits at extreme DAC settings

All pixels responds



Communication between tiers does not show any misses

Analog Part Tests
Calibration Pulses

1. During each exposure time the amount of 10 calibration pulses is sent to the analog front end.

2. Pulses with three different amplitudes

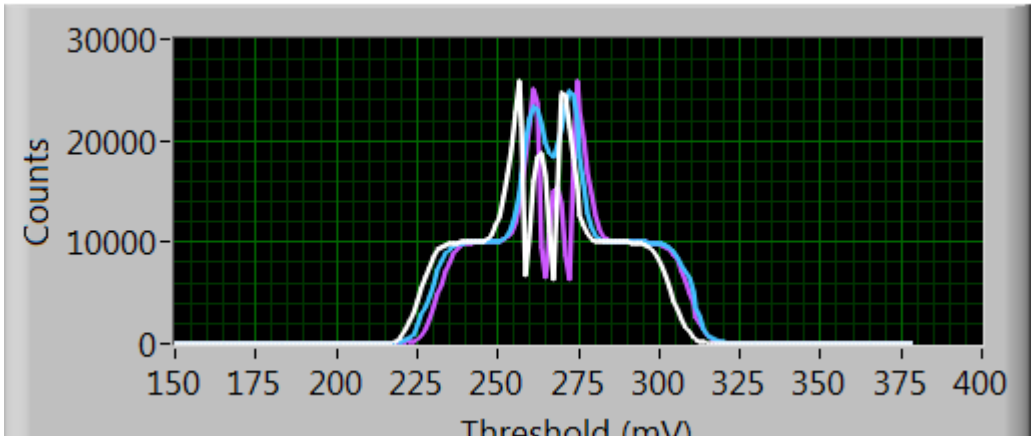
Currently calibration pulses sent simultaneously to all pixels

Gain ≈ 40 uV/el (injection capacitor only 1.7fF)

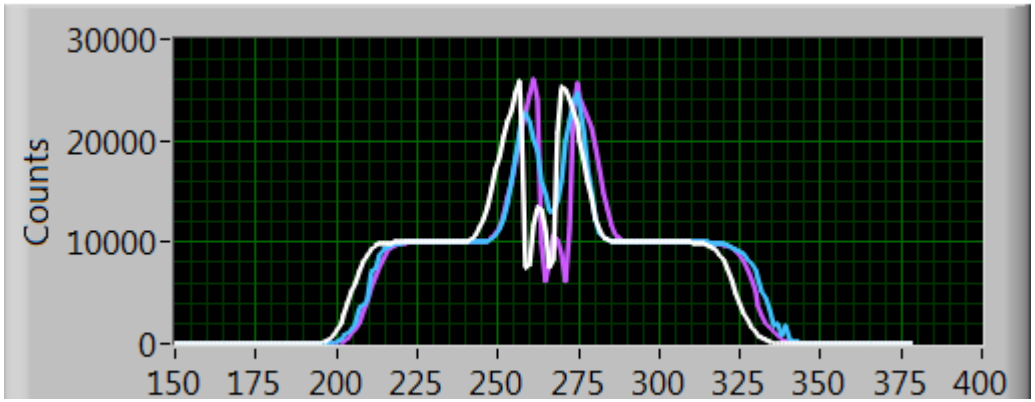
ENC ≈ 75 el. Rms

Values are close to expected

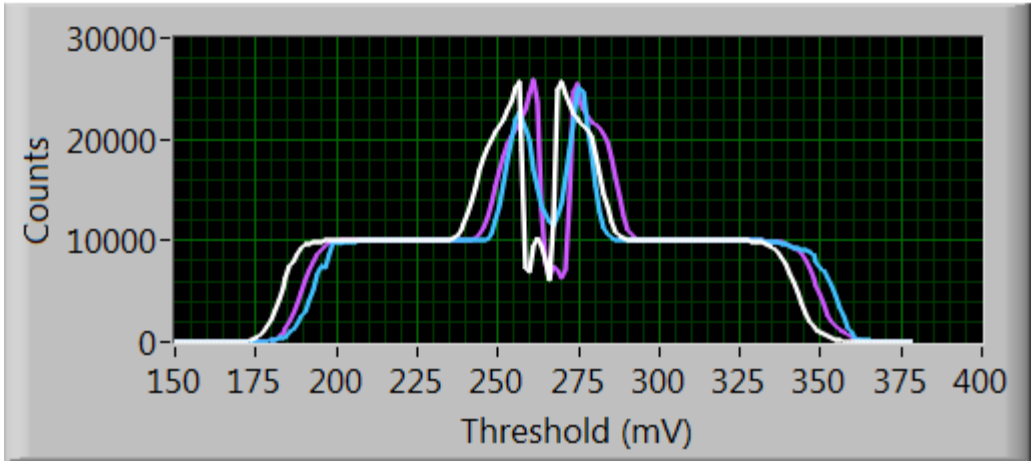
Qin = 1 000el



Qin = 1 500el



Qin = 2 000el



Conclusions

1. **3D fabrication demonstrated:**
    1. **Chip is functional (no shorts, no missing connections on the bonding interface)**
    2. **2-tier chip behaves like a standard 2D device (all signals , power supplies, biases make connections between tiers)**

2. **Full functionality demonstration still underway, but majority shows satisfactory operation of the device**
    1. **Tests of all item yielded positive results**
    2. **The "bumper-to-bumper" (from the detector pad, through the sparsifier to the readout pad) functionality of the whole chain has been shown!**
    3. **Chip works in both operation modes: timing and counting**
    4. **One problem experienced with pixel SETTING shift register – is being investigated**

3. **Next tests and steps:**
    1. **Tests of pixel to pixel uniformity and adjustment of trimming DACs**
    2. **Need more chips statistics (expected soon from new wafers) and assembly with a test detector using Au stud-bonding and later using DBI bonding to a dedicated sensor from BNL**

Acknowledgements

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