Fabrication and simulation of Novel Ultra Thin 3D Silicon Detector – Plasma Diagnostics for JET and ITER TOKAMAKS

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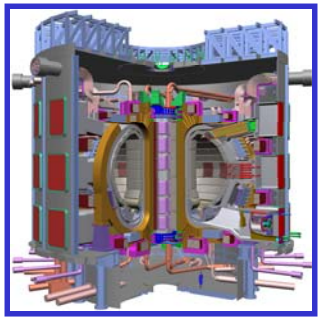
Outline

- Applications
- New detector concept
- Simulation results
- Fabrication technology
- Conclusions

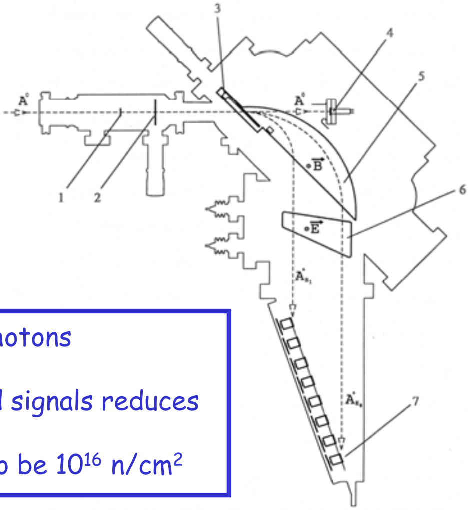
Applications



Corpuscular Diagnostics Plasma:

Neutral Particle Analyzers - NPAs

This new detectors where developed to cope with the increasing of the plasma burning power which roses the neutron and gamma background in such a way that detectors cannot cope with the particles’ rate. Therefore detectors get saturated and are not able to detect ions from the plasma, which carry information about the plasma parameters.



Neutral Particle Beam

- →Sensitivity is mainly to photons
- →Max. Count rate 100kHz
- →Pile-up of the background signals reduces S/N ratio
- →Radiation Hardness has to be 10^{16} n/cm^2

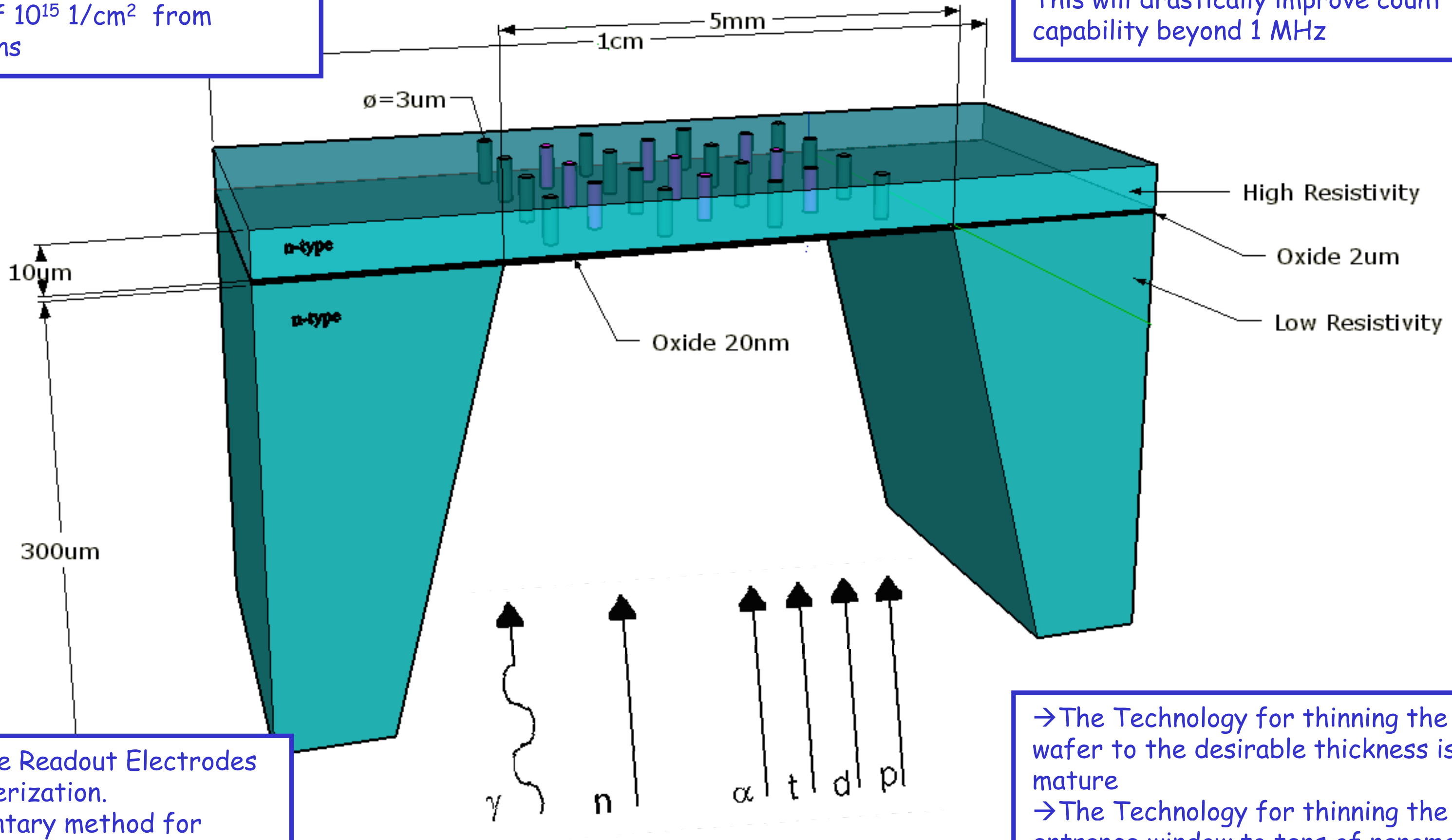
ITER (International Thermonuclear Experimental Reactor) should produce more power than it consumes. This is expressed in the value of Q, which represents the amount of thermal energy that is generated by the fusion reactions, divided by the amount of external heating. A value of Q smaller than 1 means that more power is needed to heat the plasma than is generated by fusion. In the "burning plasma", most of the plasma heating has to be come from the fusion reactions themselves.

Other applications: neutron dosimetry and imaging

New Detector Concept

→Silicon detectors with 3D electrodes are intrinsically Radiation Hard.
Test shows 3D silicon detectors withstand radiation damage of 10^{15} 1/cm^2 from neutrons and protons

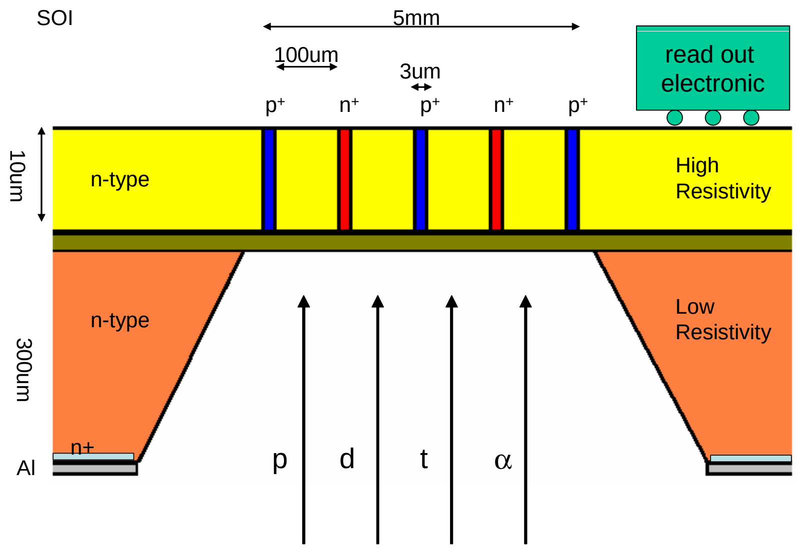
→Time Collection Charge of the order of tens of nanoseconds.
This will drastically improve count rate capability beyond 1 MHz

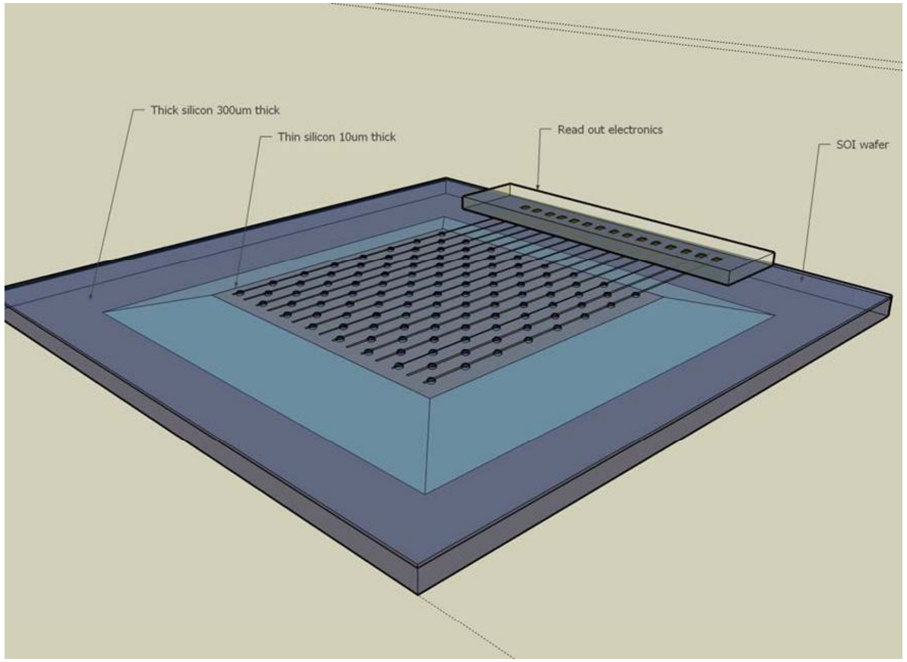


→Granularity of the Readout Electrodes will facilitate clusterization.
This is a complementary method for background rejection.

→The Technology for thinning the Silicon wafer to the desirable thickness is mature
→The Technology for thinning the entrance window to tens of nanometers was already successfully tested

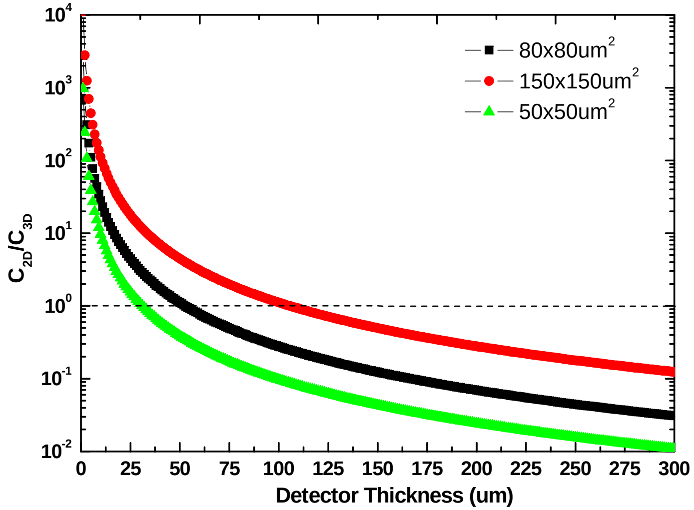
Schematic structure

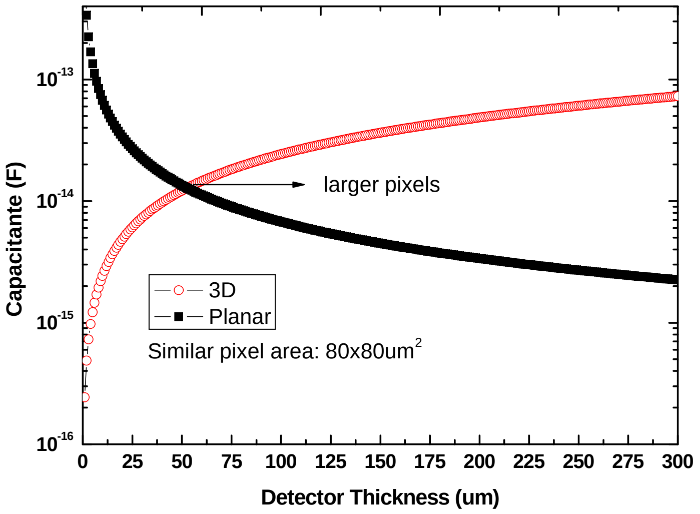




Strip configuration is ok, pixels are also possible

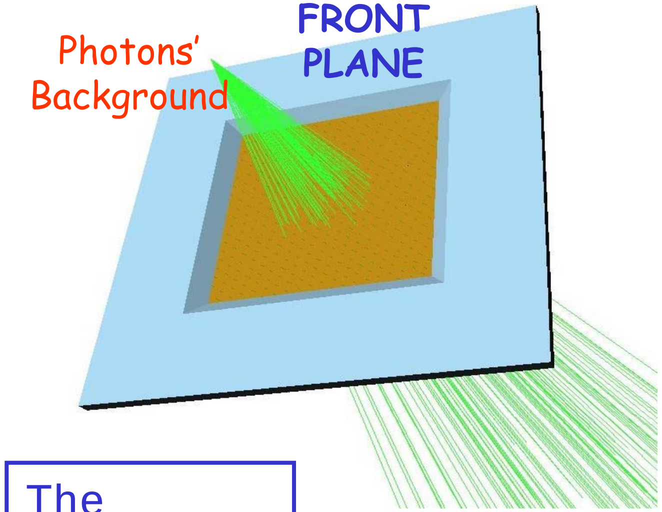
Advantages of 3D thin





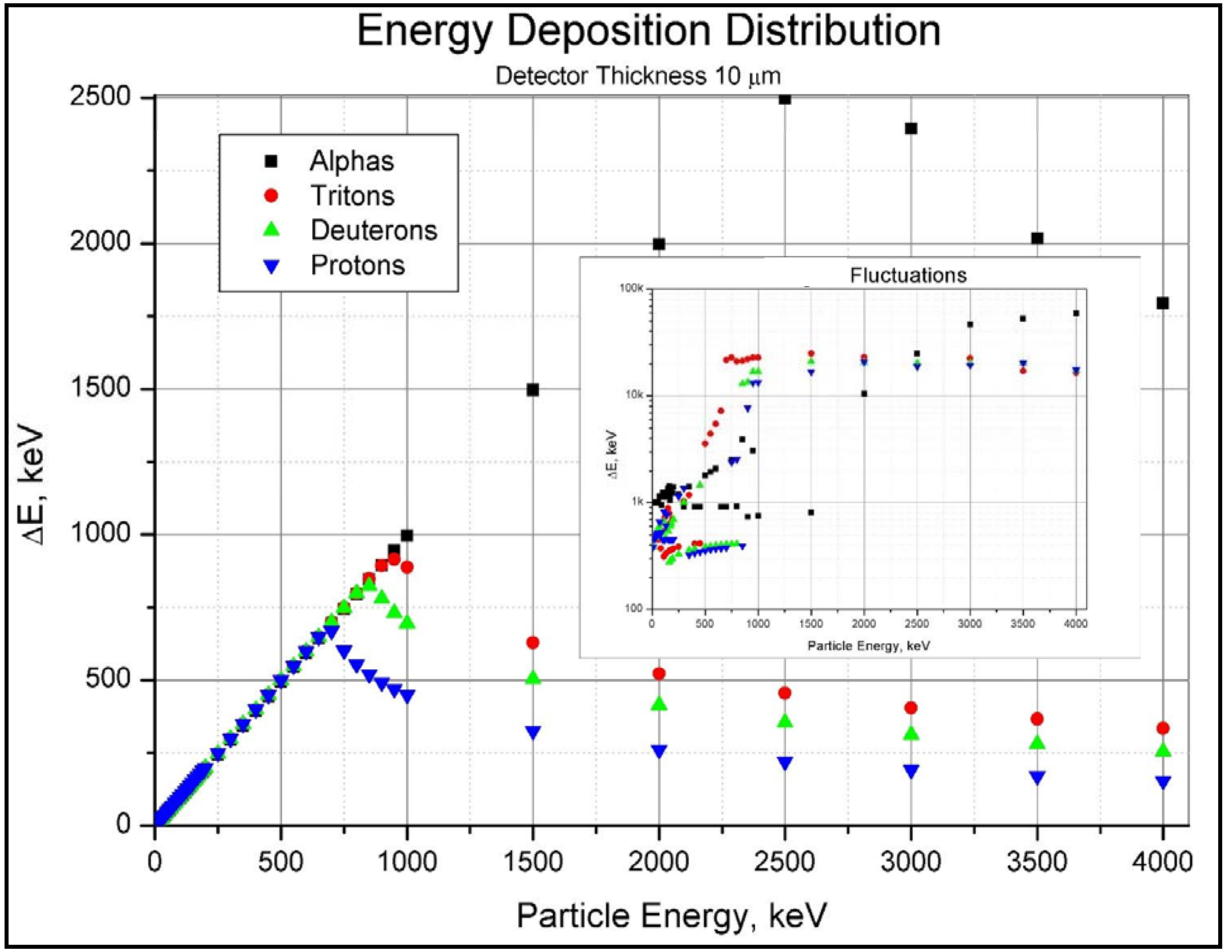
- •Keep low depletion voltage without increasing depletion capacitance.
- •Reduce stopping layer in the entrance window.
- •Increase breakdown voltage in order to withstand radiation damage.
- •Reduce contribution from background signal

Geant4 Simulation



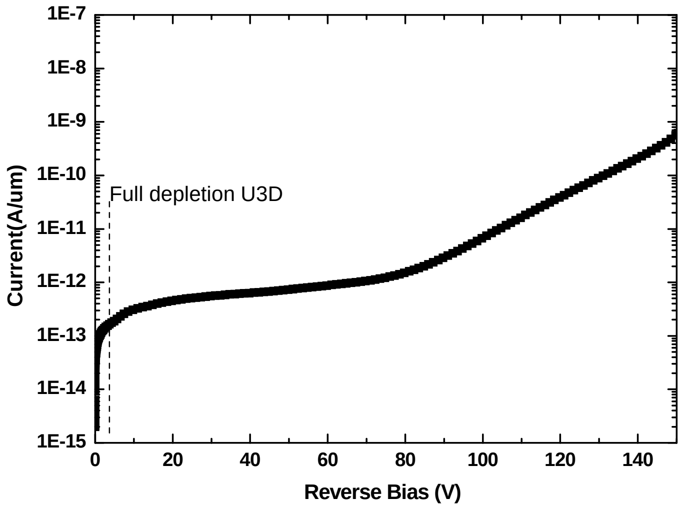
The Integral Sensitivity will be of the order of 10^{-6} or even smaller

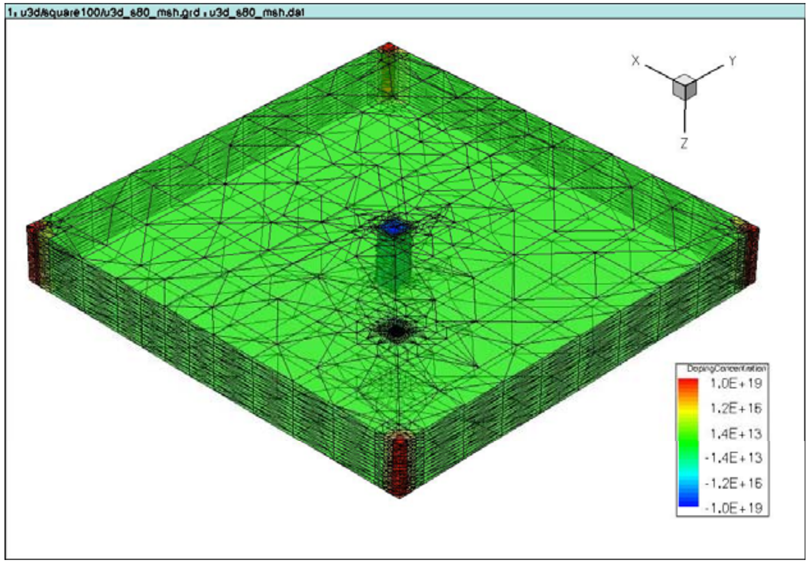
Strips:
pitch 80 um
width 20 um



F. Garcia et al, Novel Ultra Thin 3D Silicon Detector – Plasma Diagnostics for JET and ITER TOKAMAKS, presented at the 10th International Workshop on Radiation Imaging Detectors in Helsinki, Finland, June 29 - July 3, 2008.

Sentaurus Simulation

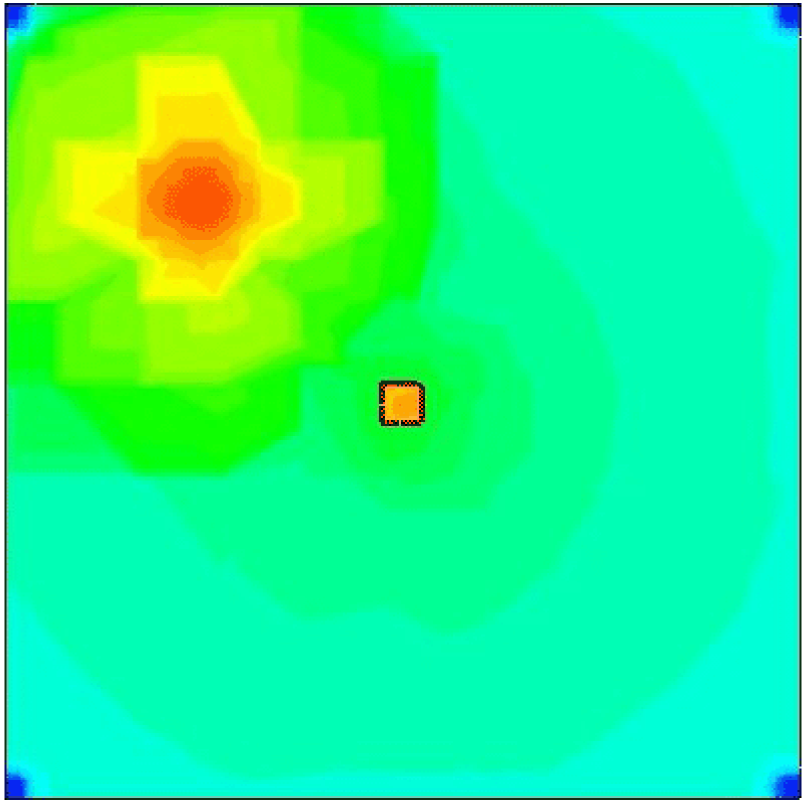




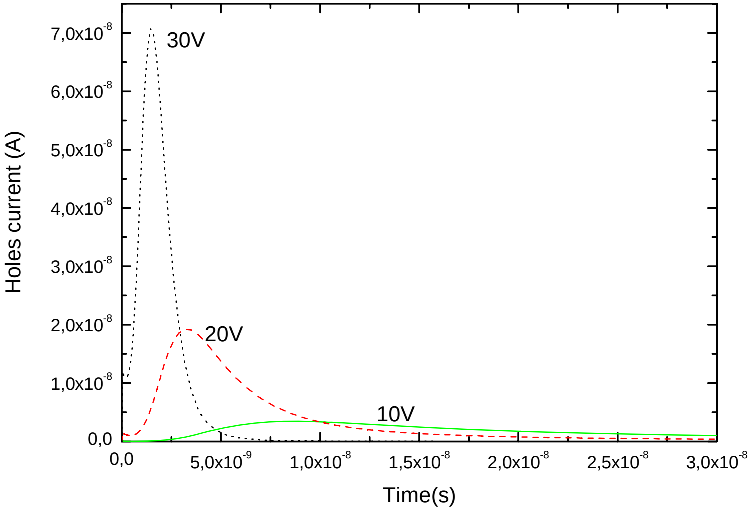
- Square pitch: 80um
- Silicon substrate: n-type 10^{12}cm^{-3}
- Holes collection at p+ electrode
- Detector thickness 10um
- Oxide charge 10^{11}cm^{-2}

- Charge carriers swept horizontally towards the electrodes
- Low full depletion: 3.5V
- Short collection time: peak at 2.1ns

Sentaurus Simulation

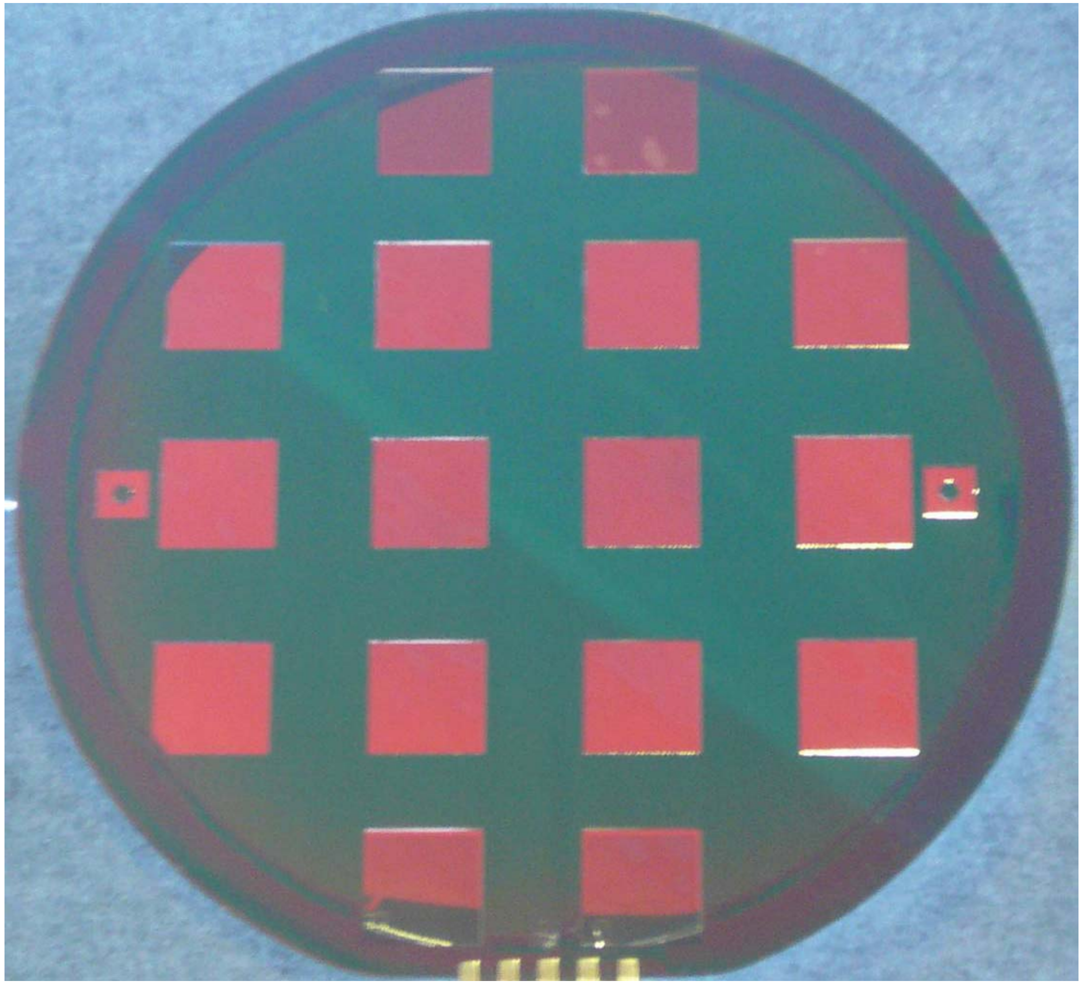


Charges collected in the central electrode



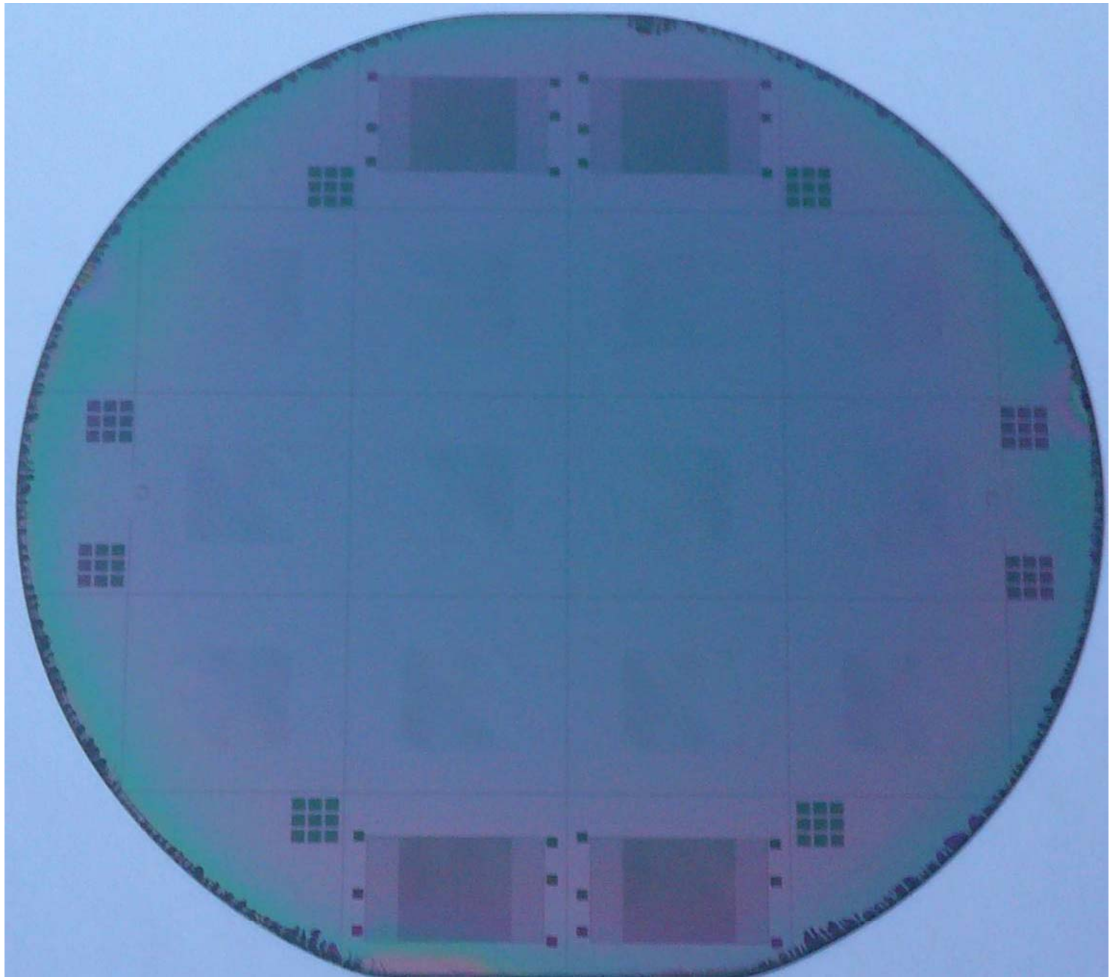
Charge collected at different bias volts.
At 10V the signal peaks at 10ns but at
30V the peak is at 1ns.

Fabrication



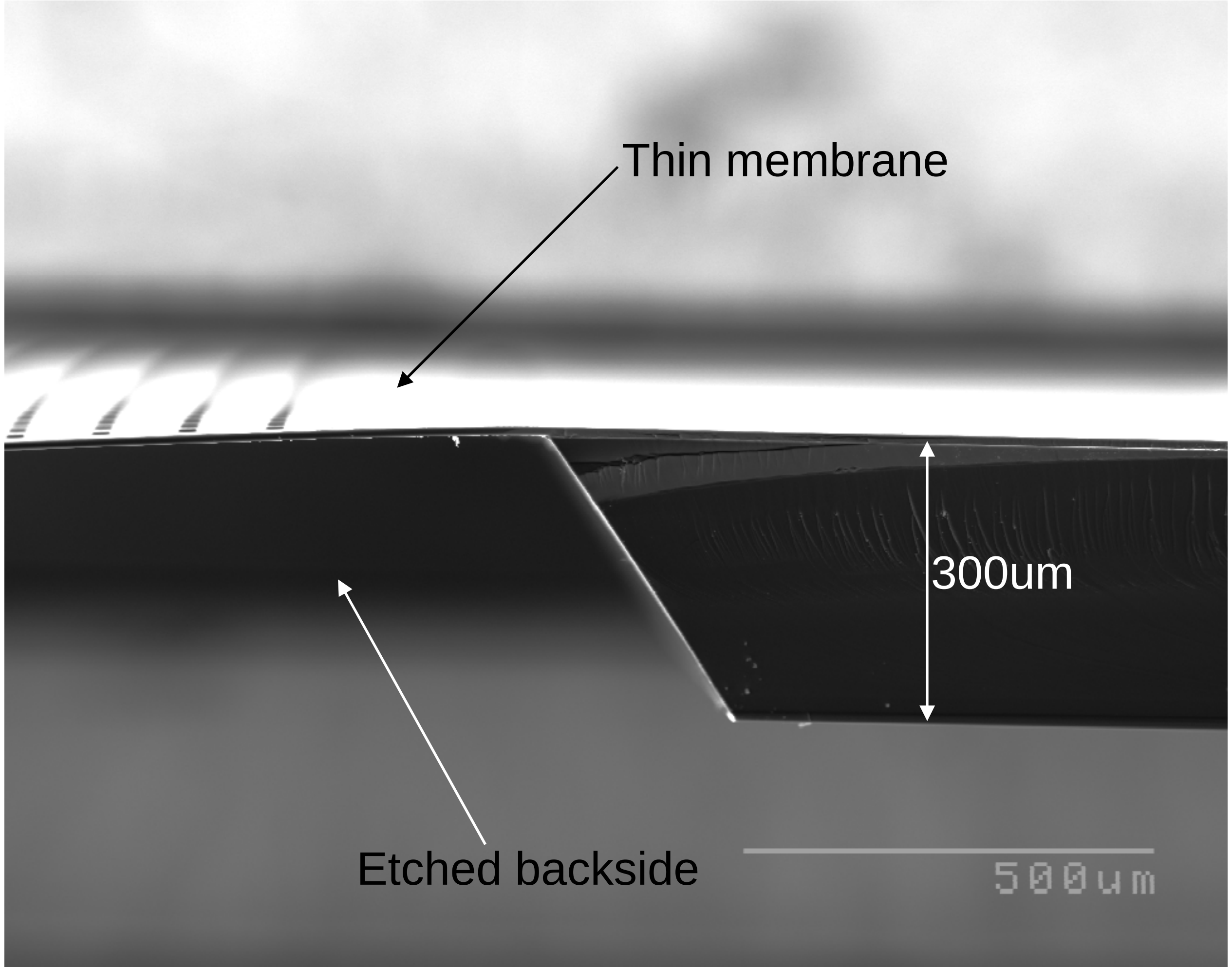
Finished wafer with back illumination. Back view.
This is a test detector with only p-type polysilicon and no metal.
The red squares are the thin (10µm) membranes with 5µm holes

Front view

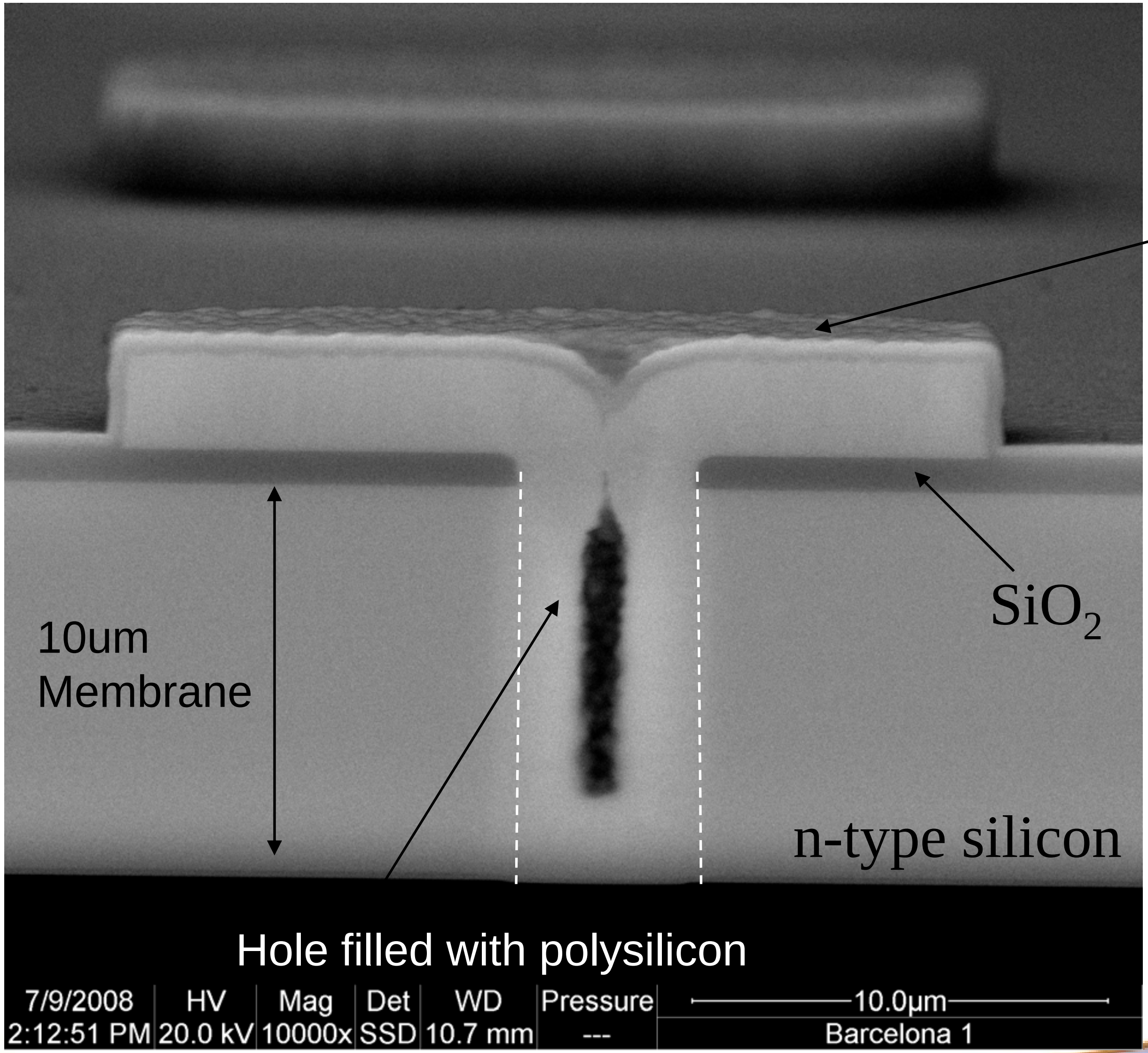


Finished wafer with front illumination. Top view.

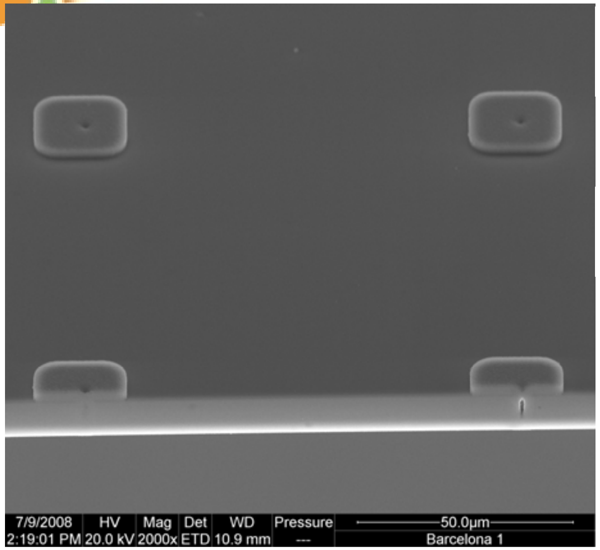
Membrane



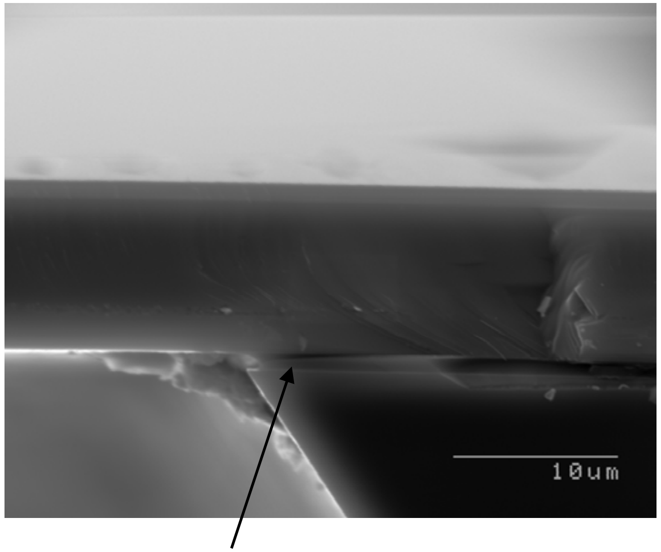
Cross section



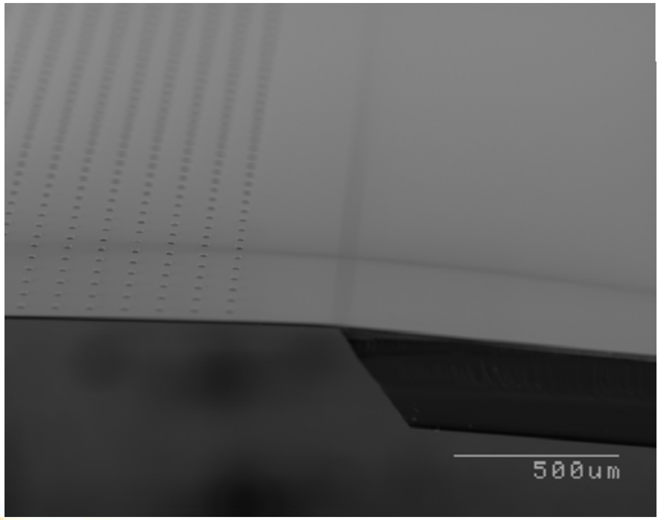
Cross sections



Detail of the surface

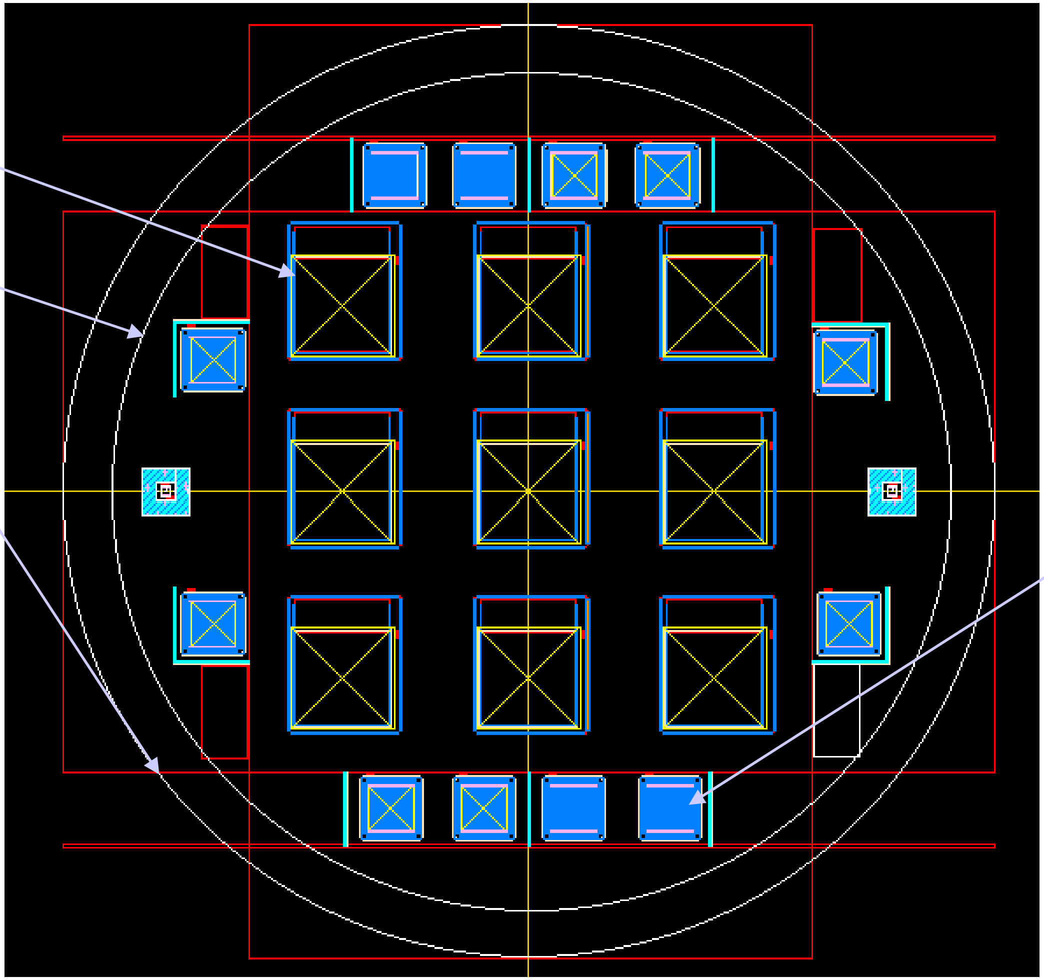


Oxide of the SOI wafer



First fabrication test run demonstrated the feasibility of the process.
A new mask set with 3D-thin detectors and test structures has been designed and the detectors are being fabricated at CNM clean room facilities.

Mask layout



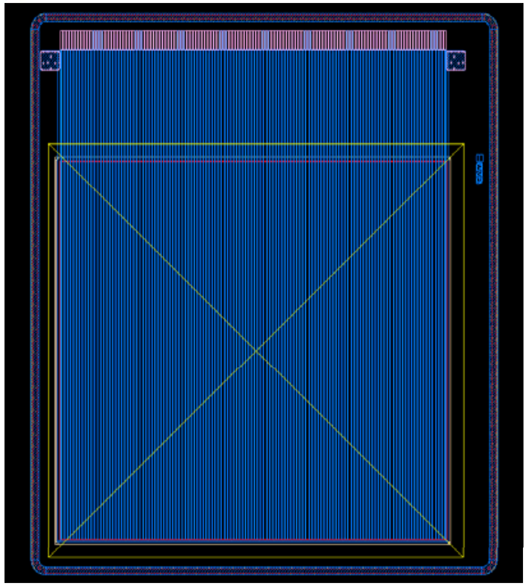
3d-thin (9)

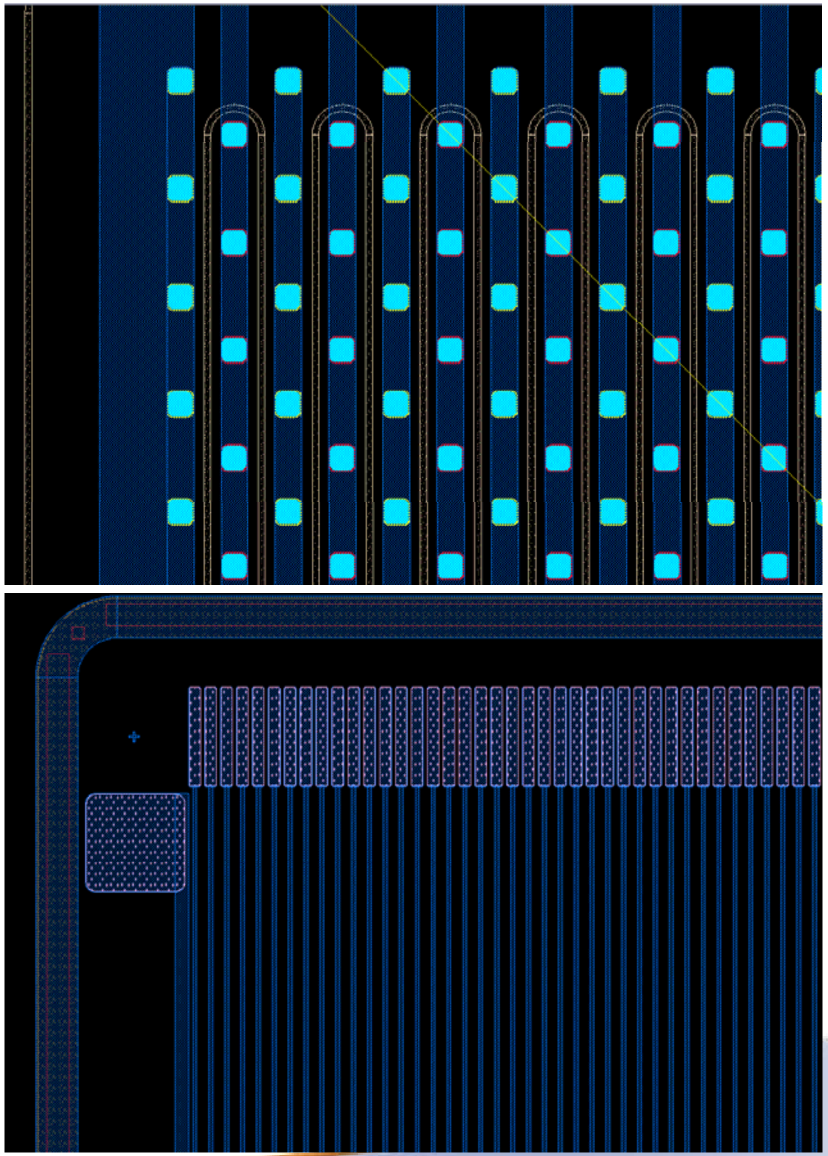
Pad conf. thin (8)

Test structures (4)

Pad conf thick (4)

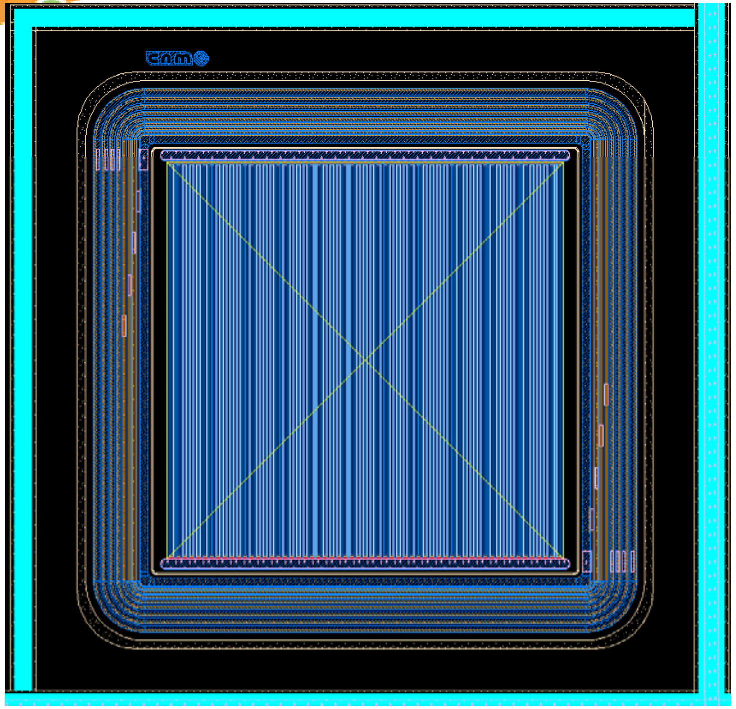
Strips

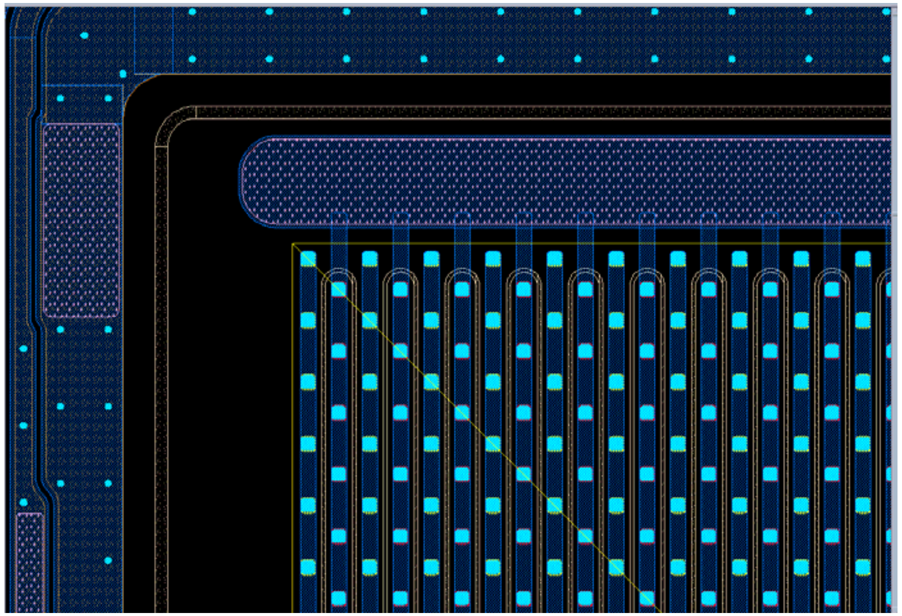




- •DC coupled
- •128 channels
- •80 um pitch
- •5um holes
- •10um thick
- •Area=1cm^2
- •p-n or n-p configuration (p-stop isolation)
- •Oxide thickness (variable).

Pad





- •Only one channel.
- •All strips of the same type shorted to the same electrode.
- •10 um thick
- •Oxide thickness (different values).
- •Area= 0.5x0.5 cm^2
- •80um pitch
- •5um holes

Conclusions

- The concept has been tested and fabrication has been performed.
- Simulation shows full depletion of 3.5V and breakdown voltage of 150V.
- Signal collection time is on the order of 1 ns at 30V biasing.
- Detector capacitance for a single cell of the U3DTHIN two orders of magnitude smaller than planar one with the same thickness.
- First complete fabrication run finished, to be tested.