Monolithic Pixel Sensors in Deep-Submicron SOI Technology

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Outline

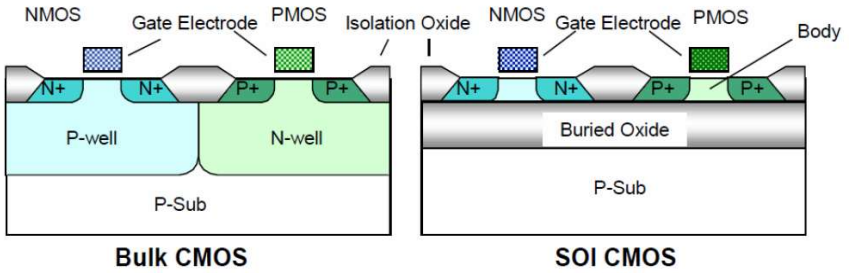
- Introduction on SOI technology: from commercial applications to radiation sensors
- OKI fully-depleted SOI-CMOS fabrication process
- Prototype chips design and testing at LBNL
- Experimental results: beam test and radiation tests
- Summary and Outlook

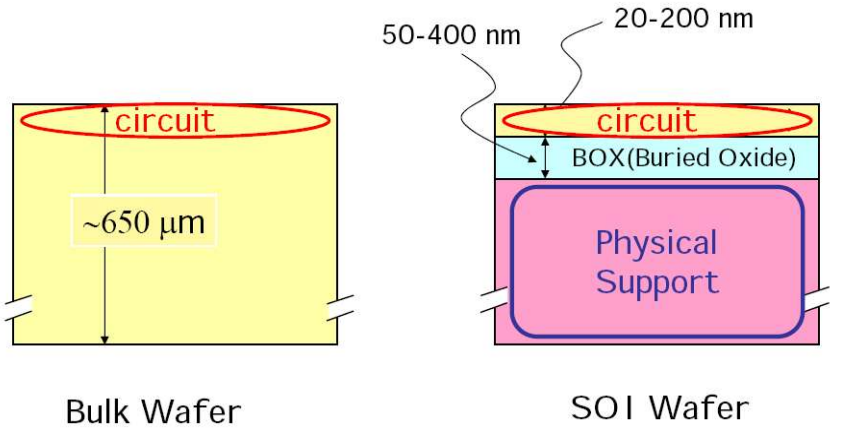
Silicon-On-Insulator (SOI) technology

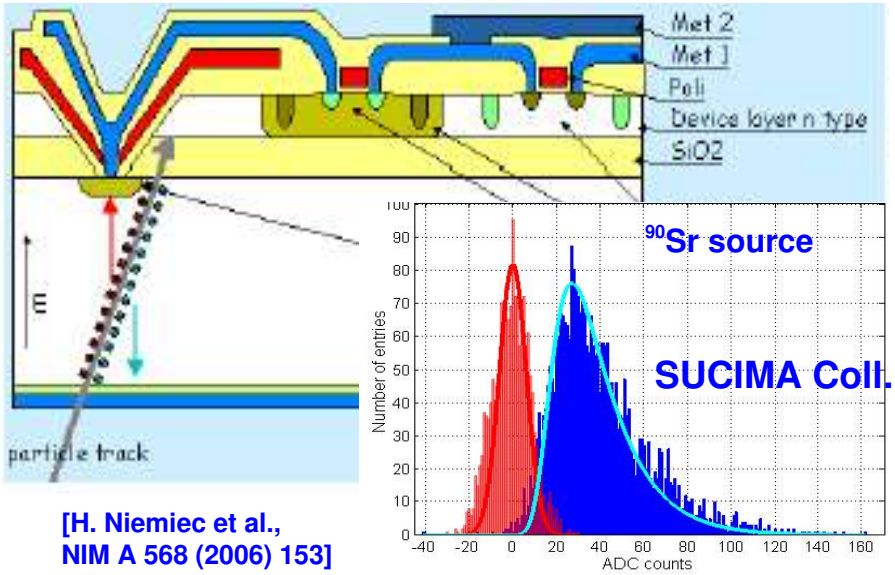
- CMOS electronics implanted on a thin silicon layer on top of a buried oxide (BOX): ensures full dielectric isolation, small active volume and low-junction capacitance

- Latch-up and soft-error immunity, low threshold, low noise: technology widely employed in high-speed and low power applications, e.g. microprocessors and portable electronics

- Radiation sensors can be built by using a high-resistivity substrate and providing a technology to interconnect the substrate through the BOX





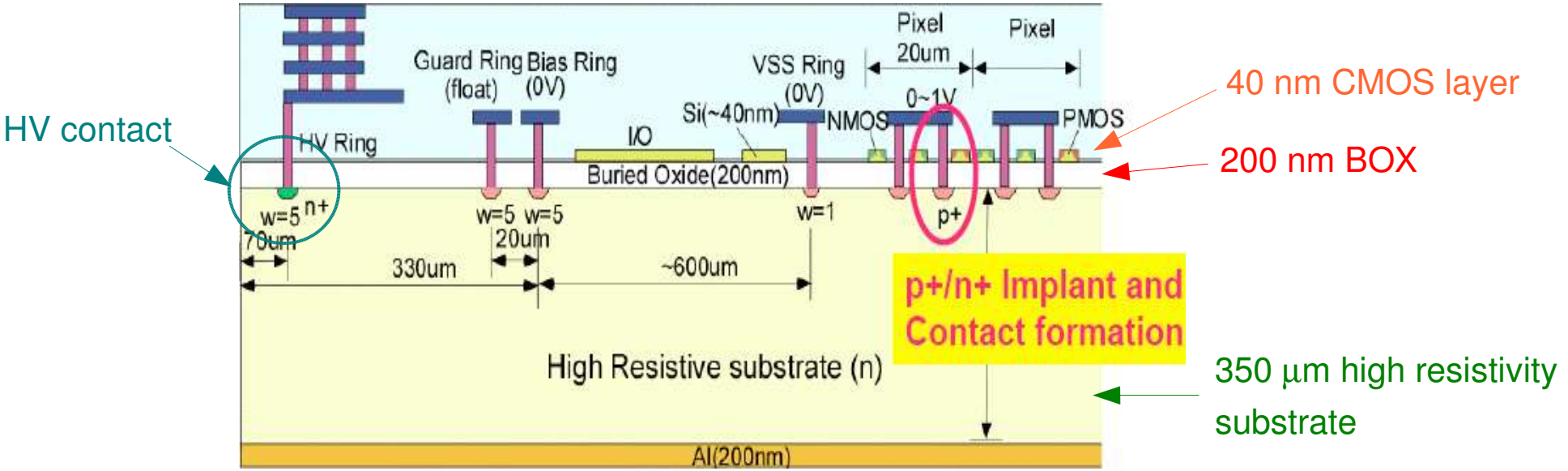


[H. Niemiec et al., NIM A 568 (2006) 153]

- First attempt from SUCIMA collaboration in a 3 µm process from IET, Poland, though not compatible with standard CMOS processes

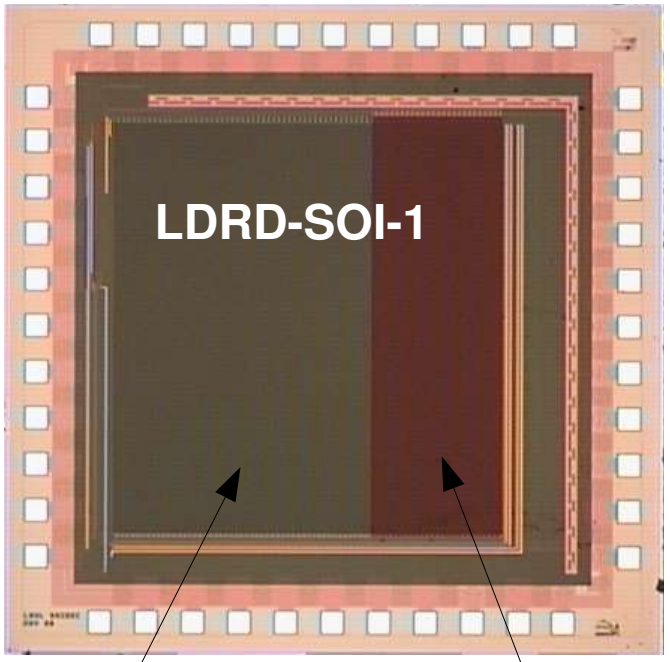
- Depletion of substrate via p-n junction implanted through BOX and fully-integrated readout logic on top
→ SOI monolithic pixel sensor

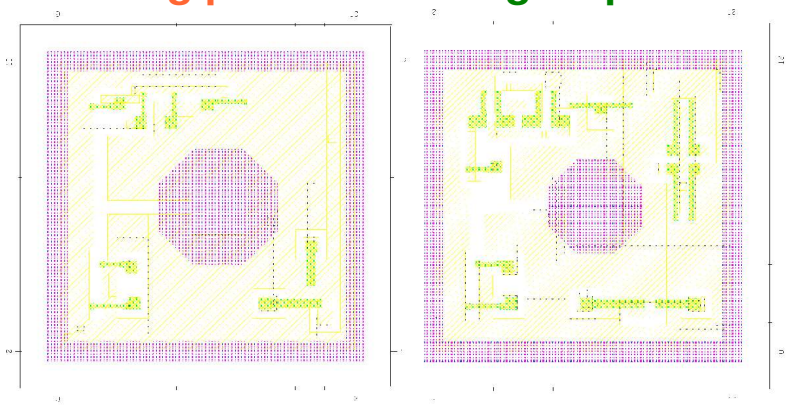
OKI Fully-Depleted SOI process



- Novel 0.15 µm Fully-Depleted (FD) SOI process from OKI Ltd., Japan
- 350 µm thick substrate, high-resistivity (700 Ω·cm): can be contacted through the 200 nm buried oxide for pixel implant formation and high voltage (HV) contact for substrate reverse bias
- 40 nm thin CMOS layer, fully depleted at operational voltages (low threshold, low power)
- Back-plane plated with 200 nm Al layer to allow biasing from the back
- Functionality demonstrated by prototype chip from KEK in '06; two subsequent runs in 2007 and 2008 involving submission from Japan and US institutes (LBNL, FNAL, U Hawaii)

LBNL SOI prototype in 0.15 μm process

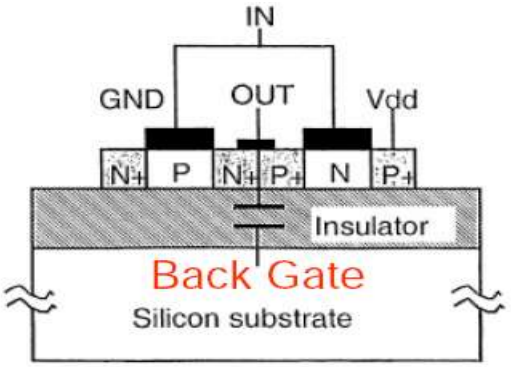


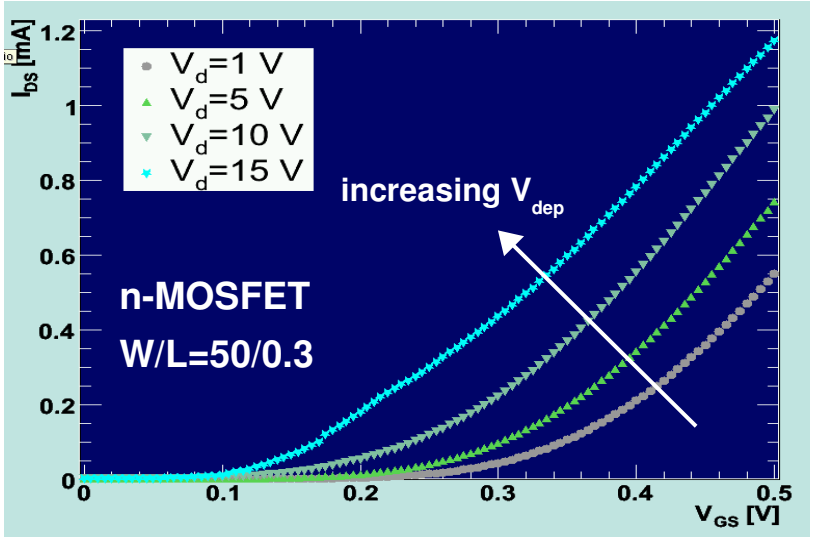


LDRD-SOI-1 (2007)

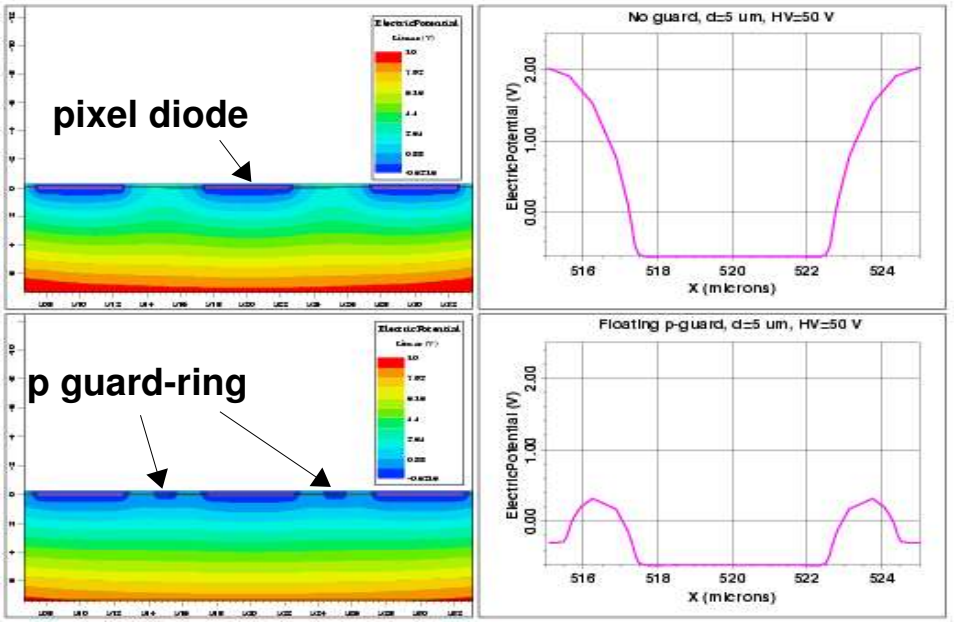
- OKI 0.15 μm FD-SOI process
- Pilot run, not optimized in terms of leakage current
- 350 μm thick substrate (n-type, 6×10^{12} cm^{-3}), 200 nm BOX, 40 nm thin CMOS layer
- 160x150 pixels, 10x10 μm^2 pixels
- Floating p-type guard-ring around each pixel
- Choice of substrate contact and pixel layout justified by TCAD simulations
- 2 analog parts: 1.8 V and 1.0 V, simple 3T pixel architecture
- 1 digital part: in-pixel comparator and latch, no amplifier; adjustable threshold; 15 transistors/pixel
- Readout at 6.25 MHz, 1.3 ms integration time (analog pixels)
- Adjustable integration time for digital pixels

The back-gating effect





- The high field in the depleted substrate causes back-gating of the CMOS electronics on top of the BOX
- Test of single transistors vs depletion voltage: shift in the threshold voltage with increasing substrate voltage
- Significant effect observed in single transistor tests: expect analog section functional for $V_{dep} < 20$ V
- Synopsys TCAD simulations: pixel surface potential for different diode sizes and depletion voltages
- Floating p-guard structure around each pixel to keep potential low and limit back-gate effects on MOSFETs



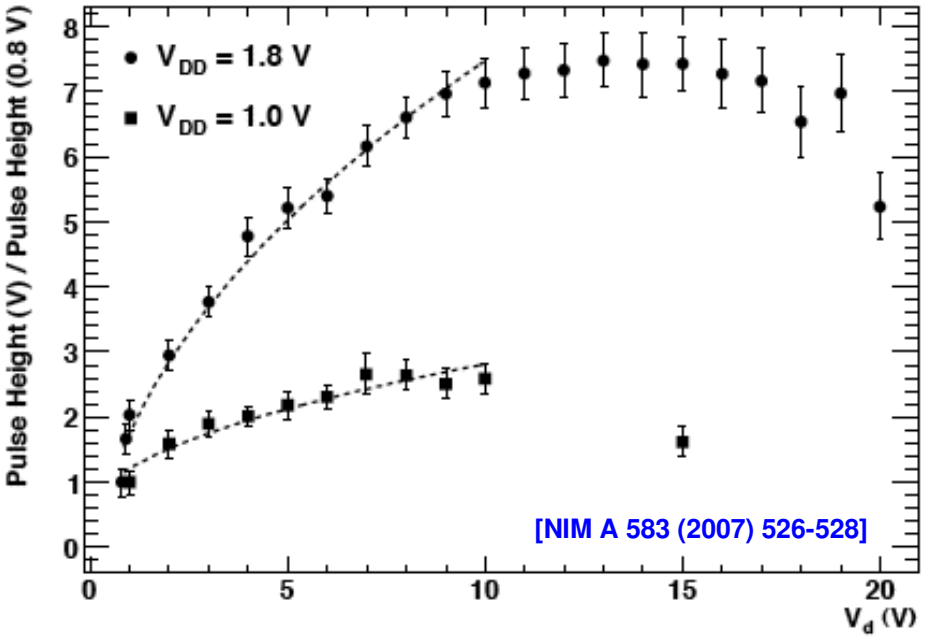
Tests with infrared laser

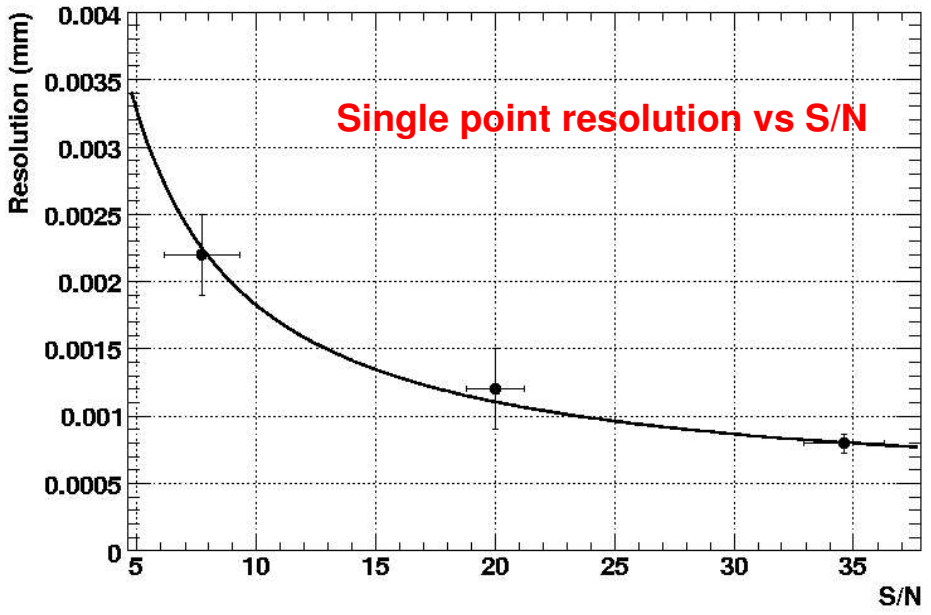
- Depletion region thickness vs substrate voltage measured with focused 1060 nm laser

- Expect signal proportional to depletion region thickness D and:

$$D \propto \sqrt{V_{dep}}$$

- Good agreement with expectation for $V_{dep} \leq 10V$ (D~45 μm), back-gating effects becoming significant for larger voltages





- Sensor spatial resolution studied by means of pixel scans performed on the analog pixels with 1060 nm laser focused to a 5 μm spot for different S/N values

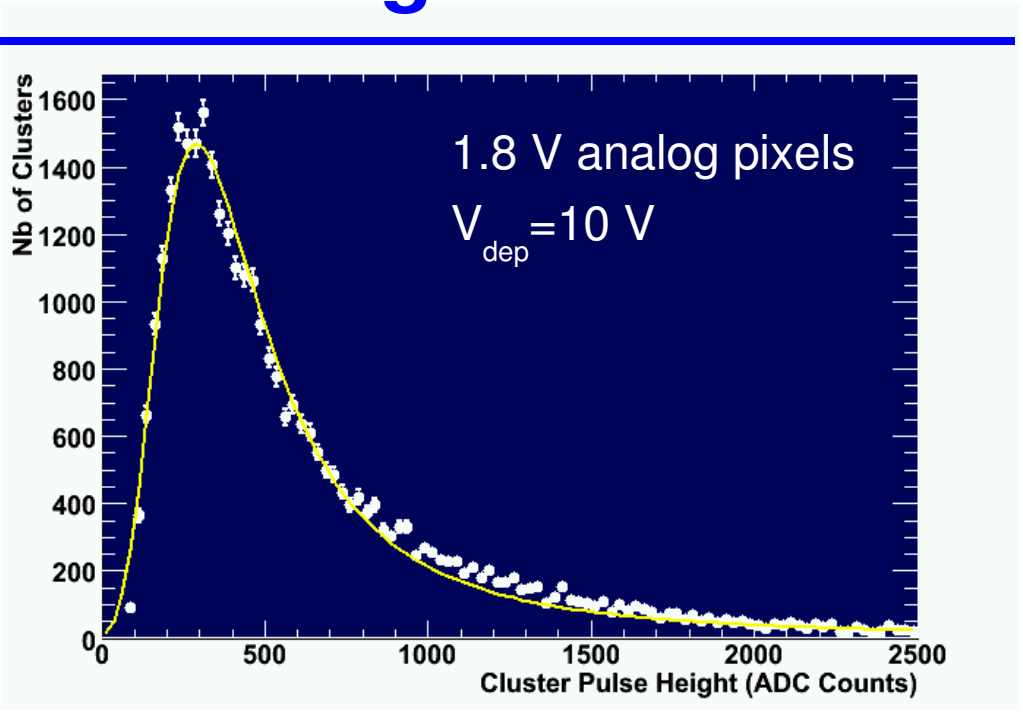
- With pixels of 10 μm pitch, 1 μm single point resolution is achievable for a S/N ratio of 20

Electron beam-test: analog sectors

- 1.35 GeV e^- beam extracted from the injection booster at the LBNL Advanced Light Source

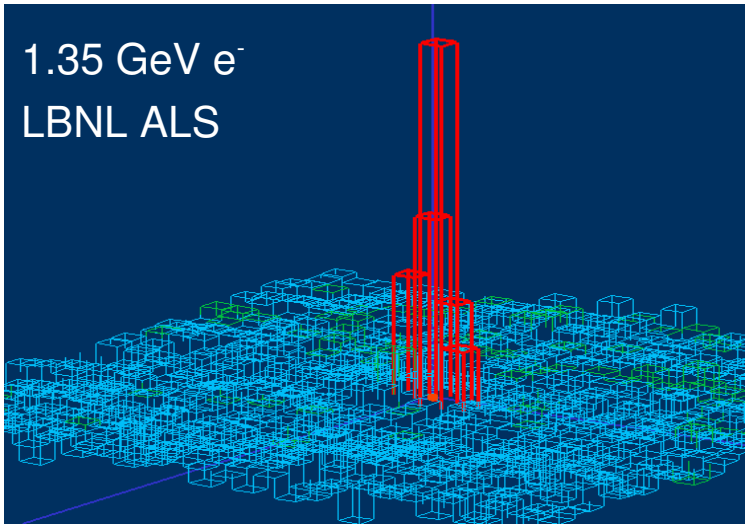
- First successful high momentum particle beam test on SOI monolithic pixel sensors

- As a function of the increasing V_{dep}: cluster pulse height increases and cluster multiplicity decreases, up to V_{dep}~10 V, consistent with lab tests and back-gating effects becoming important at V_{dep}=10 V



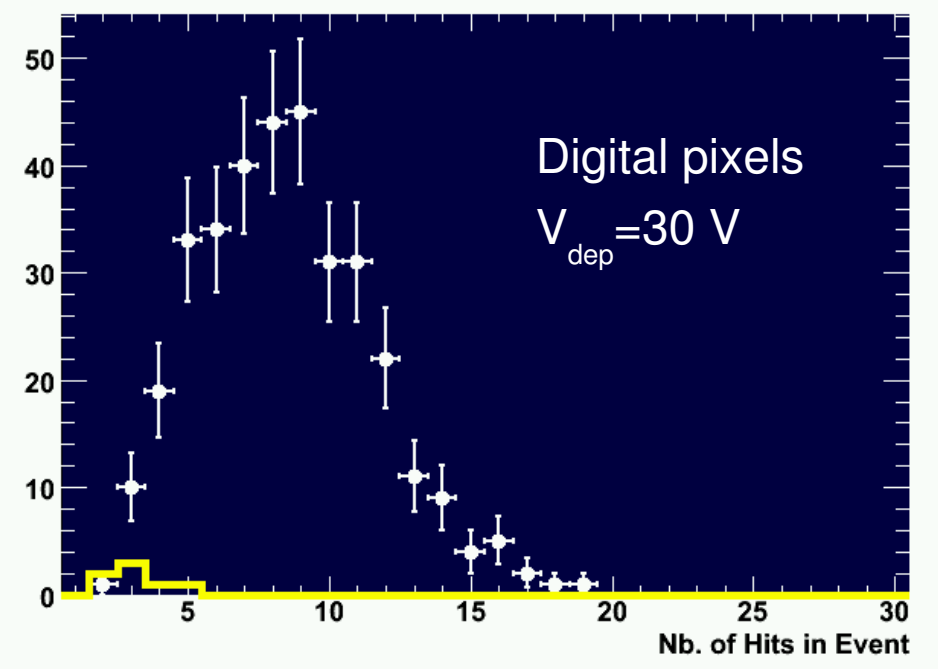
1.8 V Analog Pixels				
V_d (V)	Clusters / Spill (Beam on)	Clusters / Spill (Beam off)	Signal MPV (ADC Counts)	Average Signal/Noise
1	9.7	0.05	132	8.9
5	14.0	0.12	242	14.9
10	7.8	0.20	316	15.0
15	3.9	0.01	301	13.6

[NIM A 583 (2007) 526-528]

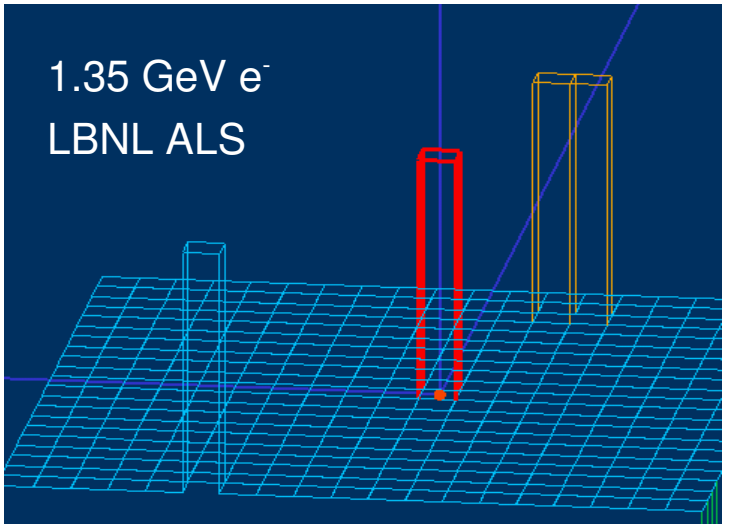


Electron beam-test: digital pixels

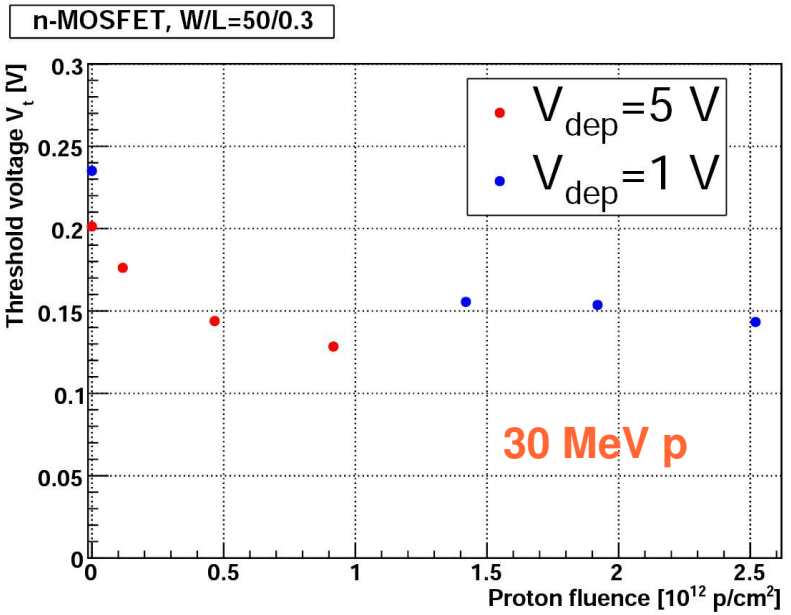
- Digital pixels: adjustable integration time allows to reduce problem of charge loss due to leakage current
- Control data sets without beam to estimate fake hits contribution
- Signal above threshold only at high substrate voltages:
  - analog threshold affected by back-gating
  - larger depletion → increased charge signal
  - at 25-30 V, these effects seem to combine for best detection capabilities
- Cluster multiplicity decreases with increasing V_{dep}

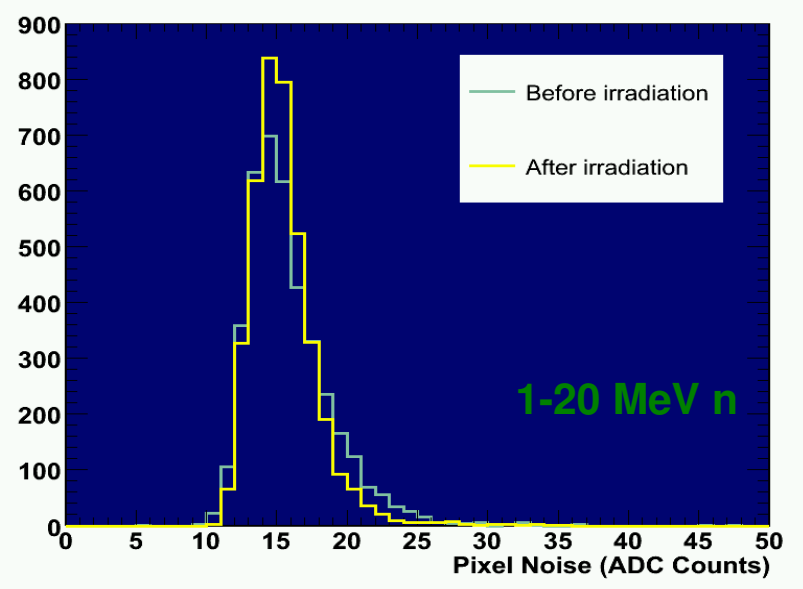


V_d (V)	Clusters/Evt w/ beam	Clusters/Evt w/o beam	<Nb Pixels>
20	3.62	0.04	1.78
25	5.81	0.04	1.32
30	8.31	0.04	1.26
35	1.60	0.01	1.14



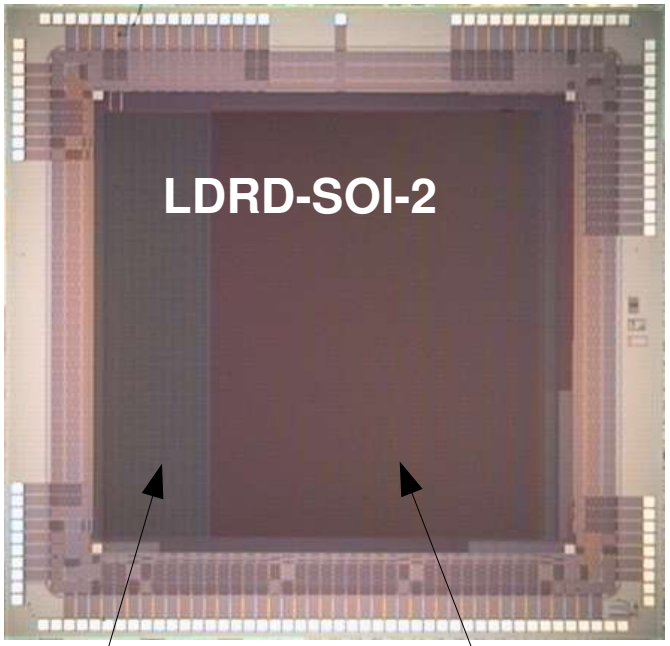
Irradiation tests





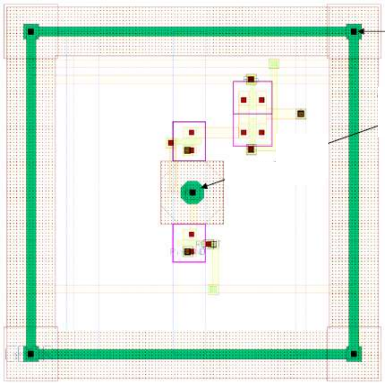
- Irradiations performed at LBNL 88" Cyclotron BASE Facility
- **30 MeV protons** up to an integrated fluence of 2.5 x 10^{12} p/cm^2 (~600 kRad)
  - Shift in transistor threshold voltages throughout irradiation
  - Charge trapping in BOX increases back-gating; contribution from charge trapped in thin MOSFET oxide negligible
- **1-20 MeV neutrons**: fluence up to 10^{11} n/cm^2
  - No change in transistor characteristics
  - Test of analog pixels shows no significant noise degradation

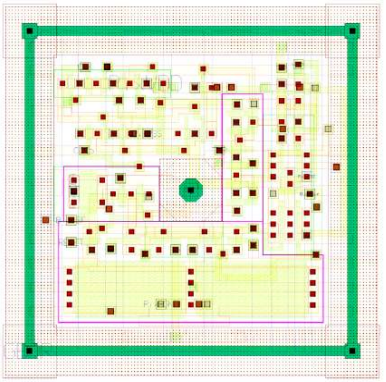
New prototype in 0.20 μm process



Analog pixels

Digital pixels



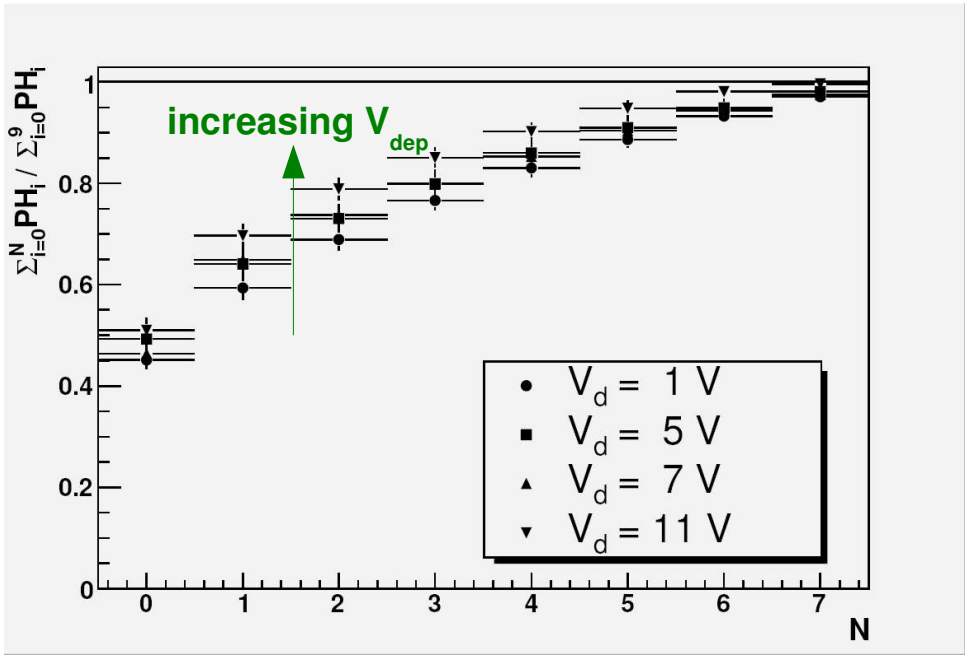


LDRD-SOI-2 (2008)

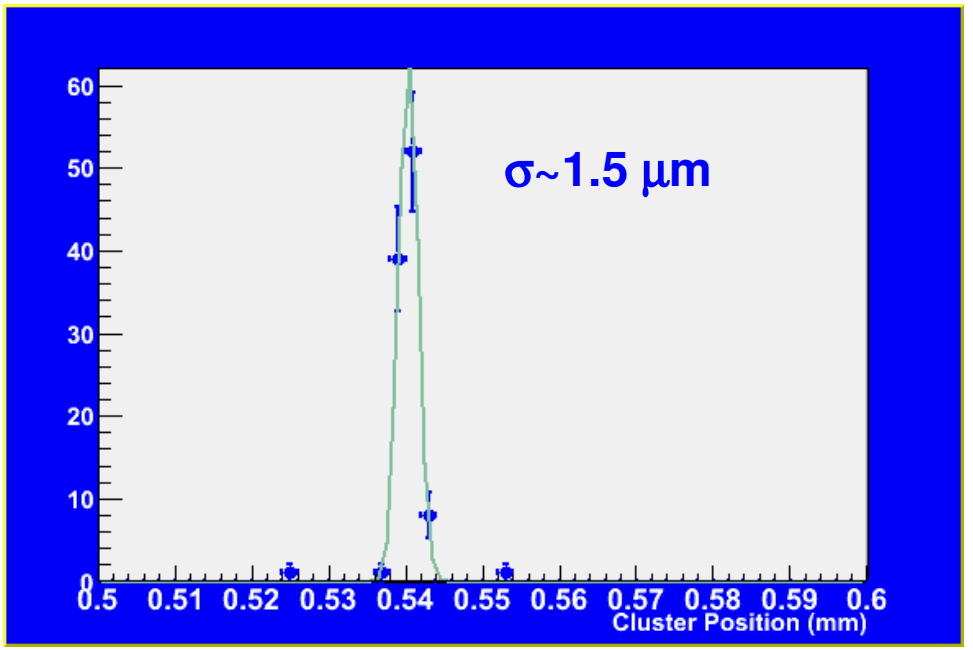
- OKI 0.20 μm FD-SOI process; production process, optimized for low leakage current
- larger size prototype (5x5 mm^2), 20x20 μm^2 pixels, 1.8 V operational voltage
- 40x172 analog pixels: simple 3T architecture for technology evaluation
- 128x172 digital pixels; evolution of chip-1 digital pixel: 2 capacitors for in-pixel CDS, clocked comparator with current threshold output; 40 transistors/pixel
- 50 MHz readout, multiple (25) parallel outputs for improved frame rate
- Just received back from fabrication, first tests with IR laser underway

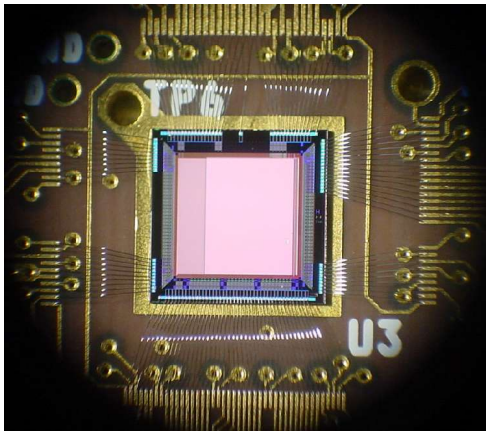
First IR laser tests on LDRD-SOI-2

Charge fraction vs nb of pixels in cluster



Reconstructed laser position





- First preliminary tests performed on the analog pixels with 1060 nm laser focused to a 5 μm spot
- Signal vs. depletion voltage follows same trend as LDRD-SOI-1, back-gating effects becoming important for V_{dep}~10 V
- Improved noise performance w.r.t. LDRD-SOI-1 (factor 3-5)
- Charge fraction distribution shows smaller charge spreading for higher V_{dep}

Summary and Outlook

- SOI-CMOS technology built on high-resistivity substrates allows the fabrication of reversely-biased silicon sensors integrated with full CMOS circuitry on the same device
- Two prototype pixel chips designed at LBNL in OKI deep-submicron FD-SOI technology
- LDRD-SOI-1 prototype in 0.15 μm process successfully tested:
  - analog and digital pixel detection capabilities demonstrated with IR laser and 1.35 GeV e^- at LBNL ALS
  - back-gating effects significant at high substrate voltages and after irradiation with protons
- Second prototype LDRD-SOI-2 fabricated in optimized 0.20 μm process:
  - just received back from foundry, currently being tested
  - first tests with focused laser on analog pixels confirm results from LDRD-SOI-1 prototype with improved noise performance
- Several potential technology spin-offs for SOI monolithic pixels:
  - thin, fast and integrated detectors for High-Energy Physics applications
  - X-ray detection for application at synchrotron facilities
  - VUV imaging for beam diagnostics, e.g. via thinning and back-processing; application foreseen at the plasma accelerator facility LOASIS @ LBNL