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GASTONE: a new ASIC for the cylindrical GEM Inner Tracker of KLOE experiment at DAFNE

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Abstract

GASTONE (GEM Amplifier Shaper Tracking ON Events) is a low-noise low-power mixed analog-digital ASIC designed to host 64 channels to readout the GEM Inner Tracker (IT) detector foreseen in the upgrade of the KLOE apparatus at the LNF e^+e^- DAFNE collider. Each channel is made of a charge sensitive preamplifier, a shaper, a discriminator and a monostable. Digital output data are transmitted via serial interface at 100 Mbit/s data rate. The chip has been developed by using the CMOS AMS 0.35 process. A 16 channels prototype has been produced and used to instrument the single layer IT prototype that has been tested with cosmic muons and a proton beam test at CERN.

Keywords: ASIC; GEM; CMOS;

1. Introduction

The KLOE apparatus has been designed for the study of CP symmetry violation in K_L decays and, in particular, for the measurement of $\Re(\varepsilon'/\varepsilon)$ with an accuracy of ~ 1 x 10^{-4}. It consists of three main parts: a large cylindrical Drift Chamber (DC), a hermetic lead-scintillating fibres electromagnetic calorimeter and a large magnet surrounding the whole detector, consisting of a superconducting coil and an iron yoke. During the six year of data taking KLOE has shown to be a very reliable and efficient apparatus, thefore the upgrades will be limited to some critical points. The major upgrade concerns the introduction of an Inner Tracker (IT) located between the beam-pipe and the DC [1]. The upgrade would allow the apparatus to reduce the 28 cm DC first hit detection, improving K_{0S}, K_{0L} and $K^{\pm}$ measurement near the interaction point and increasing the geometrical efficiency for K_{0S} and η low momentum tracks

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decays. The IT main requirements are a good spatial resolution ($\sigma_{r\varphi} \cong 200$ µm and $\sigma_z \cong 500$ µm) and a very low material budget in the active area (less than 2 % of X_0).

Therefore we propose a very low mass and dead-zone-free detector based on cylindrical and dead-zone-free triple GEM technology. The tracker will be made of five concentric cylinder triple-GEM detectors instrumented with stereo strips readout for a total amount of about 35000 readout channels. A prototype of the innermost layer is shown in Fig.1.

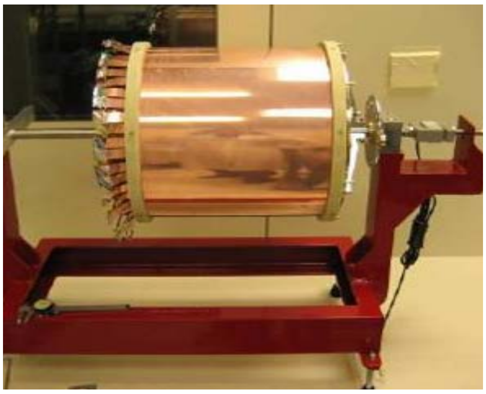

Fig.1 Prototype of innermost layer

Unfortunately, as a consequence of the stereo readout and the assembling procedure, the strips parasitic capacitance will range between 1 pF and 50 pF according to the strip position, making impossible the S/N optimization by means of capacitive matching.

Other constraints for the electronics come from the low charge amplification and gain spread of GEM devices and the quite high density readout. As a consequence high modularity, serial output and low power dissipation devices are required to instrument the detector.

2. Circuit description

A 16-channel prototype front-end chip has been developed to fulfill the requirements. Its block diagram is shown in Fig. 2. The analog channel architecture is made of four different blocks: a charge sensitive preamplifier, a shaping stage, a leading-edge discriminator with programmable threshold and a monostable circuit [2] [3]. The charge sensitive preamplifier integrates the input current signal, while the amplifier-shaper provides noise filtering and semi-gaussian shaping. The discriminator generates the digital tracking information and, finally, the monostable stretches the digital signal to store the information waiting for Lev1 trigger signal.

The expected event rate on the most internal layer strip of the final detector will be not greater than 30 KHz/strip, thus a DC baseline restoration circuit to limit baseline fluctuation is not strictly needed.

The digital section implements the control logic for threshold sensing/setting and for the serialization of the discriminated signals for data readout.

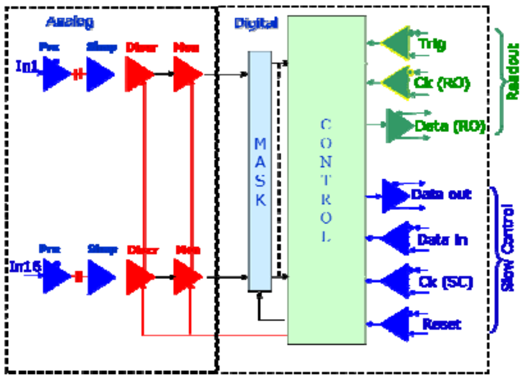

Fig.2 Circuit block diagram

2.1. The analog section

The input charge amplifier consists of a common-source amplifier in cascode configuration with an active feedback made of a 150 fF capacitor and a PMOS transistor with W/L = 2.5/100 and equivalent resistance of about 100 MΩ for the nominal bias current of 100 nA.

The main characteristics of preamp are a gain of 5.6 mV/fC @ CIN = 0pF, a non-linearity less than 1% (0 – 50 fC) and a supply current of about 110 µA.

The shaper too consists of a cascoded common source amplifier, featuring a voltage gain of 4 and non-linearity less than 3% with a supply current of about 100 μA. The measured peaking time is between 10 and 70 ns for a capacitive load ranging between 10 and 50 pF. The entire preamp-shaper circuit has a global charge sensitivity of about 20 mV/fC. A leading edge discriminator follows the shaper stage, with a threshold varying between 0 and more than 200 fC, with a supply current of 180 μA. It is characterized by a threshold spread better than 2% with an offset of about 2.2 mV rms over the entire threshold range. A monostable follows the discriminator stage allowing a variable output pulse ranging between 200 ns and 1 μs, but eventually this range could be increased tuning an external resistor. The total power consumption of the analog channel is 1 mW.

2.2. The digital section

The digital section of the chip has been designed and implemented to manage the 64 channels of the final chip.

Upon the arrival of the trigger signal, the discriminated signals are stored into a 96-bit register. The event frame is described in Table 1.

Table 1. Event frame description

# Bits	*Content*
8 bits	Synchronization
2 bits	Header
5 bits	Trigger ID
9 bits	Chip ID
64 bits	DATA
8 bits at '0'	End of frame

A relevant feature is that the 50 MHz readout clock is active only after the arriving of trigger signal, avoiding possible cross-talk with the analog section. Nevertheless, separate analog and digital power supplies have been used while all the I/O signals are implemented in the LVDS standard. At the nominal clock frequency (50 MHz), the readout of the output frame lasts 960 ns as the readout circuit uses both edge of the clock signal.

The Slow Control section of the chip is implemented in the SPI standard and consists of 28 8-bit registers, listed in Table 2, for configuring the chip functionalities, setting the threshold DACs and reading back ADCs. The SPI clock runs at 1 MHz. An internal pulsing procedure has been implemented to inject a fixed charge of 10 fC for calibration and test purpose. The chip also produces a global OR signal to be eventually used in self-triggering applications.

Table 2. List of SPI registers

# Registers	*Content*
8	Mask
4	Threshold (1 per 16 channels)
1	Pulse width (1 per 64 channels)
5	Read back from 5 ADCs
1	Test pulse configuration
8	Test pulse result
1	Control register

The GASTONE layout is reported in Fig. 3 for the developed prototype of 16 channels occupying a silicon area of 3.2 x 2.2 mm2.

A custom Front-End Board (FEB) has been developed, containing a protection circuit to protect the chip from possible spark chamber events [4] and housing two chips, for a total of 32 channels.

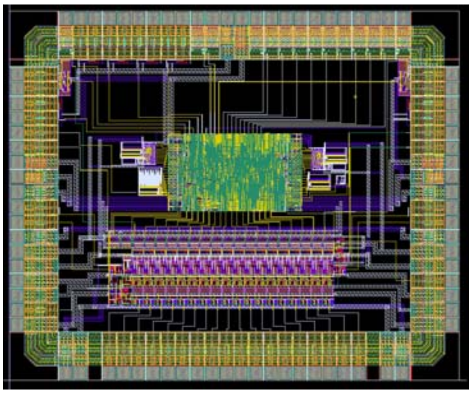

Fig.3 Chip layout

3. Test results

Measurements have been carried out both by means a test bench and with the electronics connected to the Layer 0 IT prototype in a dedicated test beam. Although data taking analysis is still in progress, preliminary results show the good uniformity response of the GASTONE chip over the detector area instrumented with it.

The chip has been tested on the test bench by using an Agilent Pulse Generator 81110A and a custom VME board where the SPI control and readout protocol has been implemented.

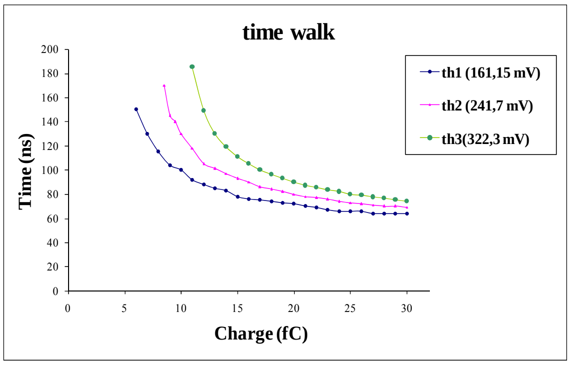

Fig. 4 Time walk vs Qin at Cdet = 10 pF

The measured ENC (erms) is about 880 e- + 61 e-/pF corresponding to 0.63 fC for an equivalent capacitance value of 50 pF associated to the maximum strip length. This noise value sets a safe level of 3 fC for the discriminated detector signal.

The time response of the chip as a function of the input charge has been measured for different thresholds and as expected by the adopted leading edge technique, it tends to increase as the charge approaches the discriminator threshold. In Fig. 4 the results for Cdet = 10 pF are shown.

The hit efficiency has been measured and very preliminary results are shown on fig. 5, where the impact point shape is due to the streamer tubes used as tracking system.

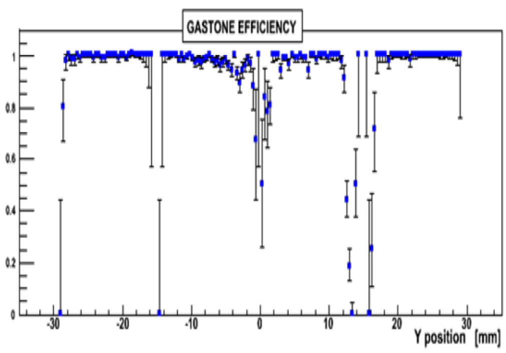

Fig. 5 GASTONE hit efficiency measurements

4. Conclusions

The test results demonstrated that GASTONE is suitable as readout electronics of the KLOE inner tracker detector. Its low noise and low power characteristic fully comply with the detector requirements. Some improvements are under development to integrate the protection circuit on the final 64-channel version of the chip, in order to increase the compactness of the final front end board that will host 128 channels.

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