Beam-Test Results from ISIS

D. Cussans on behalf of the LCFI Collaboration:

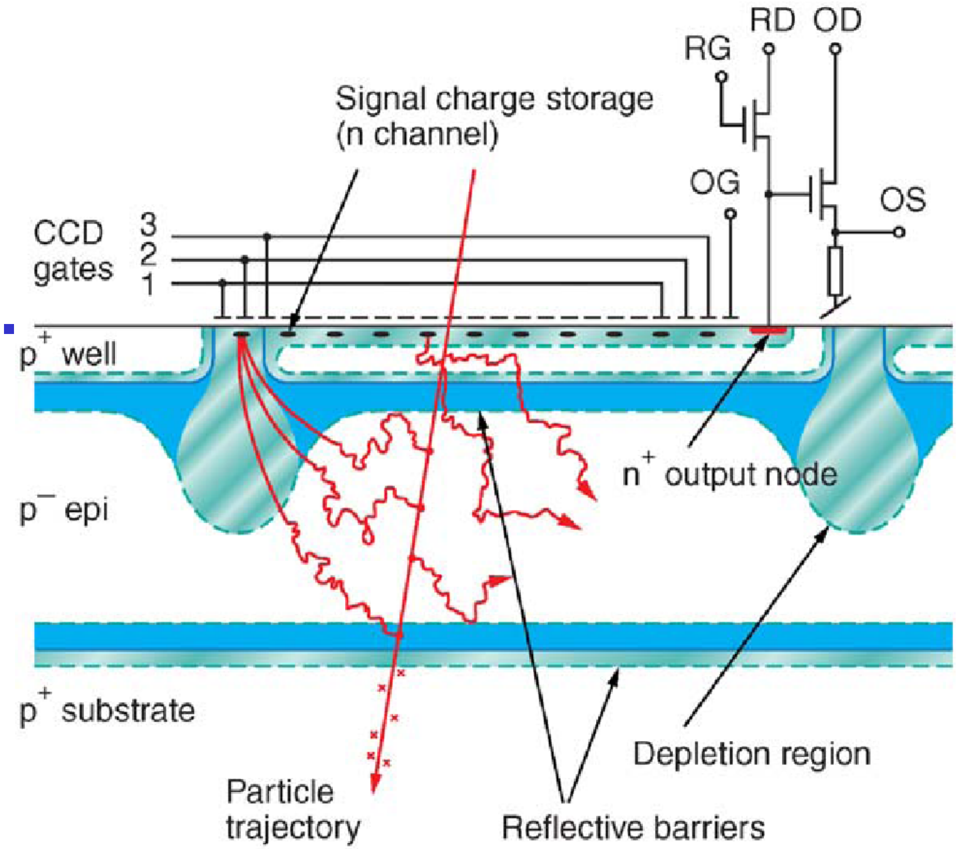
University of Bristol
University of Edinburgh
Glasgow University
Liverpool University
University of Oxford
Rutherford Appleton Laboratory

Outline

- Introduction to ISIS
- ISIS1 device
- Characterization
- Beam-test
- Summary

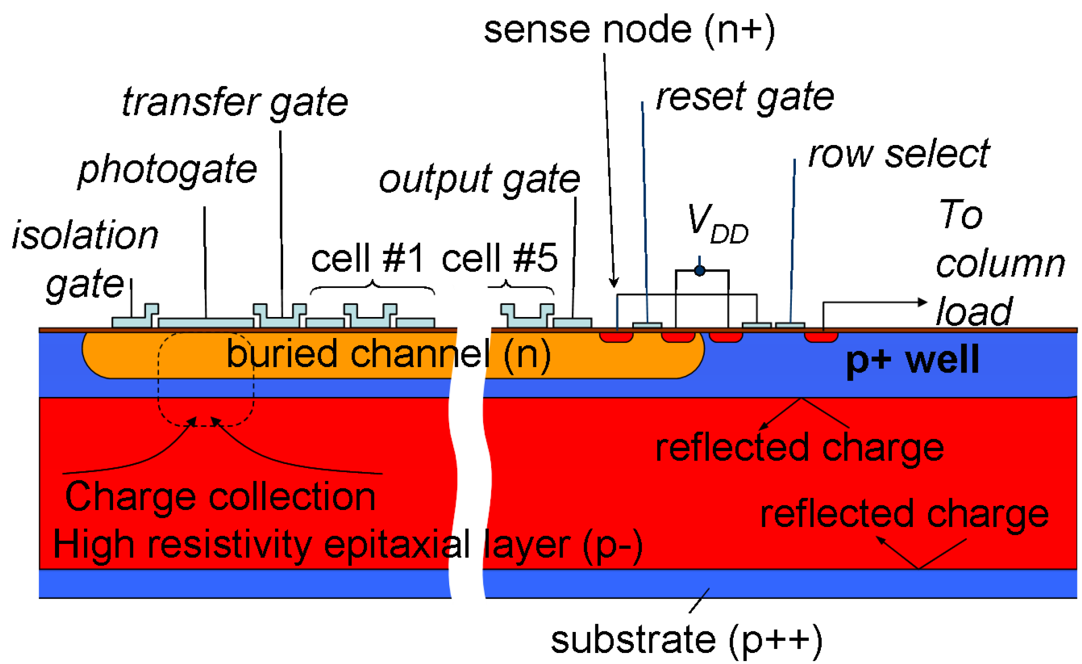
Introduction to ISIS

- In-situ Storage Image Sensor
- MAPS pixel sensor with CCD register in each pixel.
- First used for optical imaging
- Idea developed for charged particle tracking.



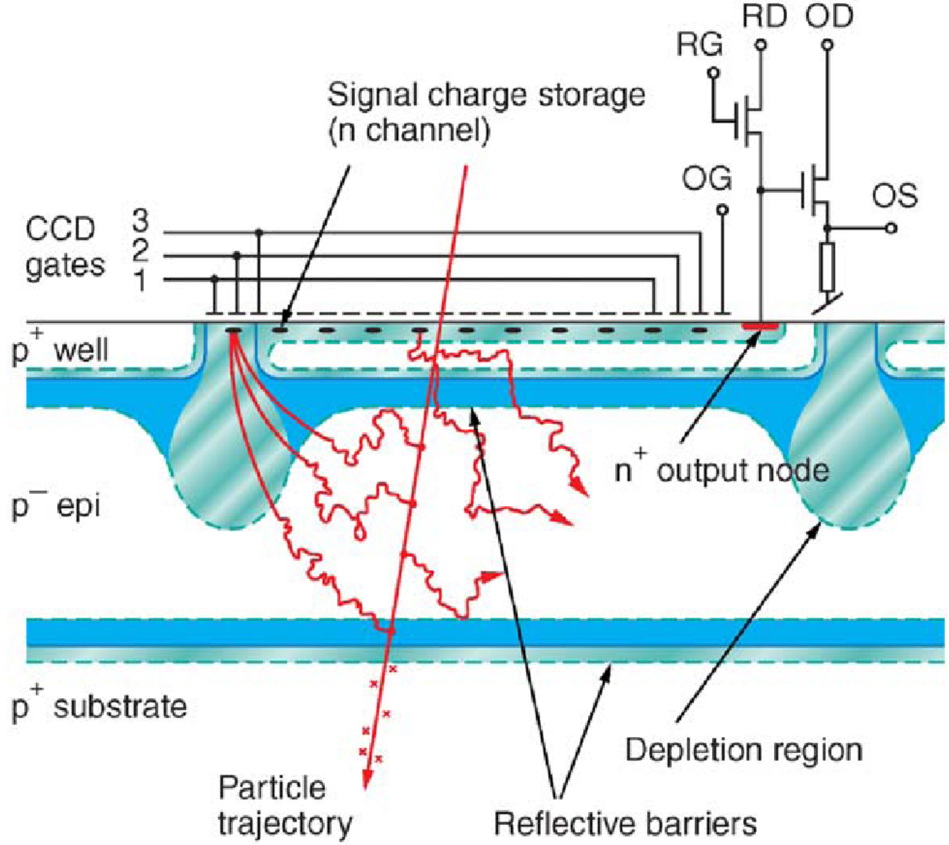
Introduction to ISIS

- Charge liberated in epitaxial layer is reflected by p-/ p+ boundaries until collected at photo-gate.
- Prototype (ISIS1) has variants with and without p-well



Introduction to ISIS

- Designed for "burst" data taking.
- During active period charge is periodically shifted into short CCD register.
- During readout period charged is moved to output gate.



ISIS @ ILC

- **ISIS Ideal detector for ILC**
- **Burst structure:**
  - 2820 bunches separated by 337ns (950μs train)
  - 5 Hz bunch repetition
- **~ 100 hits/mm^2/bunch-train for detector at 15mm from beam**
- **Aim for 0.1% X_0 per layer, implies epitaxial thinner than ~50μm**

ISIS @ ILC

- ISIS with 20 element storage in each pixel

- Low clock speeds
  - 20kHz during bunch-train
  - 1MHz during gap (multiplexed)
  - ... hence reduce power consumption

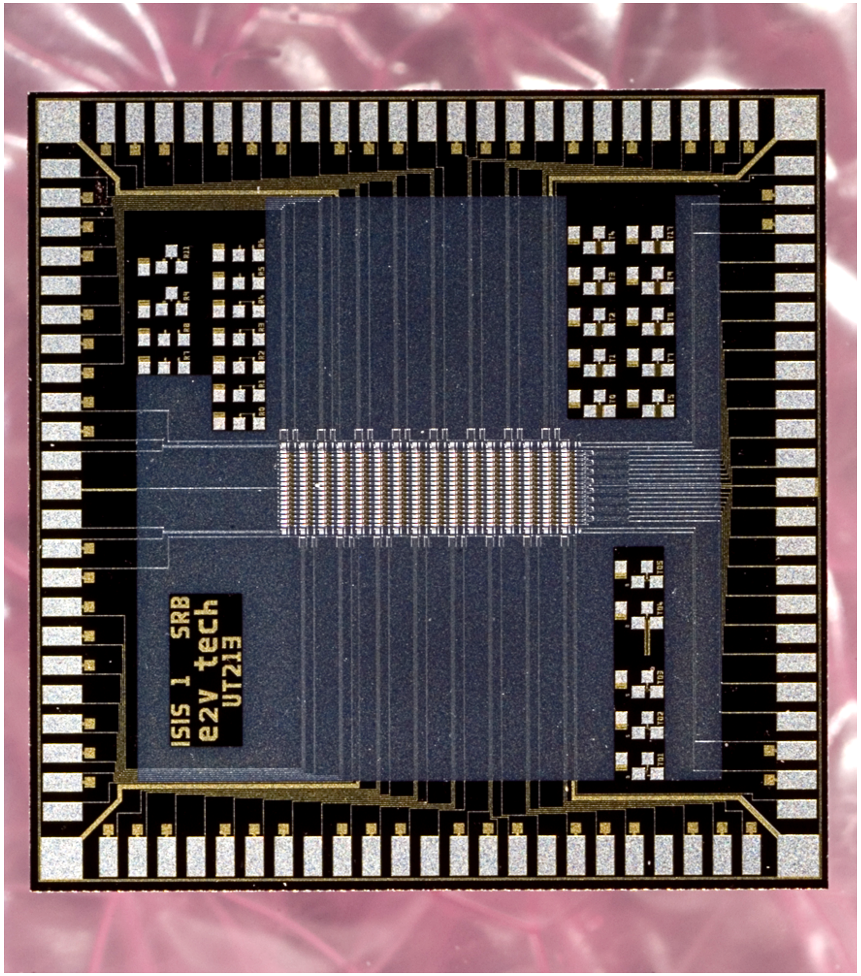
- Shift charge rather than read out voltage during bunch train – lower sensitivity to EMI

ISIS1

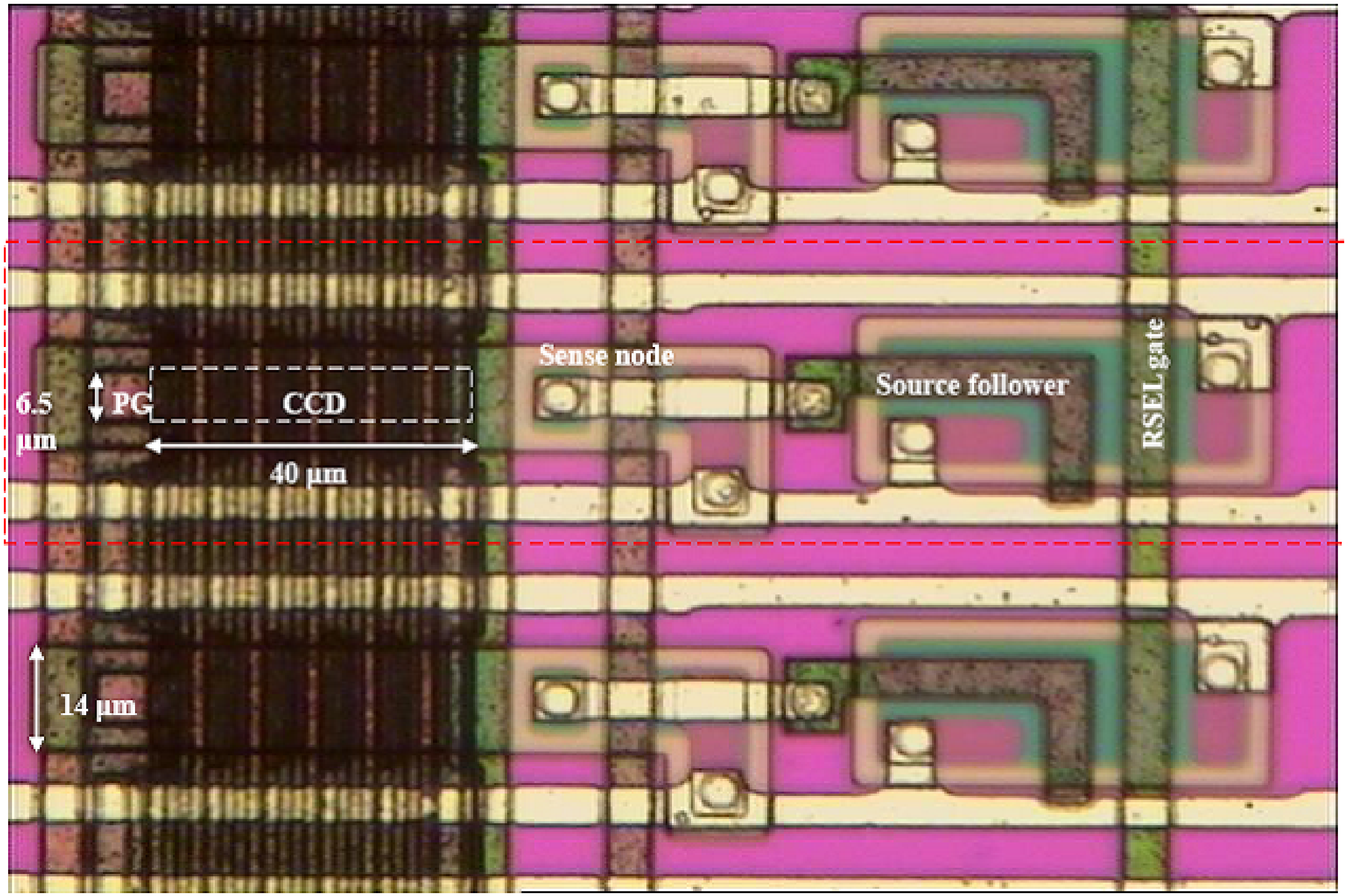
- "Proof of principle" device for particle tracking
- 50µm epitaxial layer
- Produced by e2v in a CCD process (no on-chip logic)
- 16 x 16 pixels, each 160µm x 40µm
- Column -parallel readout (16 analogue outputs)
- Variants with and without p-well (no apertures in p-well, reply on punch-through go get charge to photo-gate)

ISIS1

- Photo-gate
  (isolation gate on 3 inactive sides)
- Transfer gate
- 5 element CCD
- 3-transistor output circuit

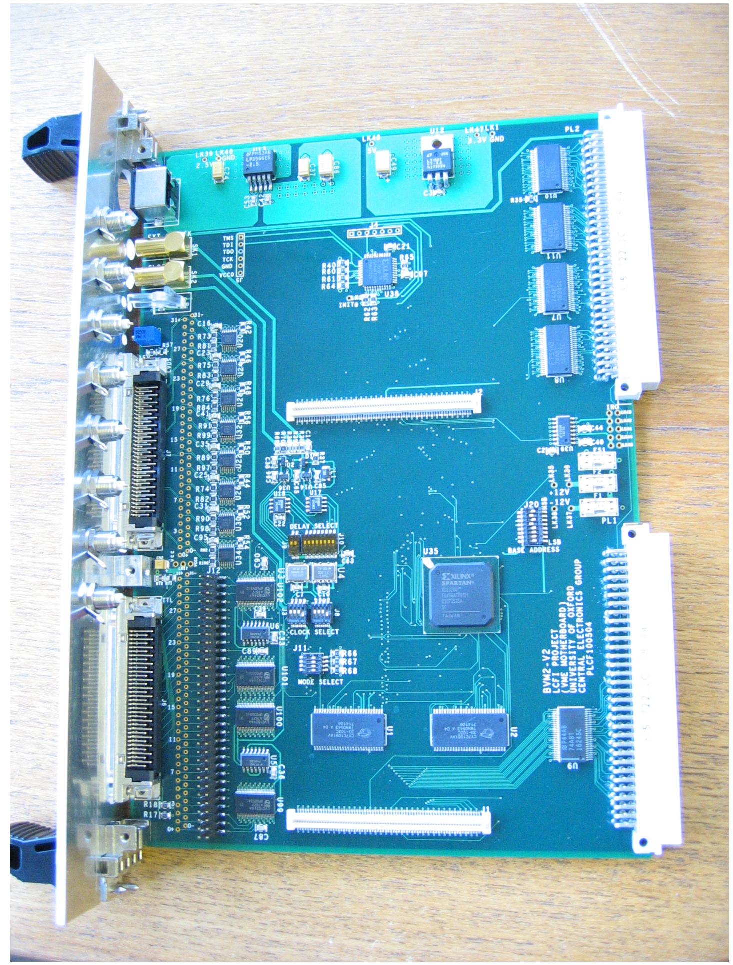


ISIS1



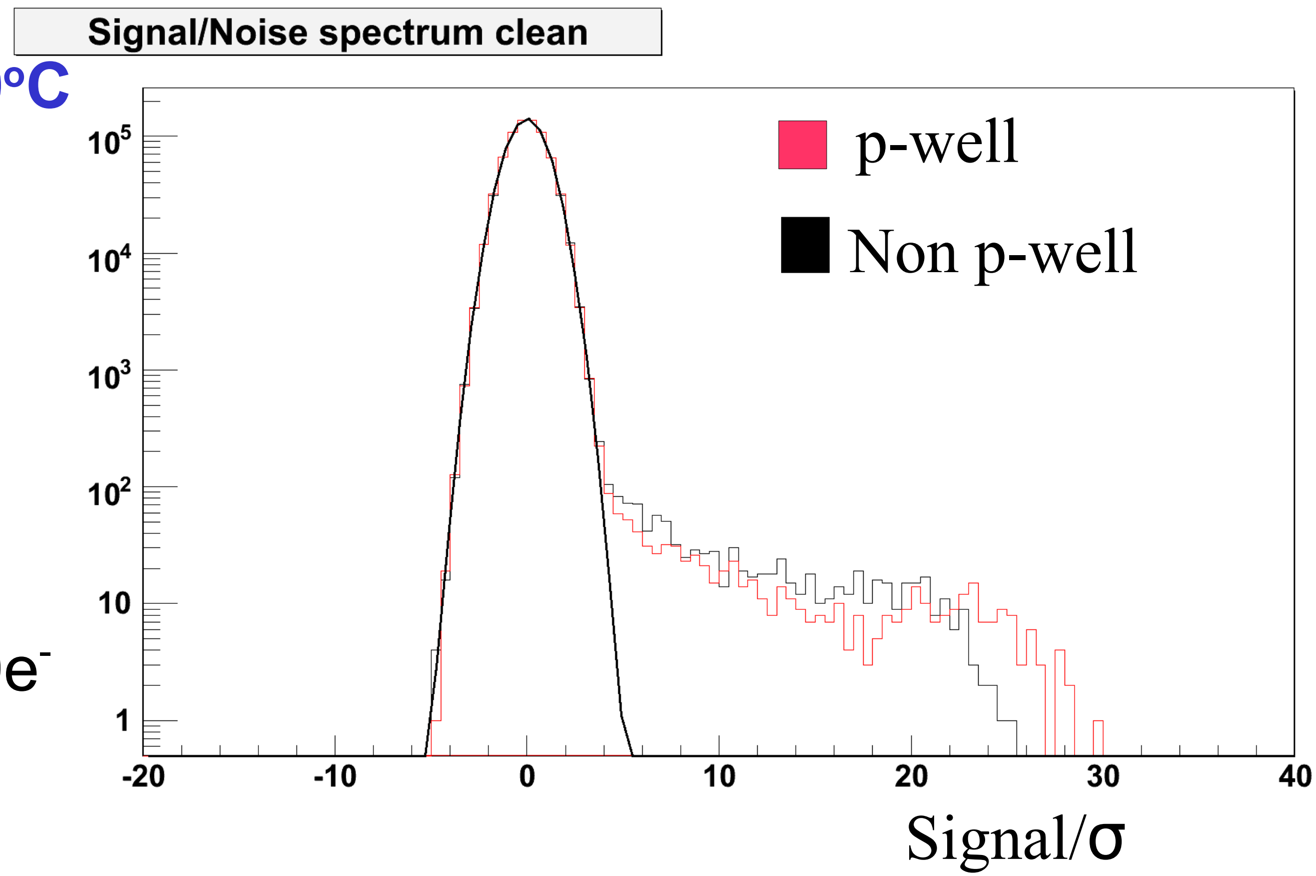
Readout and DAQ

- Correlated double sampling
- Sixteen analogue outputs multiplexed onto four CAEN 14bit V1724 ADCs
- VME based system using Labview to control
- Control signals driven by custom sequencer - BVM2



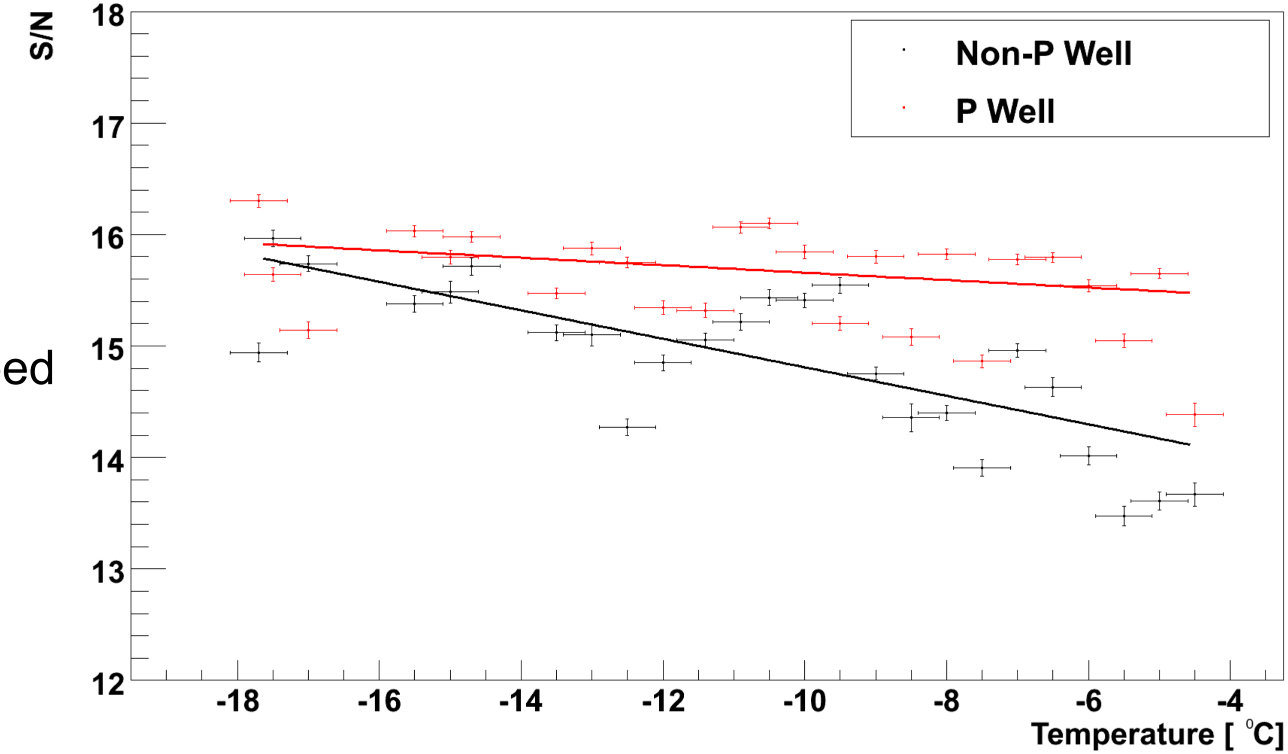
Characterization - ^{55}Fe Spectrum

- **SNR for 6keV ^{55}Fe photons = 16 at -20°C**
- **Gain:**
  - 2.9 µV/e (no p-well)
  - 2.0 µV/e (p-well)
- **^{55}Fe signal ~ 1600 e^-**
  - Noise ~ 100e^-
- **Expect MIP signal ~ 4000 e^-**



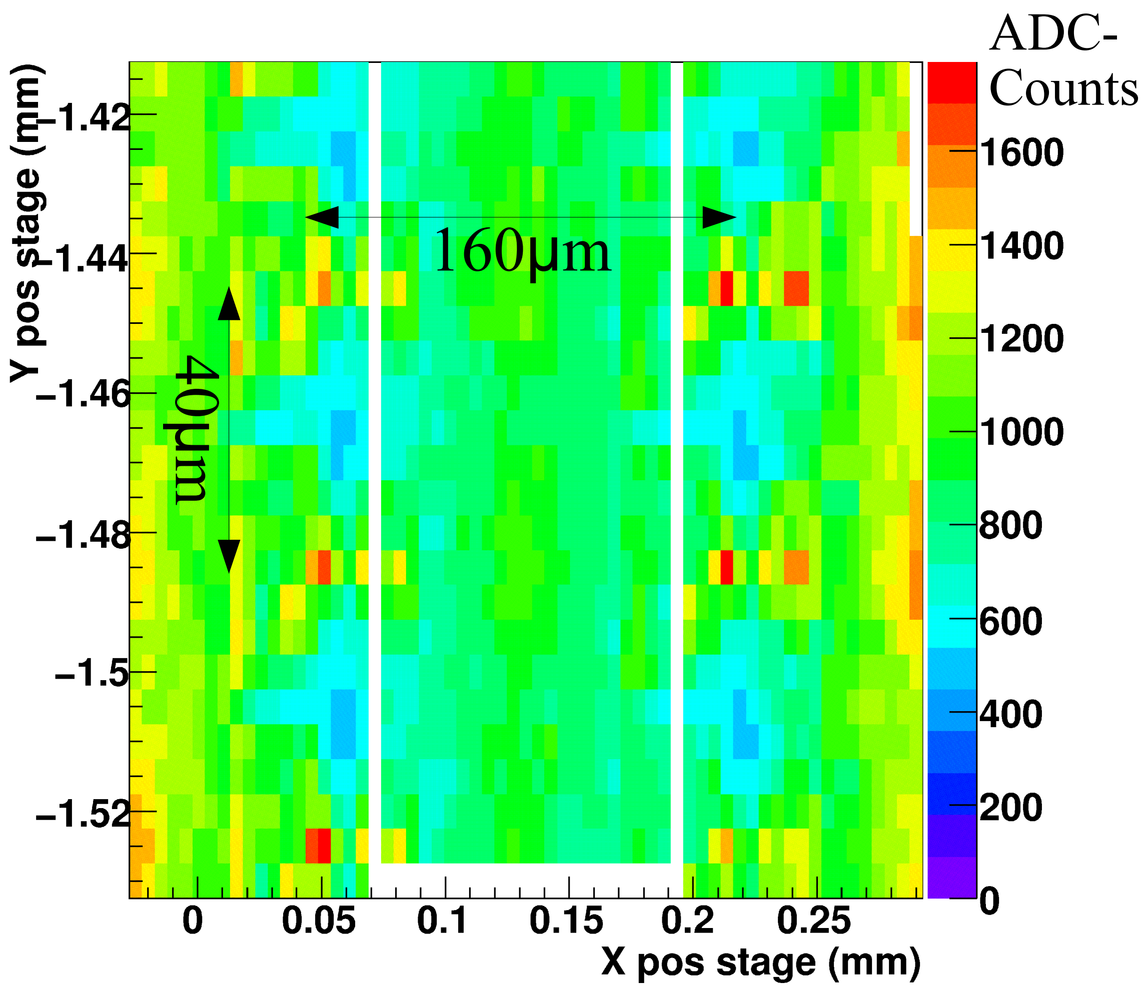
Characterization – Noise Temperature Dependence

- **Noise at -20°C ~ 100e-**
- **ISIS1 needs to be operated at low temperature:**
  - CCD integrates dark current – must not exceed full well capacity.
  - for acceptable SNR



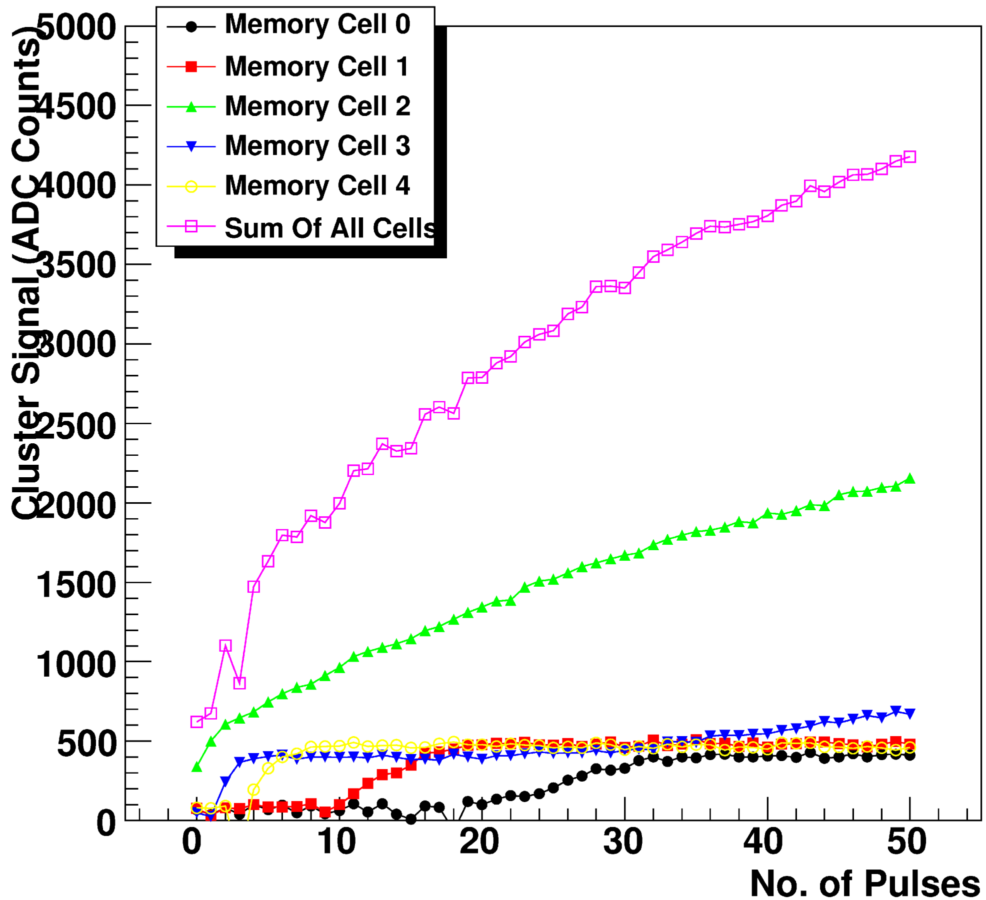
Characterization: Charge Collection

- **Scan laser (660 nm) over surface of device**
  - White line is an artifact of scan, not sensor
- **Cluster charge shown.**
- **Illuminate from above**
  - Large effect from top-surface metalization.
  - Results from 1062nm from below still being processed.



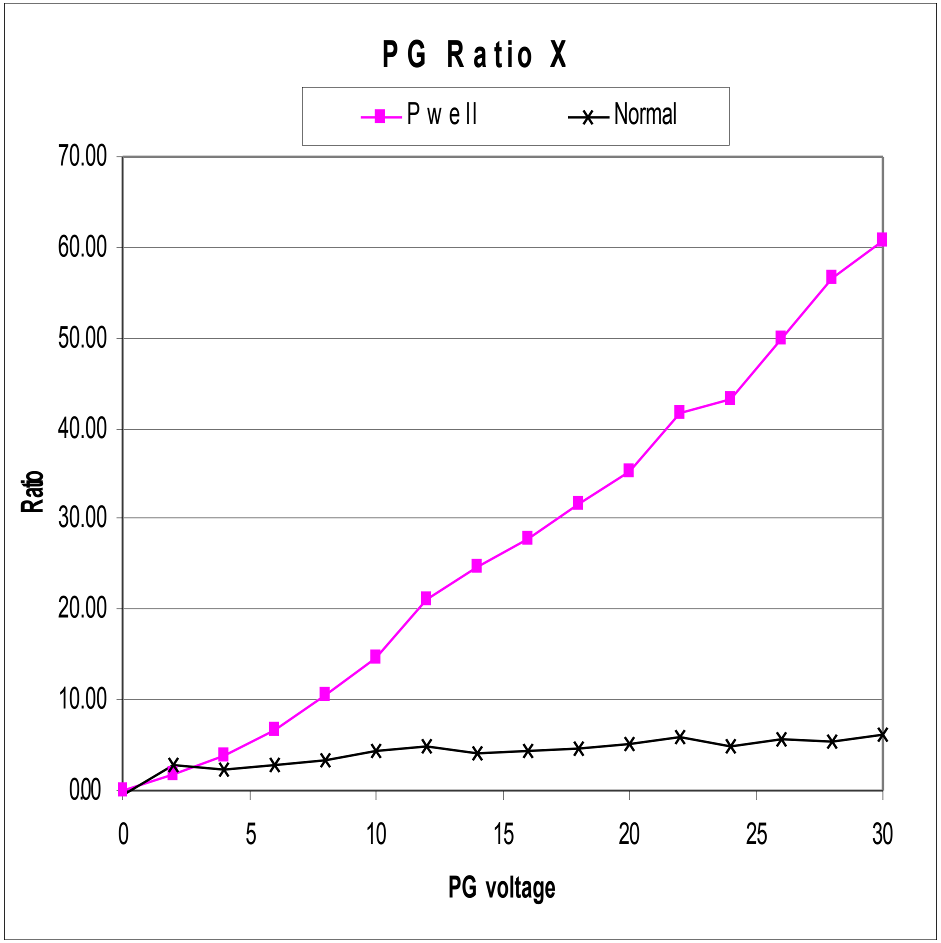
Characterization - Linearity

- Laser with spot size of a few microns used to deposit charge.
- Multiple pulses used. Amount of charge controlled by number of pulses.
- No sign of saturation up to ~ 7 MIP total charge.



Characterization - p-well

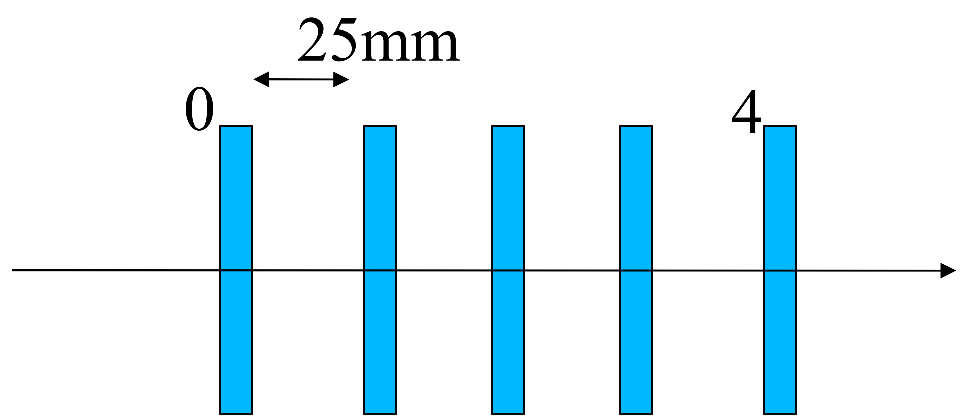
- **Check function of p-well**
  - Illuminate ISIS1 with ^{55}Fe source
  - Count hits as a function of photo-gate voltage
  - Change sequence to omit integration phase (don't clock charge from photo-gate)



- **P-well protects CCD register.**
  - Charge punched through to photo-gate

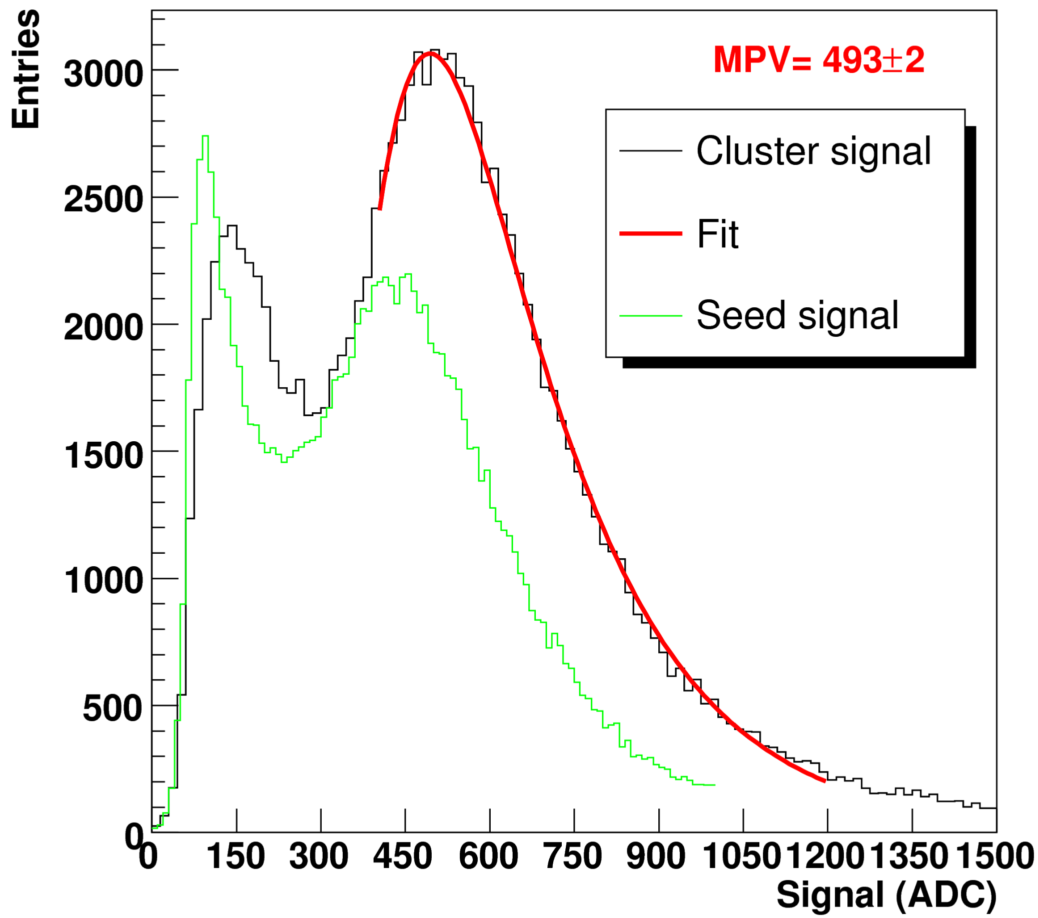
Beam-Test

- **Telescope of five ISIS1 devices (non p-well) Illuminated with 6GeV/c electrons at DESY**
- **Clustering:**
  - Find seeds of 5 v above pedestal.
  - Add charge from eight neighbouring pixels (2 v cut)



Beam-Test: Cluster Charge

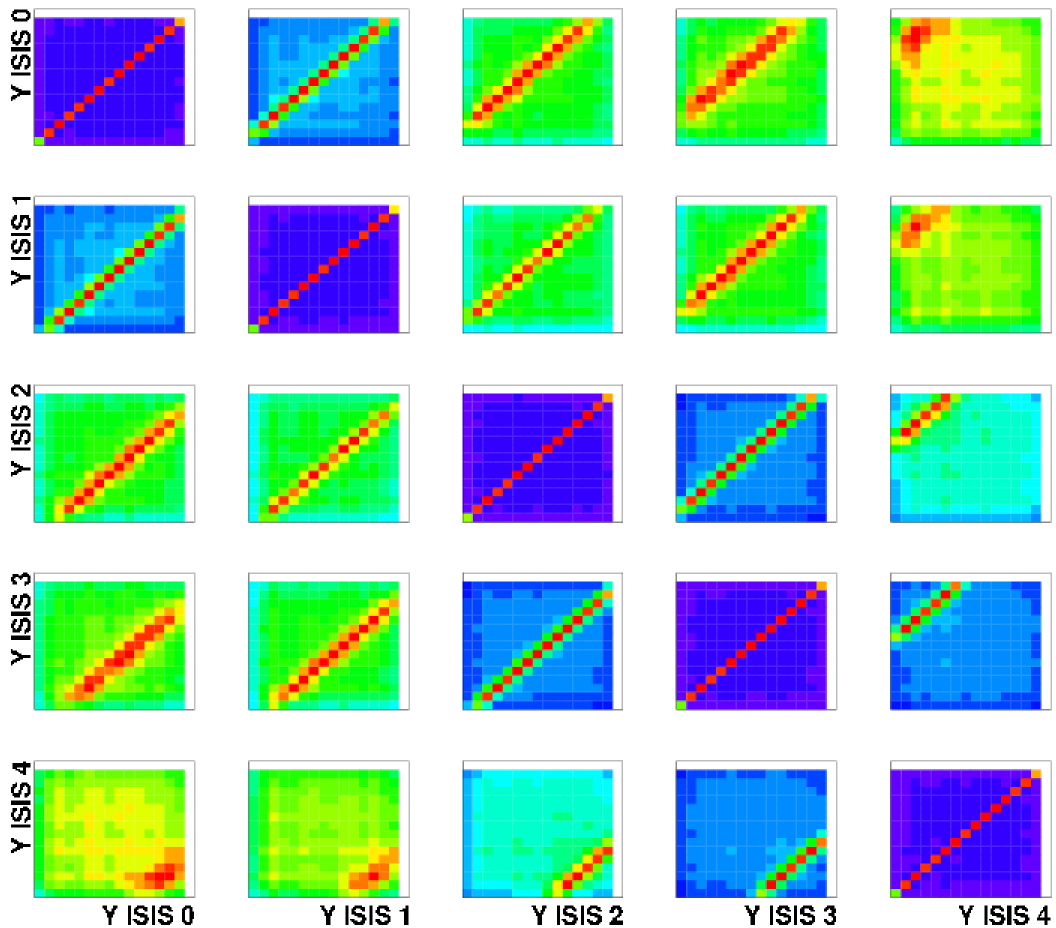
- **Hits clearly seen**
  - Most probable value 3.9ke$^-$



- **“Twin-peaks” structure caused by:**
  - noise
  - charge spreading over many pixels.
  - Charge lost to output structure.

Beam-Test: Track Finding

- **Plot correlation of hits in one plane vs. another plane**
  - "y" (pixel short side) direction shown
  - "x" direction similar
- **Tracks clearly seen**

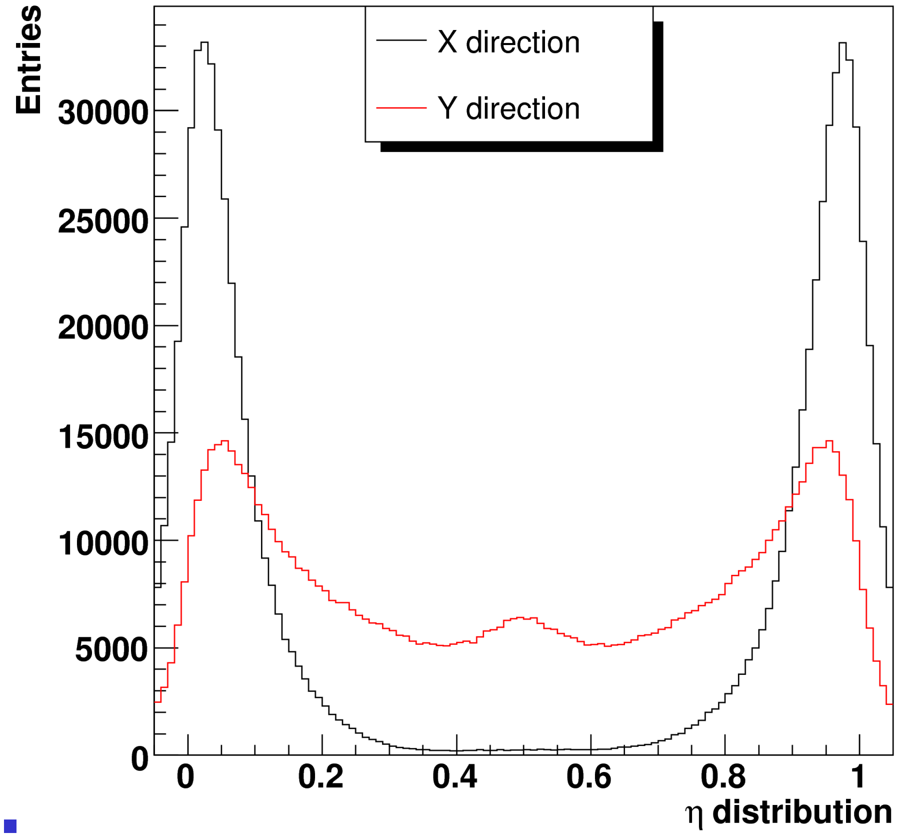


Track fitting

- **Form cluster from seed and highest neighbour (no cut on neighbour)**

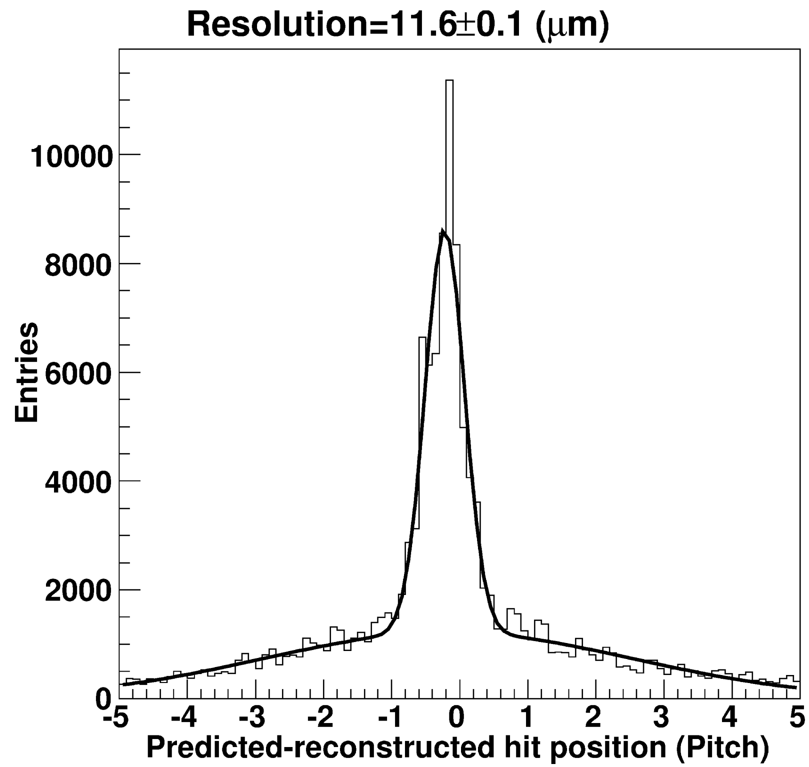
- **Calculate "η" distribution**
  - $Q_{right} / (Q_{right}+Q_{left})$
  - Hardly any charge sharing in "x" (long) direction.

- **Use "η" distribution to calculate position of hits.**



Tracking Resolution

- **Four ISIS1 well aligned enough to use for tracking**
  - First four devices
  - Fit track using sensors 0,1,3. Calculate distance to hit in sensor 2.
  - Subtract effect of multiple scattering.

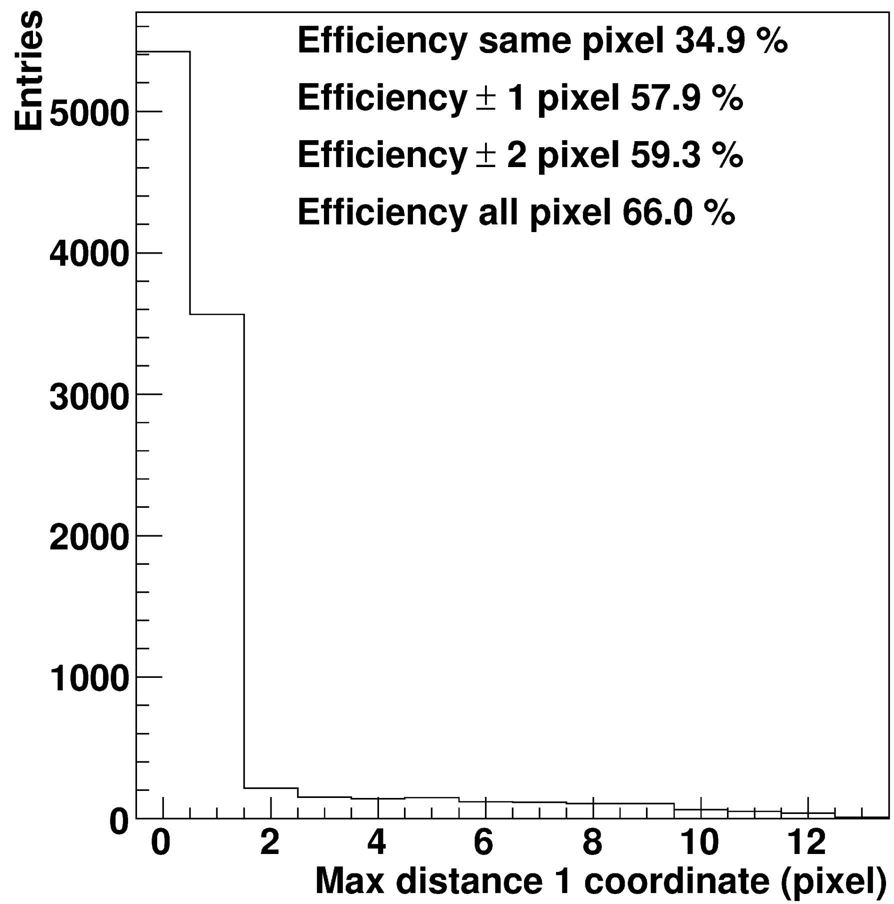


- **Corrected resolution in "y" (short pixel direction) = 9.4±0.2µm.**

- **Negligible charge sharing in "x". Hit always in predicted pixel**

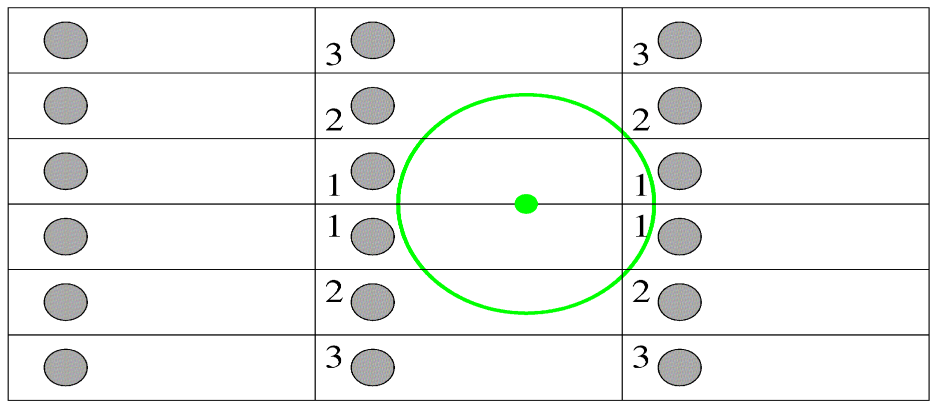
Hit Efficiency

- **59% of tracks have a hit within two pixels.**
  - 35% of tracks have a hit in predicted pixel.
- **Low efficiency due to**
  - 1:4 geometry.
  - Collection of charge by output structure (ISIS1 feature)



Geometry

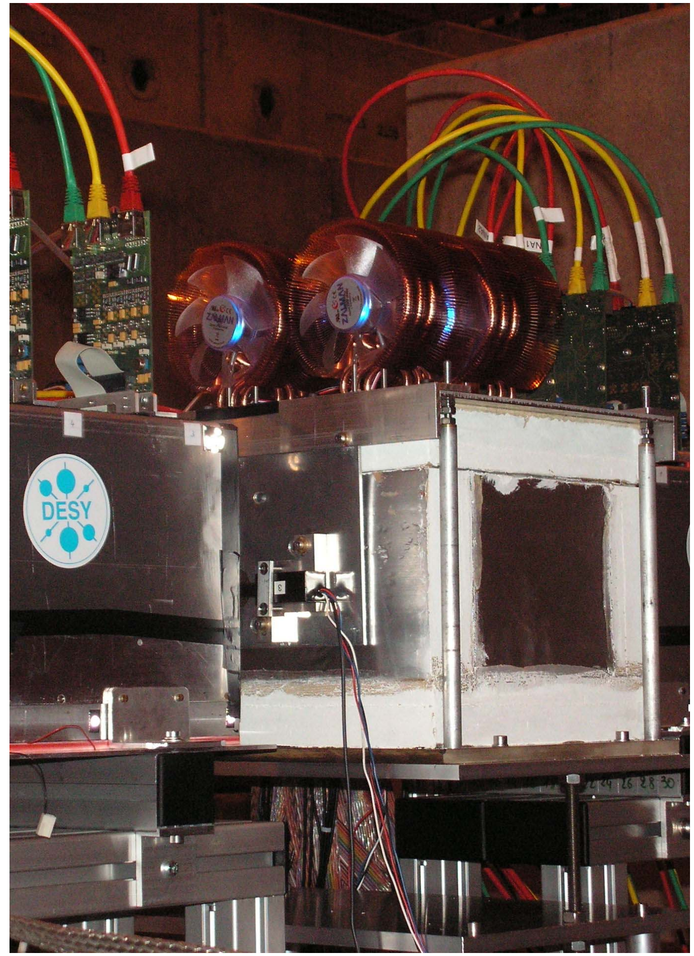
- 4:1 pixel size results in many hits sharing charge over many pixels
- Consider worst case:
- Only ~ 7% of charge collected by highest signal photo-gate
- Would need SNR of 70 for a MIP to pass 5σ cut



Future - ISIS1

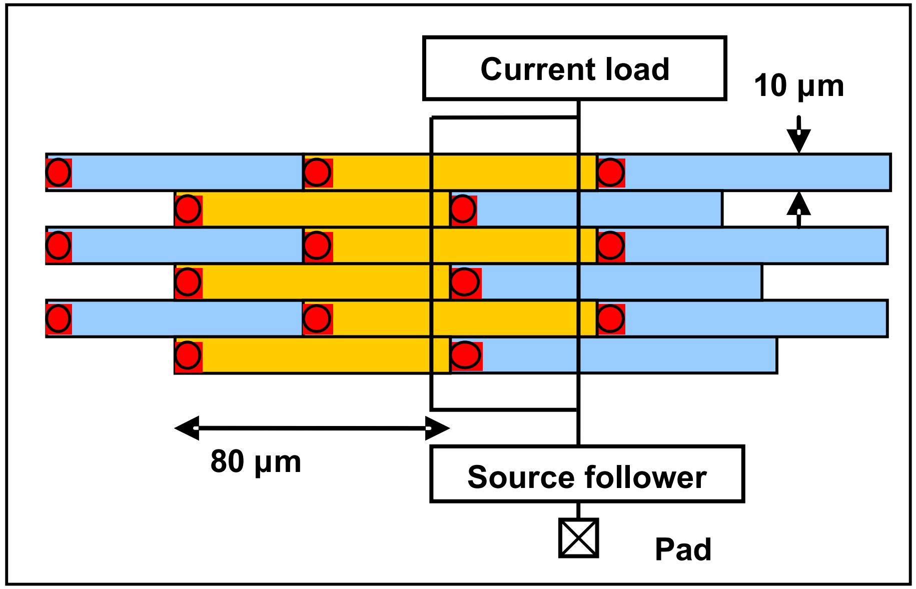
- **ISIS1 test-beam with EUDET telescope. 120 GeV/c π at CERN**
  - Test P-well devices
  - Charge collection

- **Laser scan (660nm/1062nm) of p-well ISIS**
  - Effect of p-well
  - Charge collection



Future Developments - ISIS2

- **ISIS2**
  - True CMOS process. 0.18μm dual gate-oxide
  - Pixel geometry 80μm x 10μm. Staggered to give 20μm x 40μm photo-gate geometry
  - Introduces CCD (charge transfer) into a CMOS process
  - Apertures in p-well (unlike ISIS1)
  - Analogue readout
  - 20 memory cells.
  - Back from fabrication.



Future Developments - ISIS3

- Select process on basis of ISIS2.
- On-chip ADCs
- On-chip Gbit/s serializer
- Three-fold stagger to give almost square photo-gate geometry.

Summary

- **"Proof of Principle" In-situ Storage Image Sensor optimized for particle tracking constructed and tested.**
  - Self contained telescope used for tracking.
- **Advantages for a "burst mode" accelerator such as ILC**
  - Offers benefit of lower clock speed and increased resilience to EMI compared to many other sensor technologies
- **Development continues with ISIS2**

Thanks

- DESY
- EUDET (EU FP7 program) for providing assistance at DESY test-beam