Study of Delay-Line Readout for GEM Detector

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Abstract

Delay-line readout method is suitable for the position sensitive detectors in the early stage of high energy physics experiment at low-rate environment. In this paper, we present a fast delay-line circuit (cut off frequency: 0.7 GHz) equipped with a triple-GEMGas Electron Multiplierdetector for X-ray imaging. An experiment shows that the position resolution of the detecting system is less than 100 μm with readout strip of 0.15 mm width and 0.4 mm pitch at 10^5 Hz counts rate of 8 keV X-ray. A full simulation model has been developed for the design of delay-line electric circuit.

1. Introduction

Recently, Position Sensitive Detectors (PSD) have opened a new trend in the radiation detection and X-ray imaging, such as the Gas Electron Multiplier (GEM) based detector which has high position resolution and stability in intense particle beams [1–3]. Most of the readout techniques for GEM detector based on Center-of-Gravity readout method employ large number of amplifiers and shaping electronics for the channel-by-channel readout. To decrease the cost on electronics and keep good spatial resolution, we design a fast delay-line circuit for the GEM detector readout. The fast delay-line consists of many discrete LC (inductor-capacitor) cells [4], as shown schematically in Fig. 1. These discrete LC cells are connected to individual anode or cathode strips. The localization information is derived from the propagation time of the induced signals traveling along the delay-line and measured directly by current amplifiers at each end of the delay-line. The linearity and time response depend on the accuracy of time difference which is determined by the time delay per cell and the distributed parameters of PCB .

2. Design of the delay-line PCB

Three parameters, the time delay per cell τ, the cut off frequency ω_0 and the characteristic impedance Z_0, are most significant on the design of delay-line PCB. The model of
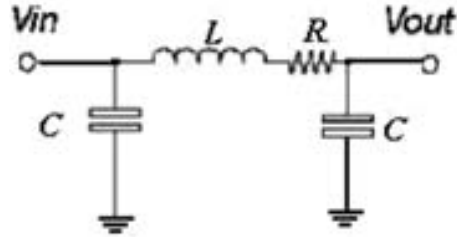

Fig. 1. One delay-line cell (L: inductor, C: capacitor, R: internal resistance of the inductor).

the delay-line cell is shown in Fig. 1. These parameters can be calculated with the following formulas,

$$
\begin{aligned}
\omega_0 &= 1/\sqrt{LC}; \\
Z_0 &= \sqrt{\frac{L}{C}} \Big/ \sqrt{1 - (\frac{\omega}{\omega_0})^2} \approx \sqrt{\frac{L}{C}} \quad (\omega \ll \omega_0); \\
\tau &= \frac{1}{\omega}[\frac{\omega}{\omega_0} + \frac{1}{3}(\frac{\omega}{\omega_0})^3 + \cdots] \approx \sqrt{LC} \quad (\omega \ll \omega_0).
\end{aligned}
\tag{1}
$$

According to these formulas and the typical signals of GEM detector, three delay-line models (named D1, D2 and D3) with different parameters are chosen for both the simulation and the experiment. The parameters are shown in Table 1. The cut off frequencies of all the delay-line PCBs are large enough so that the output signal of GEM detector can pass through with almost no distortion.

A full simulation model of delay-line readout system is constructed in Matlab-Simulink environment [**?,?**] (Fig. 2(a)) according to the electric circuit model of delay-

Table 1
The parameters of the three delay-line models

	L(nH)	R(Ω)	C(pF)	ω_0(GHz)	τ(ps)	$Z_0(\Omega)$
D1	15	0.13	6	3.3	300	50
D2	20	0.23	12	1.67	600	50
D3	290	0.17	7	0.7	1420	207

line readout. It consists of the delay-line readout PCB, the Amplifier, the Constant Fraction Discriminator (CFD, as shown in Fig. 2(b)) and the Time-to-Digital Converter (TDC, as shown in Fig. 2(c)). Each simulated delay-line PCB contains 96 cells. The input signal, a trapeziform pulse with 40 ns width, 3 ns rising time and 0.75 V amplitude, is injected into the delay-line at a certain cell port (in the case shown in Fig. 2(a), the cell port is No.2) and divided into 2 parts, propagating forward and backward along the delay-line. The output signals from both ends of the delay-line are discriminated by the CFD, which output two standard gate signals. The TDC converts the time difference of the two gate signals into pulse amplitude and outputs a digital value. The simulation results show that the delay time is 297.0 ps/cell for D1, 398.5 ps/cell for D2 and 1712.3ps/cell for D3 model, respectively.

Manufactured six layers PCB of delay-line with 96 cells is shown in Fig. 3. Three models of delay-line circuit are calibrated by the pulse signals same as in the simulation. The time differences of output signals at each end of the delay-line shaped by a CFD (Ortec Model 935) are measured by a TDC (Phillips TDC 7186, 25 ps/channel). The measured the time propagation rates are 360.8 ps/cell for D1, 654.7 ps/cell for D2 and 1778.0ps/cell for D3, respectively. Using a digital oscilloscope (LeCroy WavePro 7100A, 1GHz bandwidth) with its function of timing measurement, the time propagation rates can be tested directly and similar values were observed.

In order to take into account the influence of the parasitical parameters of delay-line PCB routes, all parasitical parameters with a matrix are calculated from a distributed routes model of PCB which is constructed by the software of Ansoft 2D Extractor. To simplify the electric circuit model of the PCB route, the parasitical inductance, impedance and the mutual capacitance between two routes are neglected. Only the self-capacitances of the routes are kept down and used to construct the simplest electric circuit model (as the zero-order model). The calculated parameters are: 76.35pF/m on TopLayer, 145.78pF/m on MidLayer1, 149.73pF/m on MidLayer2, 155.13pF/m on MidLayer3, 80.99pF/m on BottomLayer of the PCB, respectively. According to the route lengths in the delay-line PCB, the average capacitance of the PCB routes is about 2.3 pF/cell. After adding this value to the delay-line cell in the above constructed simulation model, the simulation results of the upgraded model show that the delay time are 353.1 ps/cell for D1, 656.8 ps/cell for D2 and 1786.4 ps/cell for D3 and are in good agreement with the calibrating data. The output signals of D1 (with 96 input port) from simu-
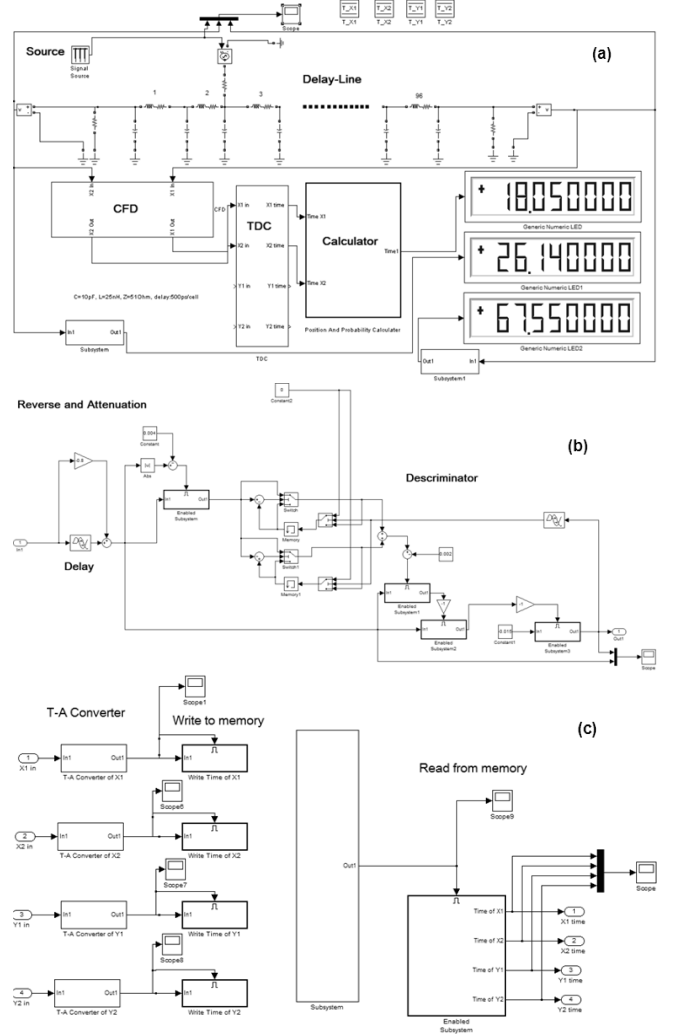

Fig. 2. (a): Simulation model of delay-line readout system. (b): Simulation of CFD model. (c): Simulation of TDC model.
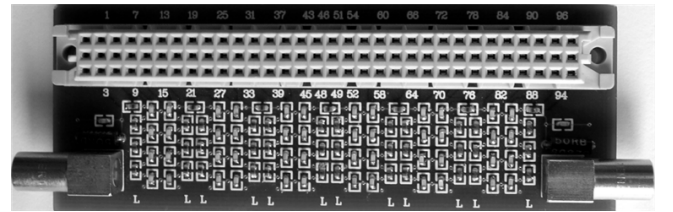

Fig. 3. The photograph of delay-line PCB (with five signal layers and one ground layer).

lation and test are shown in Fig. 4.

3. Experimental setup and results

An effective detecting area of 50 mm × 50 mm triple-GEM detector is built with the delay-line (D1 model). The electrons from a process of avalanche multiplication are collected by readout PCB with stripes of 0.15 mm width and 0.4 mm pitch. The distributed model of the stripes on readout PCB is also constructed by the software of Ansoft 2D Extractor for the parameter matrixes (inductance, capac-
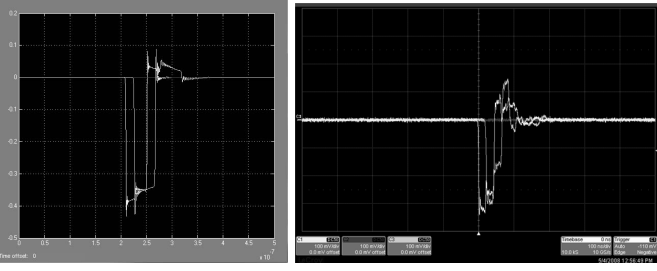
Fig. 4. Compare with the output signals of simulation (left) and experiment (right) (the signal input port is No. 25).
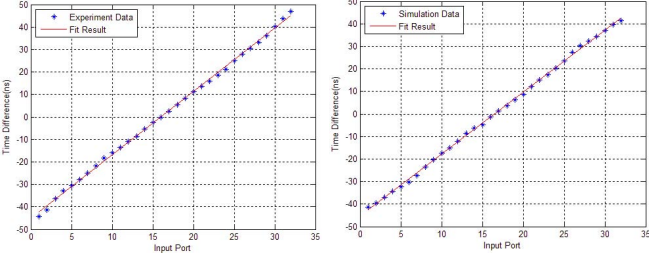

Fig. 5. Experimental and simulative calibration results for 32 channels.
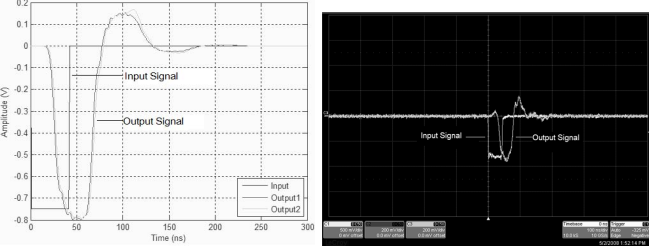

Fig. 6. Output signals from simulation (left) and experiment (right) (Test signal input port is No. 16).
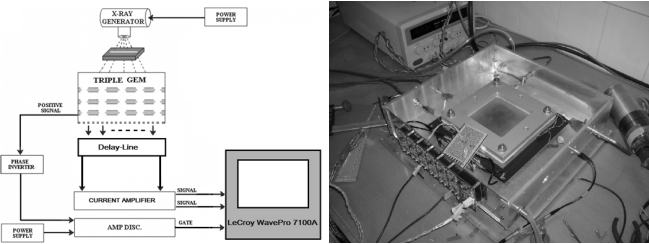

Fig. 7. Left Panel: Setup diagram of GEM+Delay-Line X-ray imaging device. Right Panel: Photograph of GEM+Delay-Line X-ray imaging device.

itance and impedance) calculation. A distributed electric circuit model is generated and imported into Ansoft Simplore. With a full model consists of the GEM detector, the delay-dine (D1) and readout PCB, the delay time is 2.75 ns/channel from simulation and 2.82ns/channel from the test (Fig. 5). The output signals both in simulation and experiment are shown in Fig. 6.

An experimental setup of GEM detector with delay-line readout electronics (Fig. 7) is developed and tested with 8 keV X-ray. An aluminium block with a 0.2mm width slot is used as the collimator. The output signals of GEM detector are amplified by a current amplifier (1ns rise time) and
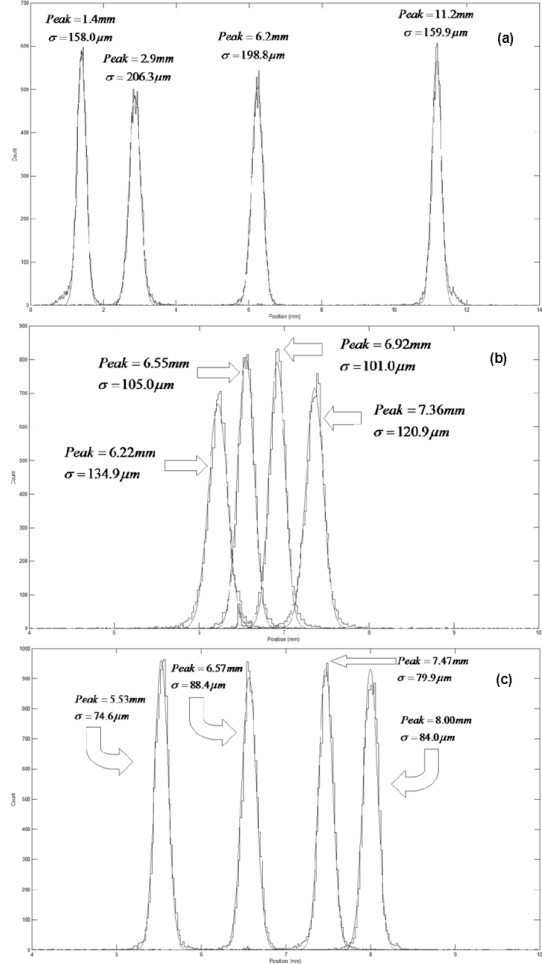

Fig. 8. (a): Position distribution of GEM+D1, tested at the counts of Hz. (b): Position distribution of GEM+D2, tested at the counts of Hz. (c): Position distribution of GEM+D3, tested at the counts of Hz.

the distribution of the time difference of input signals can be measured directly by the oscilloscope (LeCroy WavePro 7100A). The X-ray tube is moved perpendicularly to the direction of stripes and test at several positions. The position resolution (σ) is around 180 μm which include the contribution from the readout electronics. Fig. 8(a) shows the test results of D1. The resolution of GEM+D1 contains the resolution of GEM detector and the contribution of the noise. The waveform of the output signal of every event is similar so that the contribution of the noise is almost a constant. In this case, using a delay-line that has larger per-cell delay can improve the accuracy of the measurement system. Fig. 8(b) shows the test result of GEM+D2 ($\sigma \sim 120$ μm), and Fig. 8(c) shows the result of GEM+D3 ($\sigma \sim 85$ μm). Changing the filament current of X-ray tube, the intensity of X-ray can be varied from 10^3 Hz to 10^5 Hz [7]. The test results show that GEM+D1 and GEM+D2 have the resolution fluctuation of $<\pm6\mu$m while the resolution of GEM+D3 increases 12μm when the intensity of X-ray reached 10^5 Hz.

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4. Summary

The good agreement of simulation and experiment results show that the design method of the delay-line PCB is effective. Due to the different route length of each input port of the delay-line, the zero-order model is not accurate enough to describe the real PCB routes which result in the fluctuation of positional resolution. It may be well described by using a more complex model such as the 1-order or 2-order model. Under our experimental condition, the D3 model with larger per-cell delay has a better resolution than D1and D2, but D2 has more stable performance than D3 as the count rate increasing up to 10^5 Hz.

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