Applications in Particle Physics

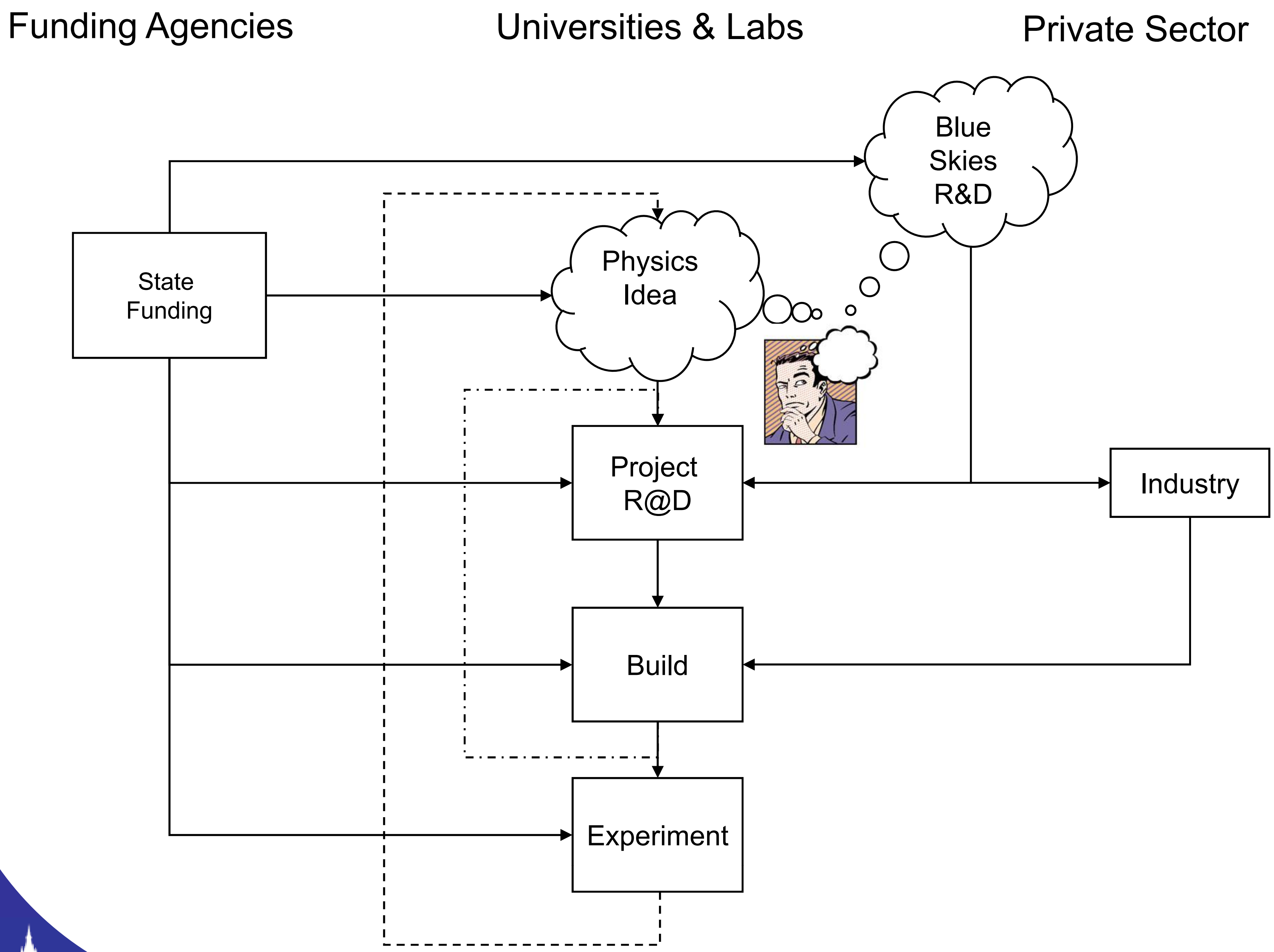
Themis Bowcock

UNIVERSITY OF LIVERPOOL

PSD

Introduction

- Concentrate on applications
  - Many new ideas in other session
  - Active R&D for an experiments
- Do not attempt to produce exhaustive list
  - So much exciting work happening
  - Heavy dependence on electronics
- Flavour of some issues…
  - Highly personal



Funding Agencies

Universities & Labs

Private Sector

State Funding

Physics Idea

Blue Skies R&D

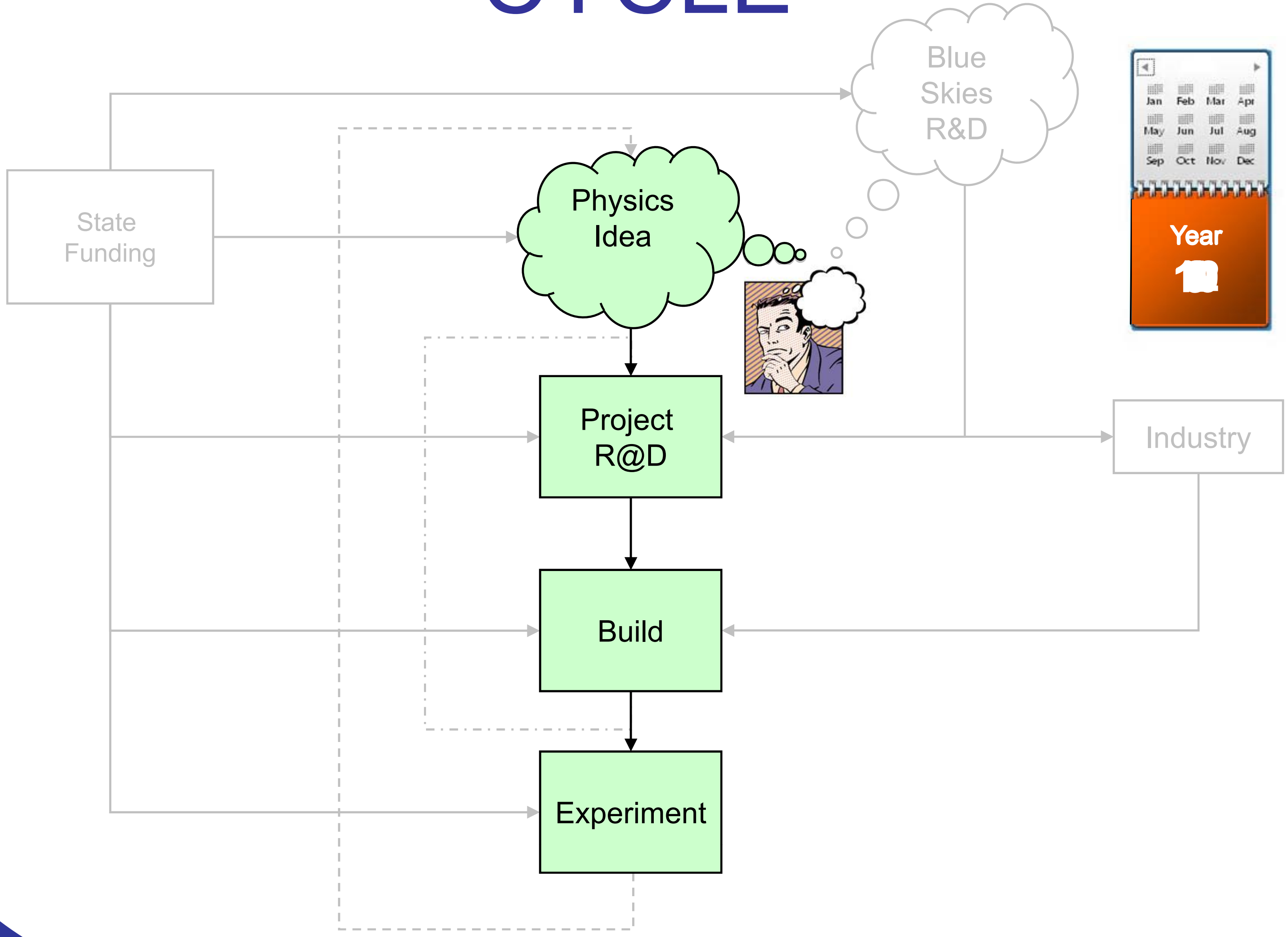
Project R@D

Build

Experiment

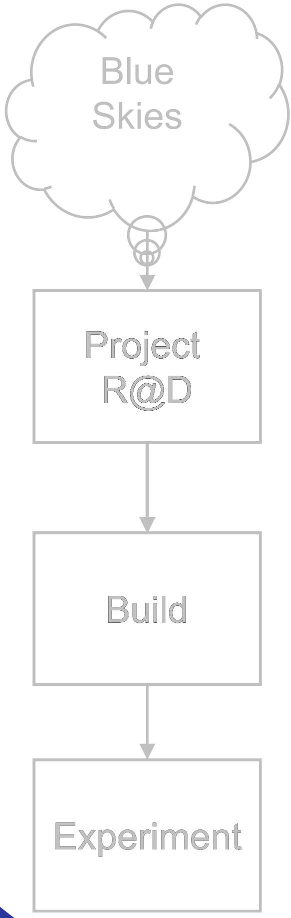
Industry

CYCLE


Blue Skies R&D
State Funding
Physics Idea
Project R@D
Industry
Build
Experiment
Jan Feb Mar Apr
May Jun Jul Aug
Sep Oct Nov Dec
Year

History

PSD VI (2003)



- MAPS
- 3D →
- Diamond
- MSGCs

Strips/Pixel

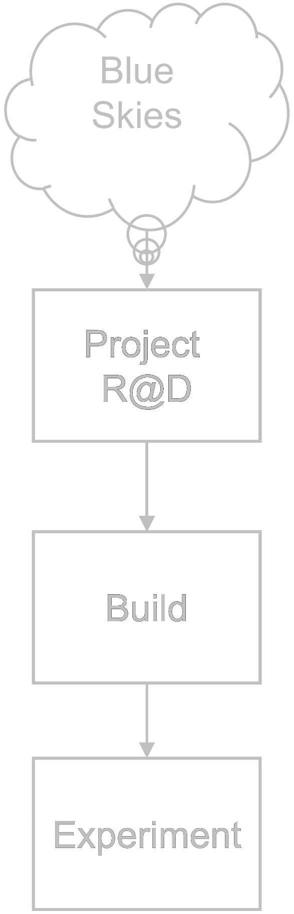
- ATLAS
- CMS

- Gas (HERA-B)

Strips

- CDF
- D0

PSD VII (2005)



- n$^+$p
- MAPS
- 3D
- Diamond

- CMOS

Strips/Pixel

- ALICE
- ATLAS
- CMS
- LHCb

Strips

- CDF
- D0

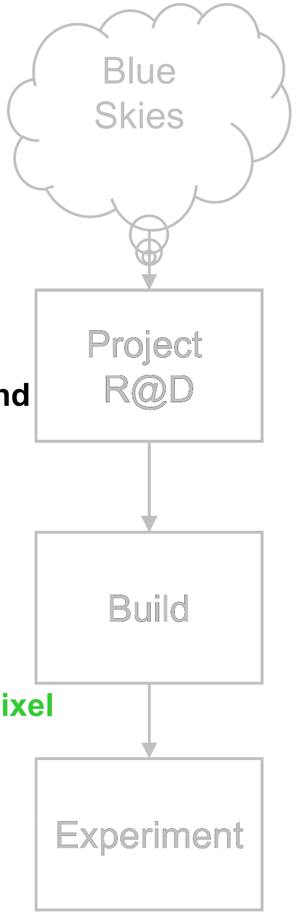
PSD VIII (2008)

- MAPS
- 3D
- Diamond
- CMOS

- n$^+$p LHCb

Strips/Pixel

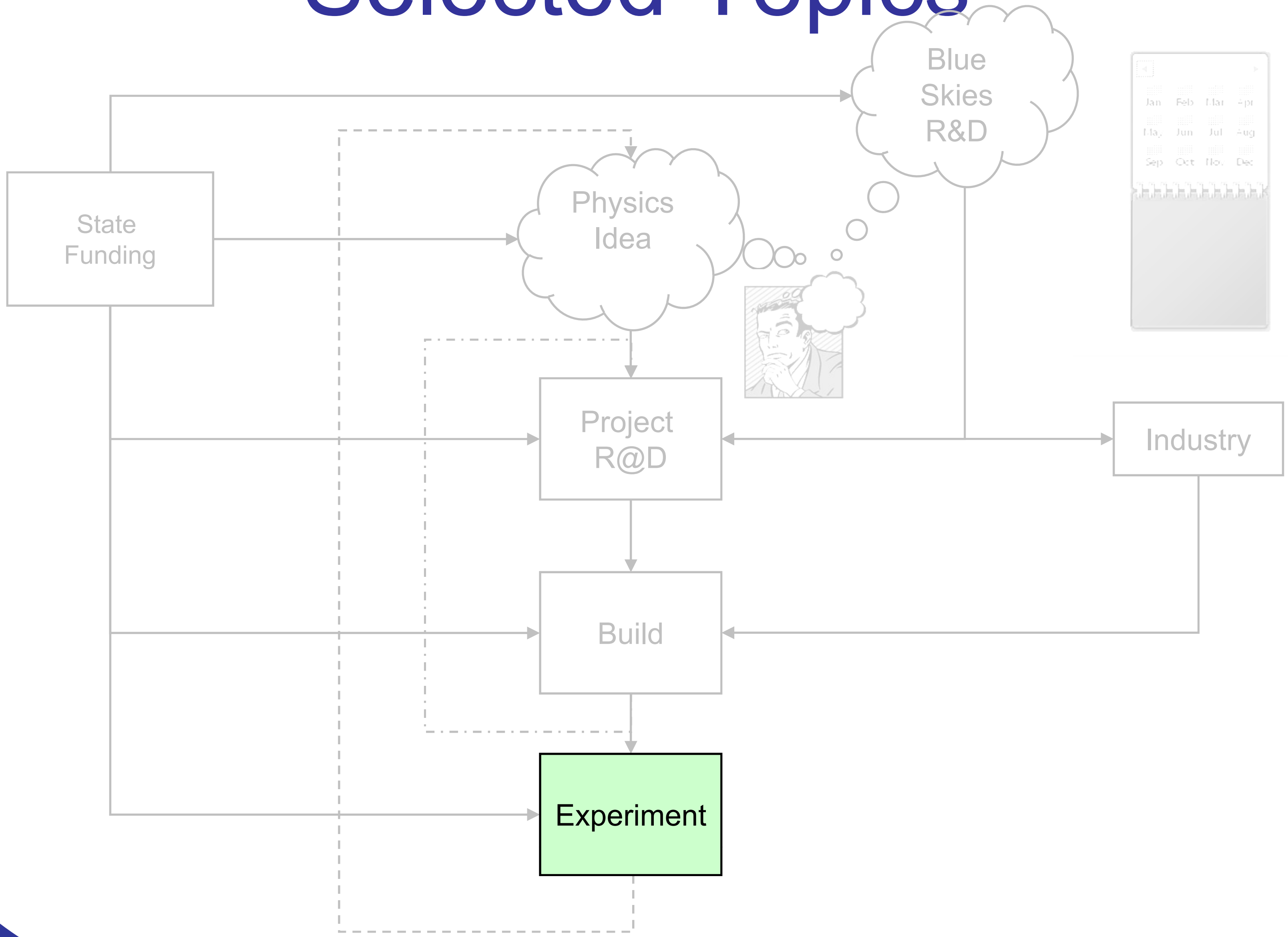
- ALICE
- ATLAS
- CMS
- LHCb



Particle Physics - Last 5 years

- Increasing concentration on solid state detectors
  - In PP less gas
- More emphasis on pixels (over strips)
  - strips → engineering issues
- Progress on radiation hard Si
- Maturing of many technologies
  - Diamond
- Large progress
  - CMOS

Selected Topics



Blue Skies R&D

State Funding

Physics Idea

Project R@D

Industry

Build

Experiment

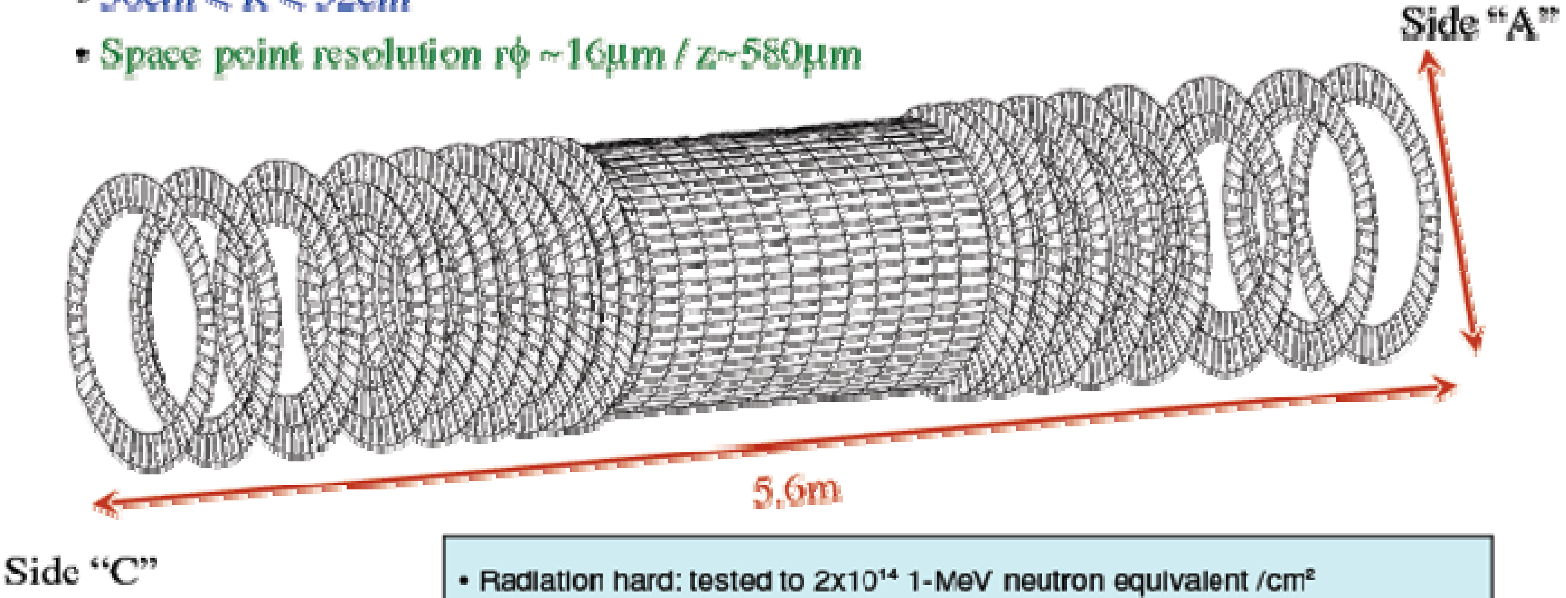
News from LHC

- PSD’s figure highly in recent developments (see Chris Parkes’ talk on opening day)
- Commissioning
  - Cosmic Rays
  - Synchronization tests
  - Building up to criculating beam (10th Sept)

ATLAS

Atlas SemiConductor Tracker in numbers:

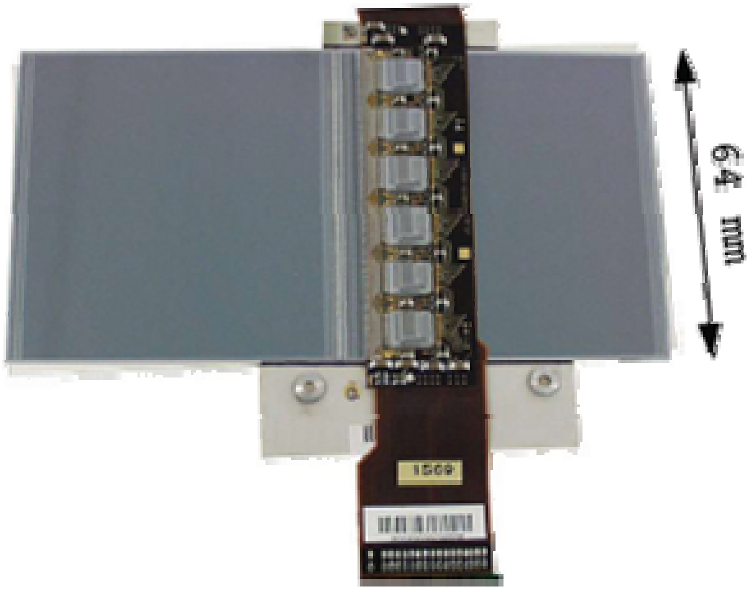
- 61 m^2 of silicon, 6.2 million readout channels
- 4088 silicon modules, arranged to form 4 Barrel layers and 18 Disks (9 each end)
- Barrel : 2112 modules (1 type) giving coverage $|\eta| < 1.1$ to 1.4
- End-caps : 1976 modules (4 types) with coverage 1.1 to $1.4 < |\eta| < 2.5$
- $30cm < R < 52cm$
- Space point resolution $r\phi \sim 16\mu m$ / $z \sim 580\mu m$



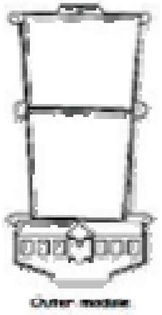
- Radiation hard: tested to 2×10^{14} 1-MeV neutron equivalent /cm^2
- Lightweight: 3% X0 per layer
- Global collaboration by 32 institutes

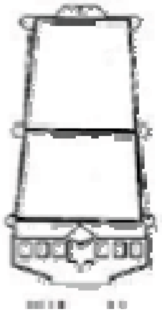
ATLAS MODULES

- Single-sided *p*-implanted strips on *n*-type *Si*
- Back-to-back sensors, glued to highly thermally conductive substrates for mechanical/thermal stability
- 40mrad stereo angle between sensors
- 1536 channels (768 on each side), 6 chips/side
- Binary readout
- Optical communication to DAQ
- 5.6W/module (rising to ~10W after 10 years LHC)
- up to 500V sensor bias
- Cooled to -8°C to limit sensor radiation damage



- 2112 barrel modules
- one shape
- assembled at 4 SCT sites

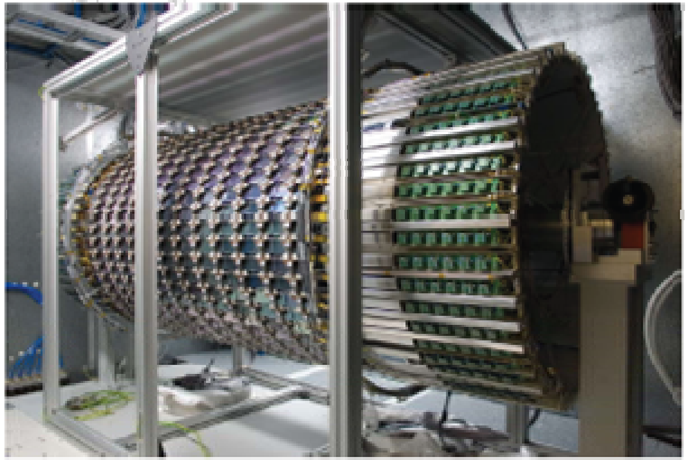


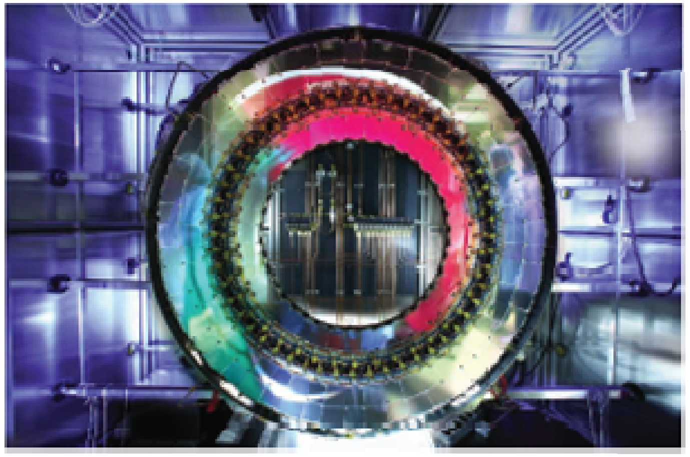


- 1976 endcap modules
- 3 shapes
- assembled at 7 SCT sites

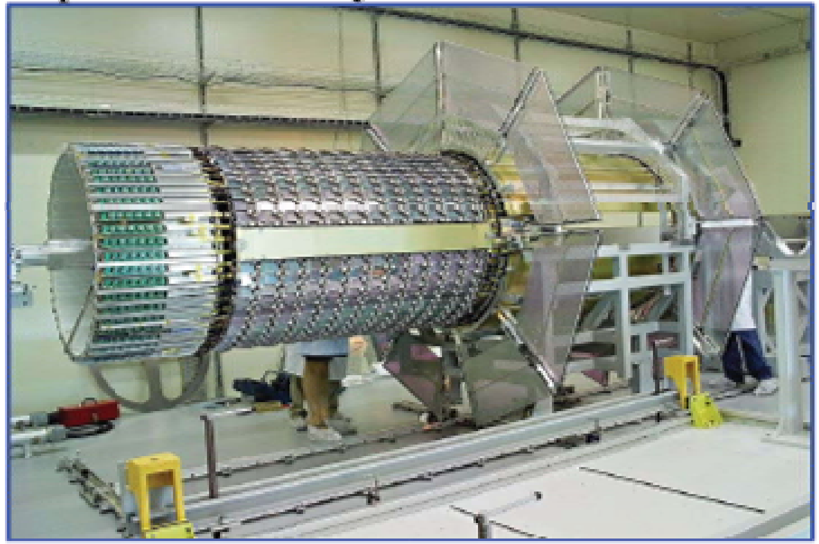
ATLAS

Single cylinder tests



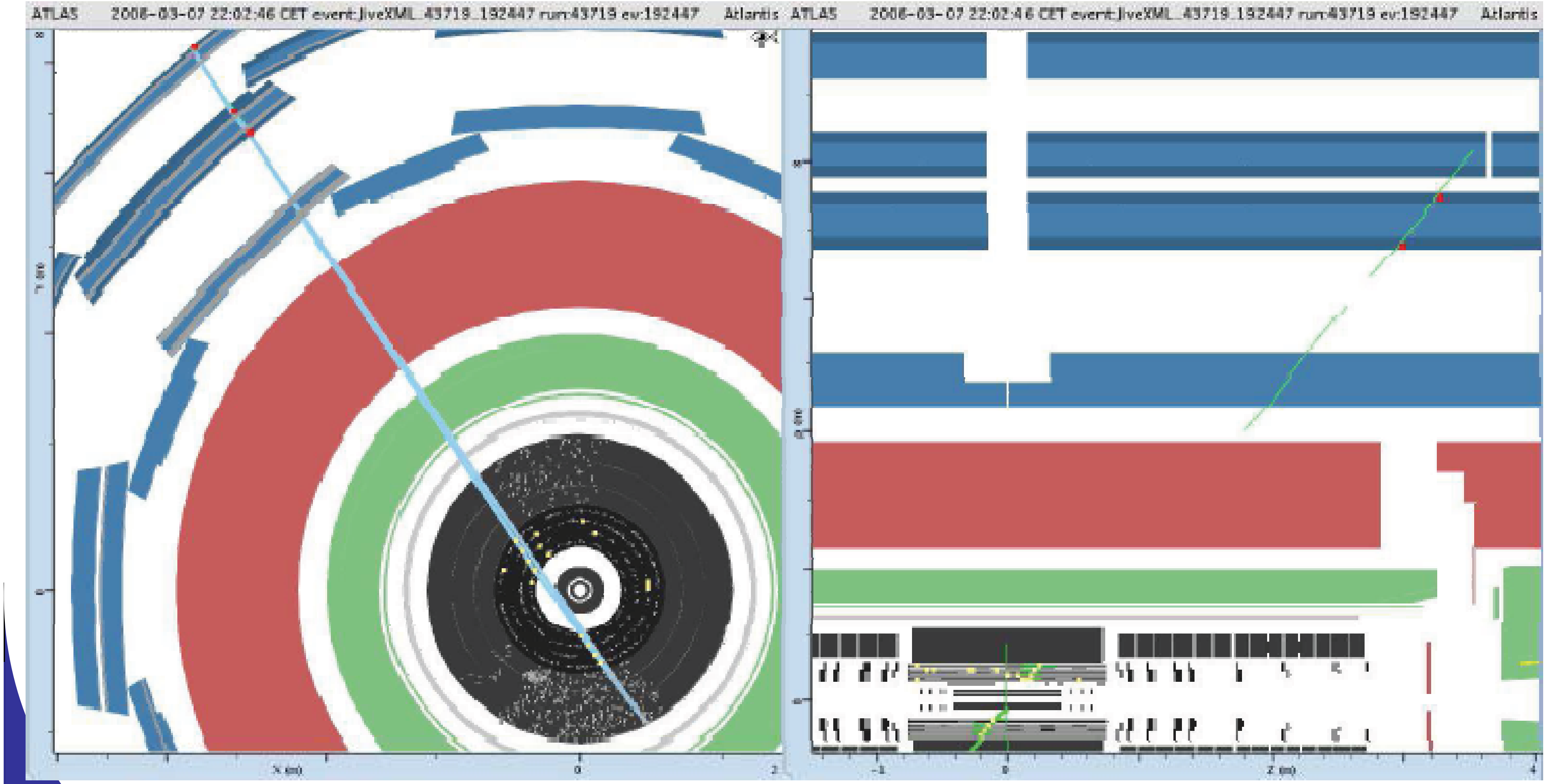


Sept. 2005: outer layer in thermal enclosure



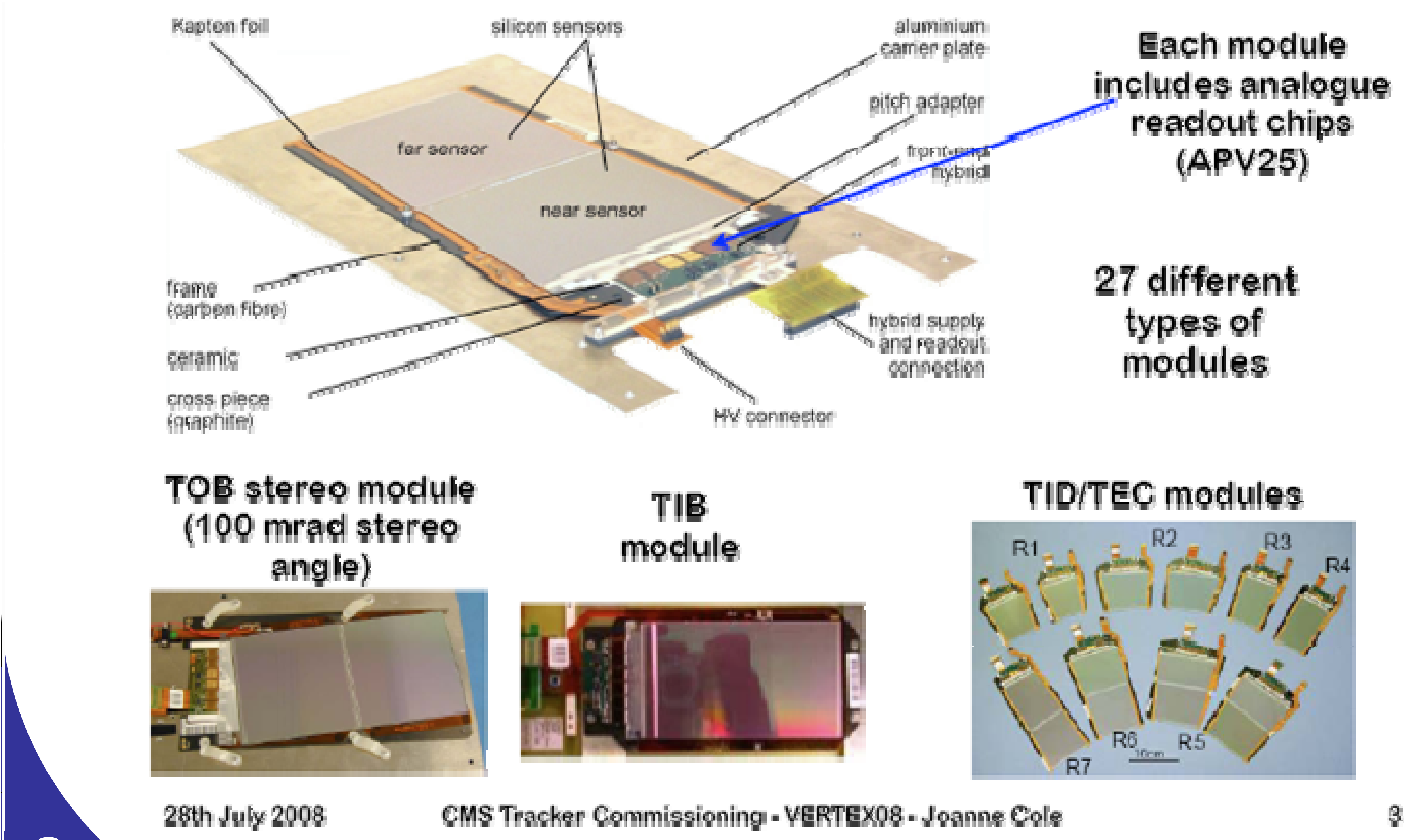
Dec. 2006: inner layer insertion

LHC Experiment Commissioning



Early 2008:Cosmics observed
in all LHC experiments

CMS modules



Each module includes analogue readout chips (APV25)

27 different types of modules

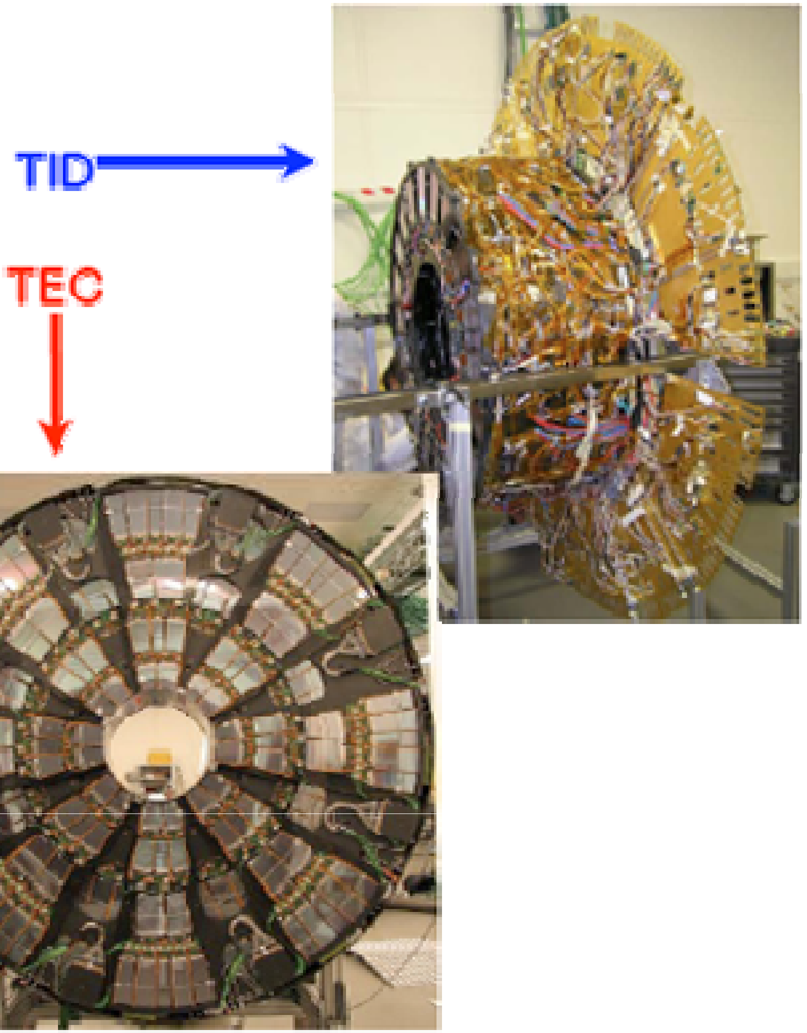
TOB stereo module (100 mrad stereo angle)

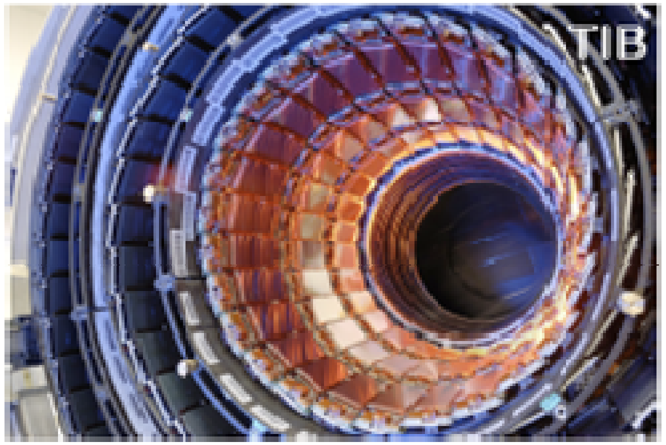
TIB module

TID/TEC modules

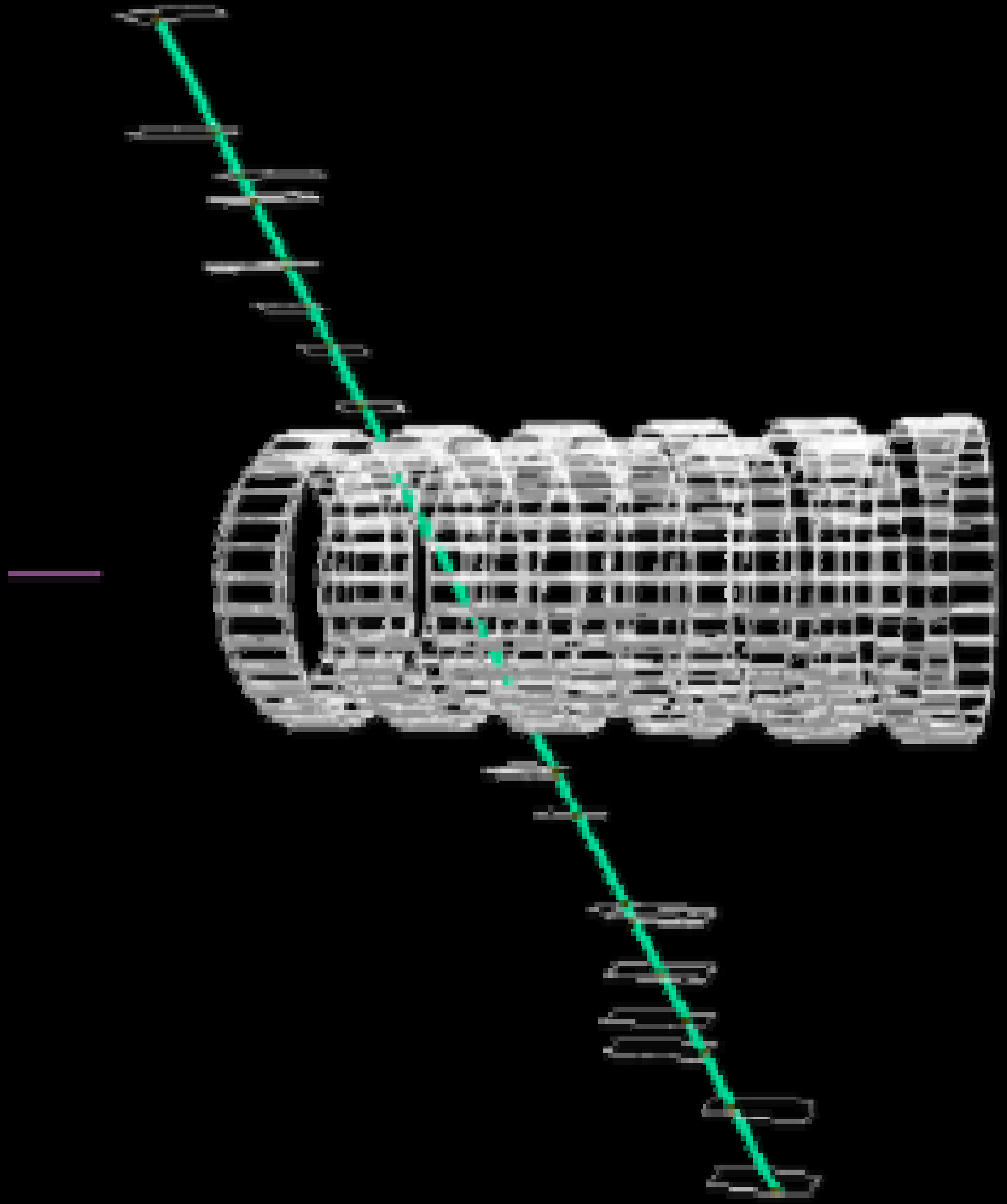
28th July 2008 CMS Tracker Commissioning - VERTEX08 - Joanne Cole 3

CMS

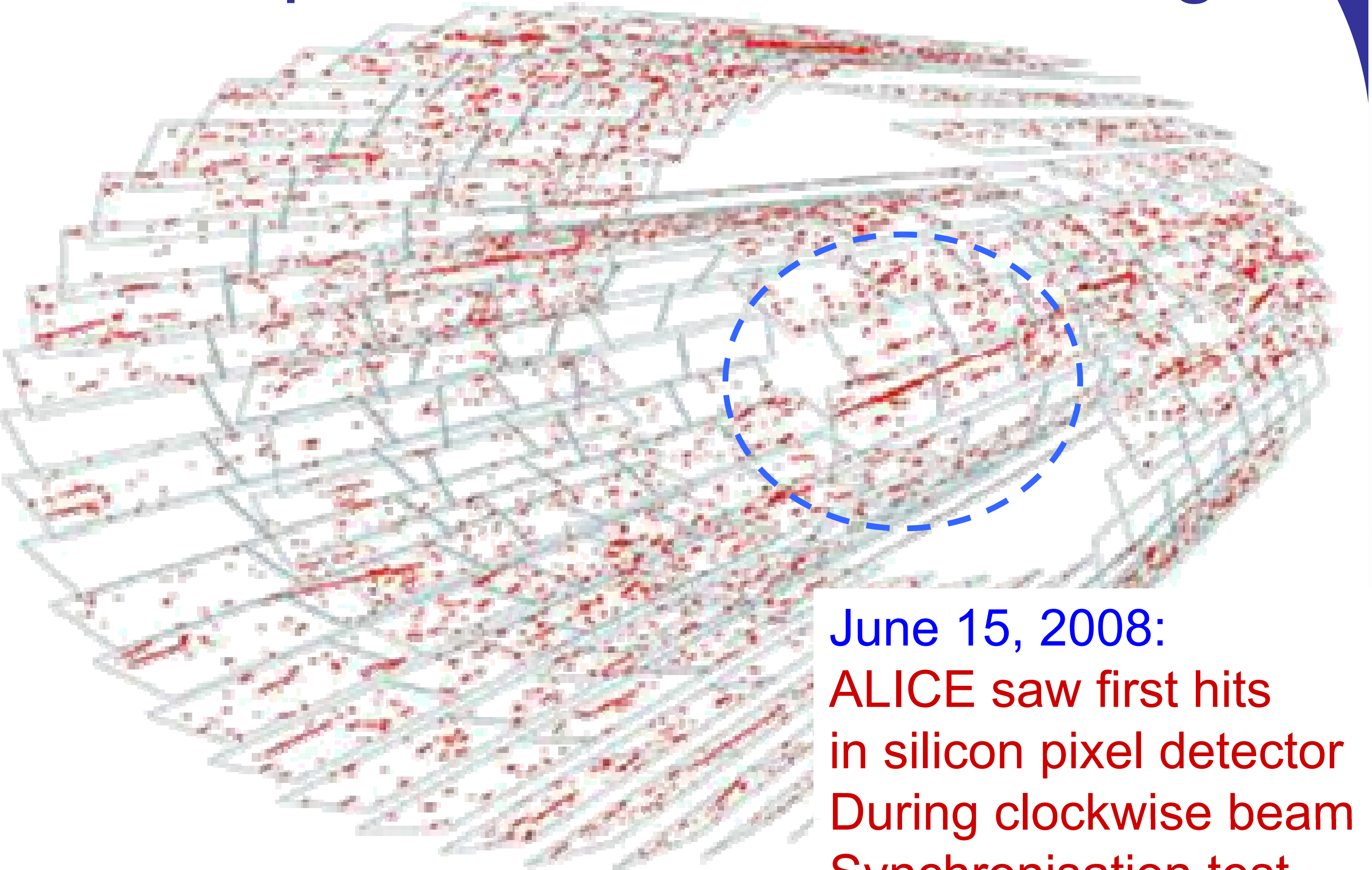




CMS

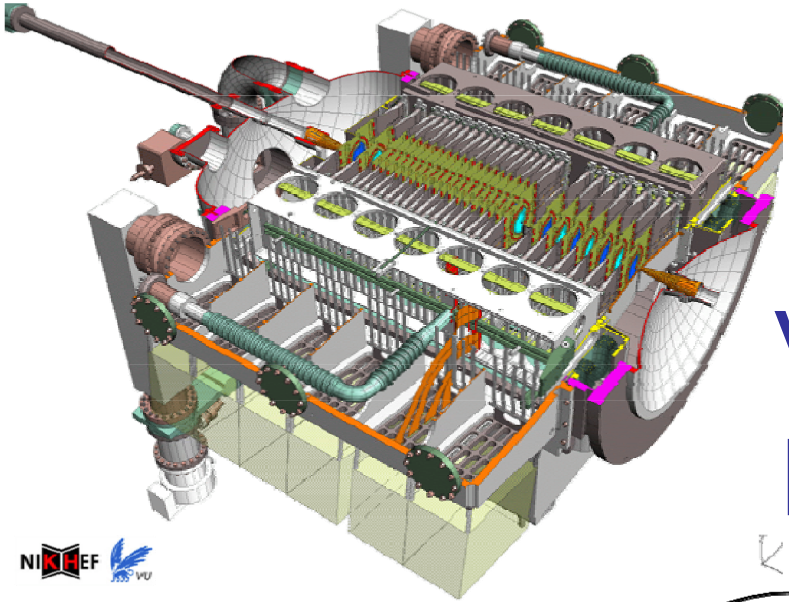


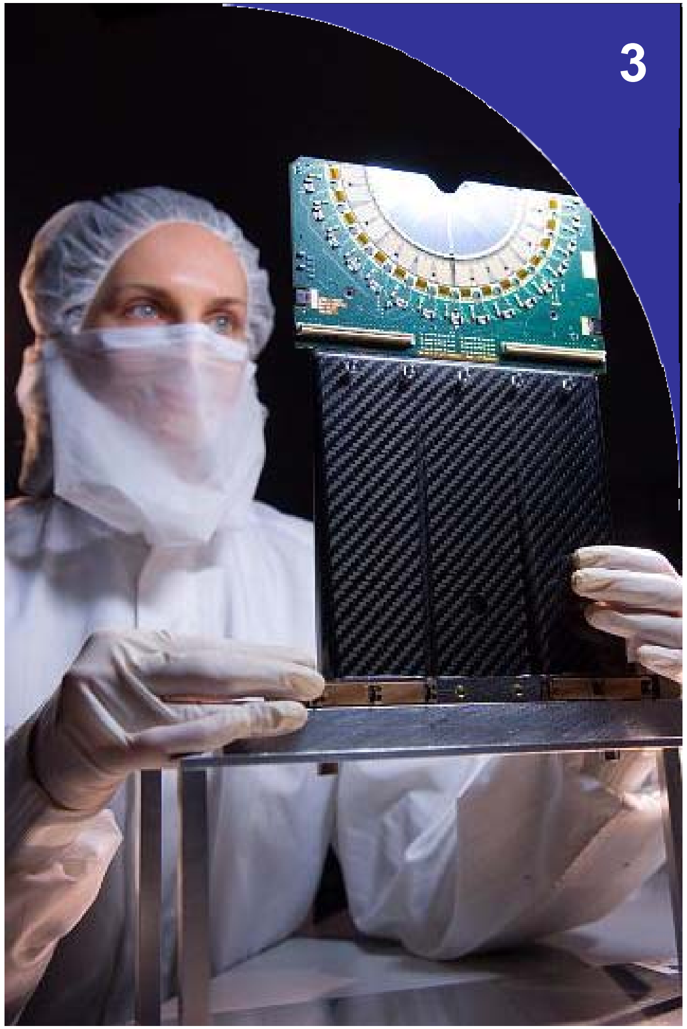
LHC Experiment Commissioning

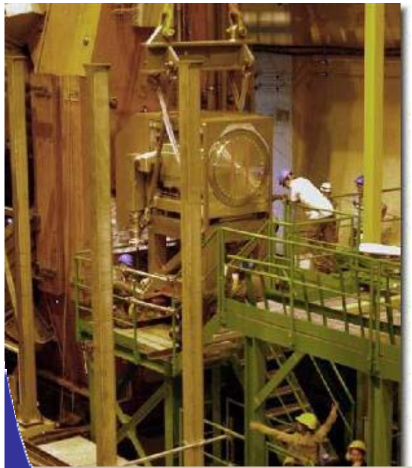


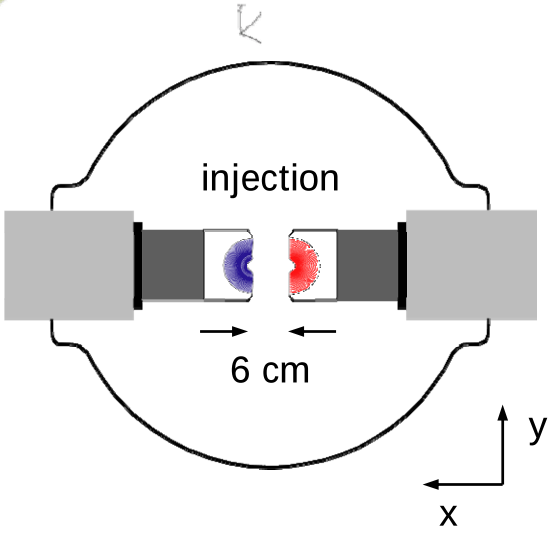
June 15, 2008:
ALICE saw first hits
in silicon pixel detector
During clockwise beam
Synchronisation test

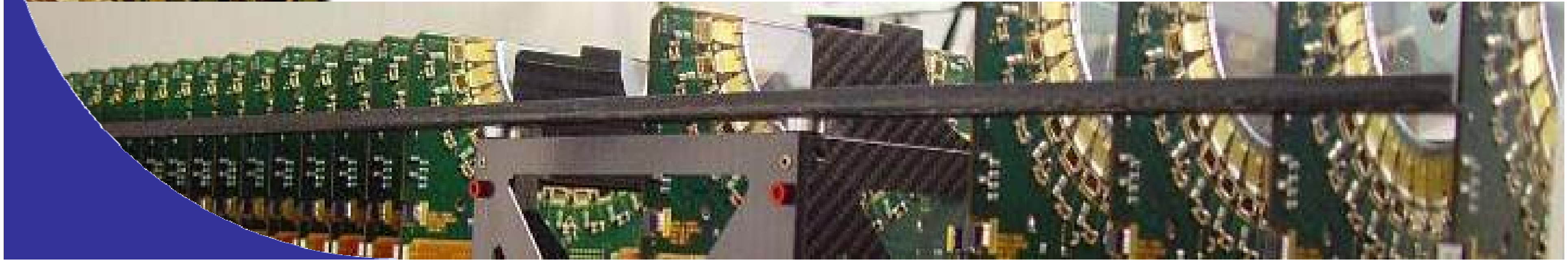
VELO LHCb



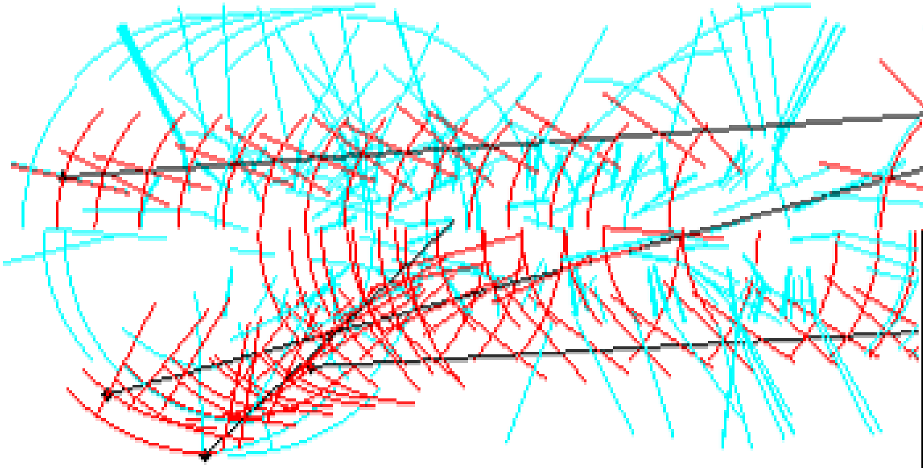




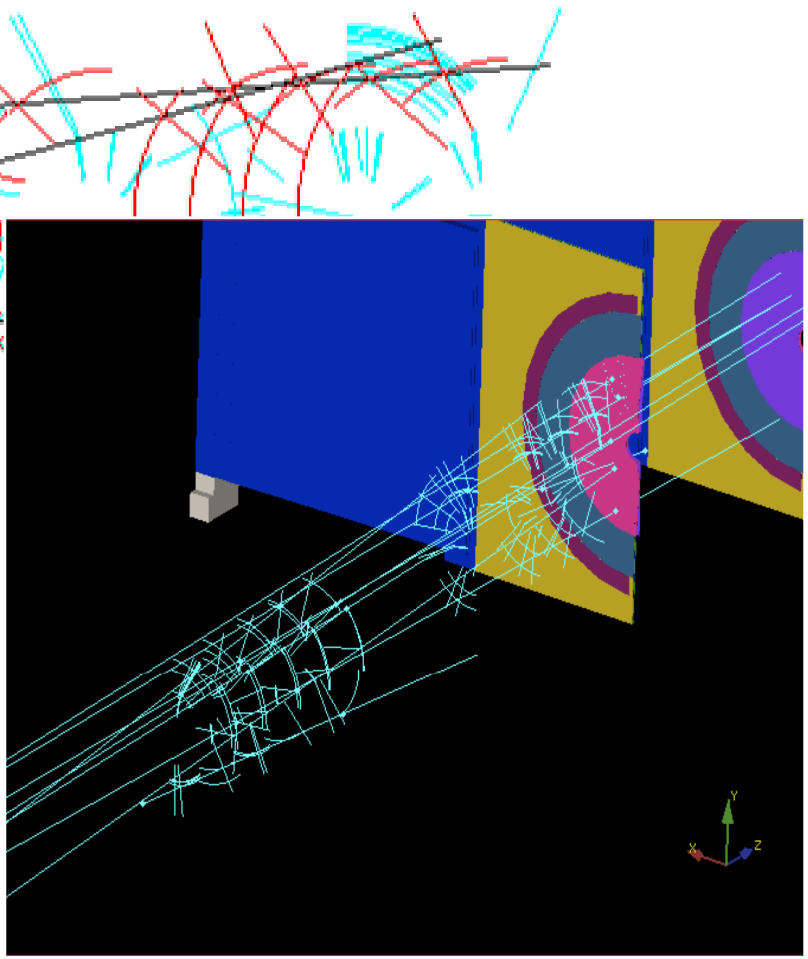




22nd August



Reconstructed tracks!

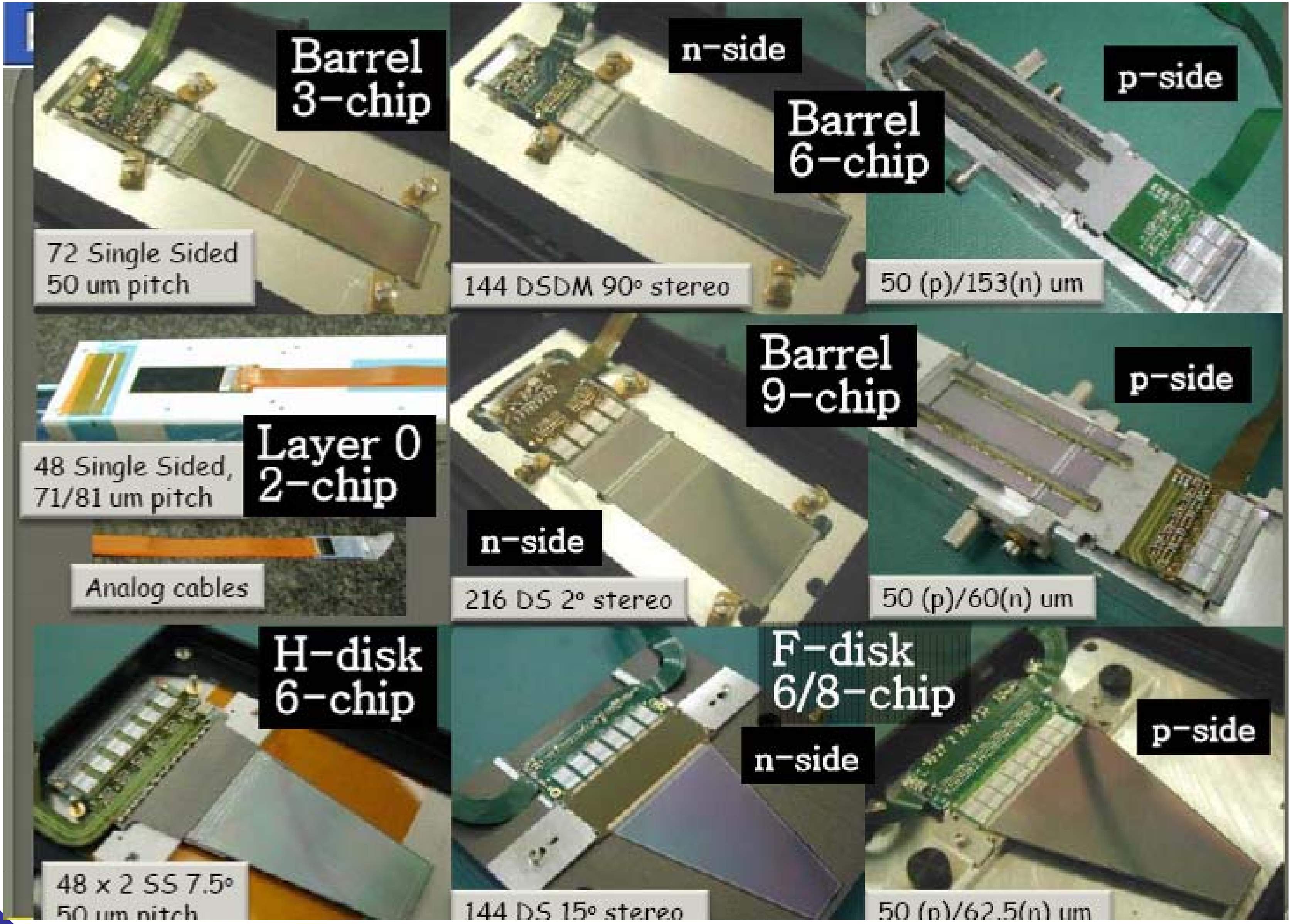


In a few weeks…

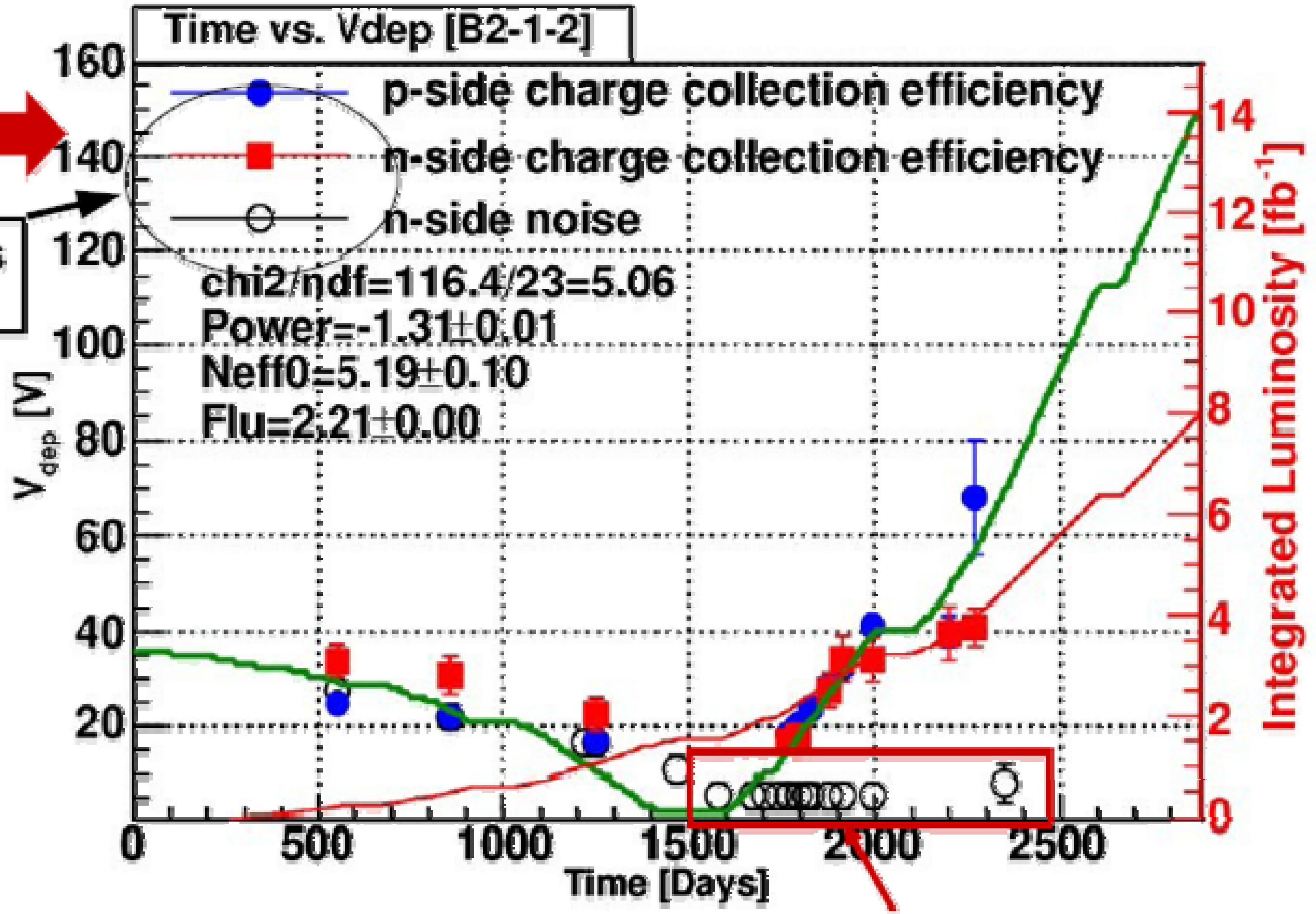
- Real tracks and vertices from the next generation of detectors (See the next PSD!)

Other experiments

- D0


Barrel
3-chip
72 Single Sided
50 um pitch
n-side
Barrel
6-chip
144 DSDM 90° stereo
p-side
50 (p)/153(n) um
48 Single Sided,
71/81 um pitch
Layer 0
2-chip
Analog cables
Barrel
9-chip
n-side
216 DS 2° stereo
p-side
50 (p)/60(n) um
H-disk
6-chip
48 x 2 SS 7.5°
50 um pitch
F-disk
6/8-chip
n-side
144 DS 15° stereo
p-side
50 (p)/62.5(n) um

Type Inversion

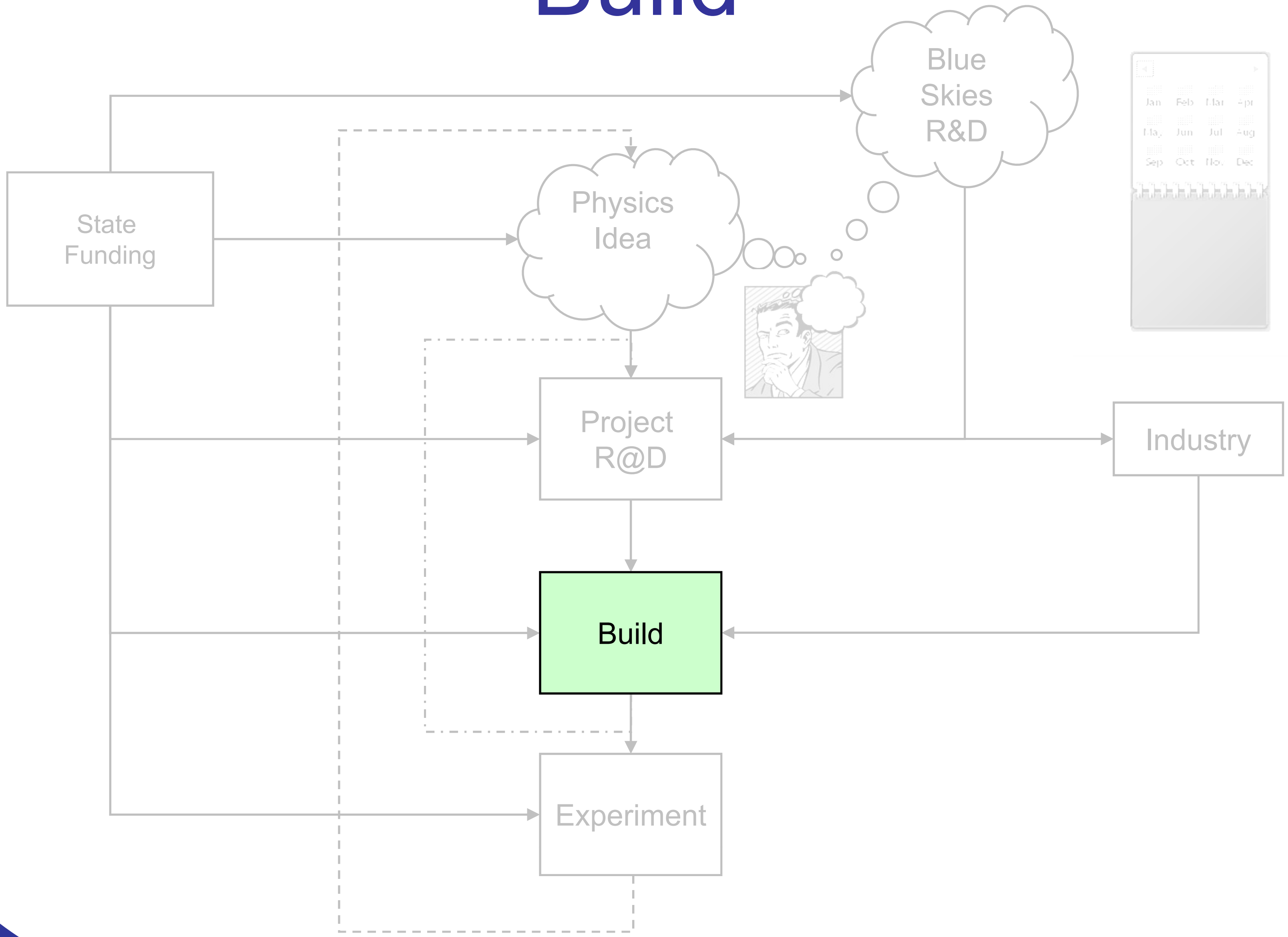


HV Limit

Simultaneous fit to all data

Exclude n-side noise from fit after type inversion

Build



State Funding

Physics Idea

Blue Skies R&D

Project R@D

Industry

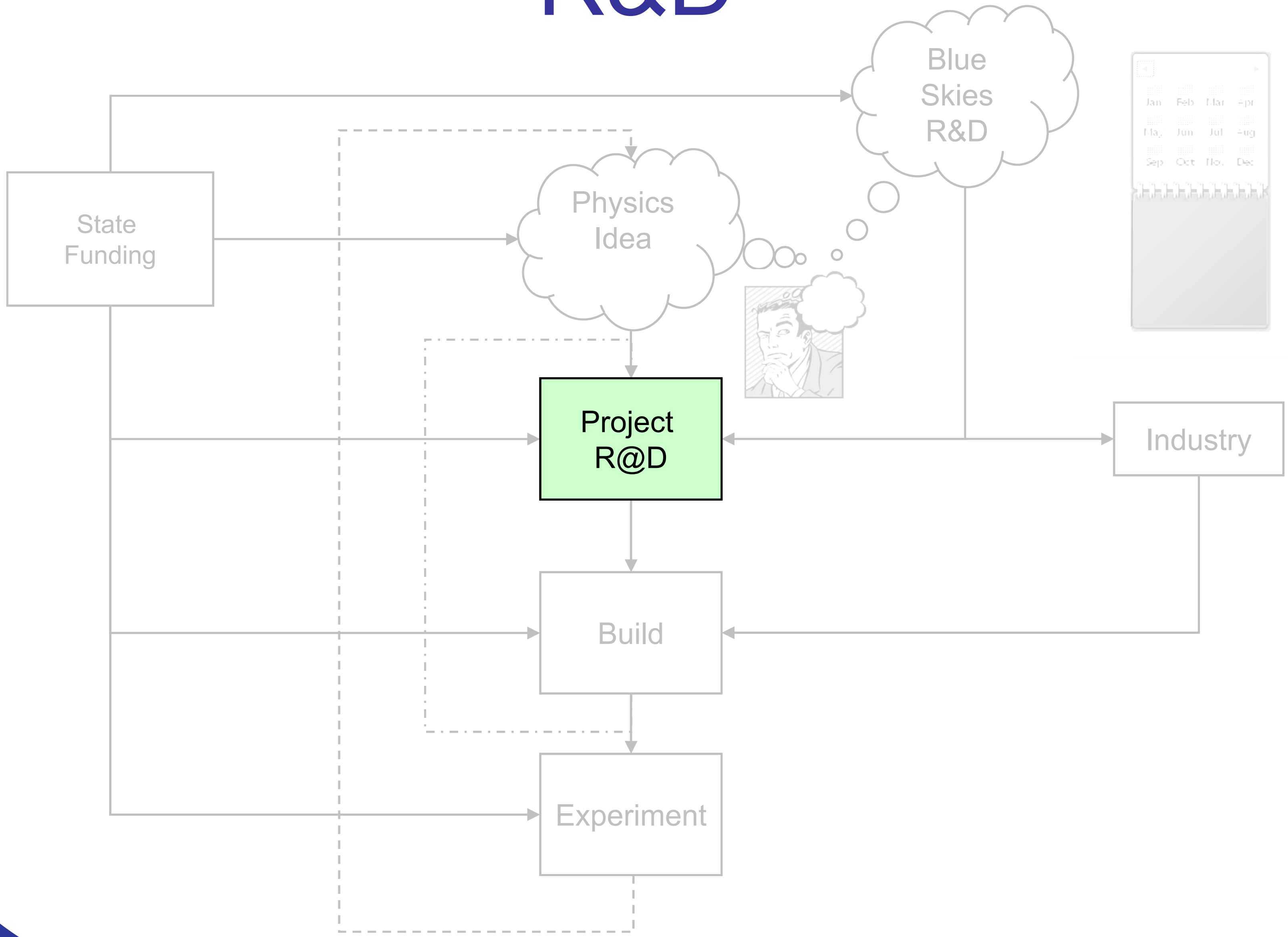
Build

Experiment

Build

- The effort to get the CERN experiments ready dominated the last few years
  - A few builds still in progress
    - E.g. LHCb “spare” VELO using n^+p technlogy

R&D



Blue Skies R&D

State Funding

Physics Idea

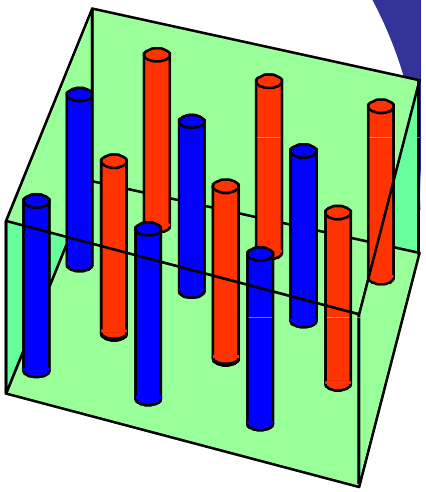
Project R@D

Industry

Build

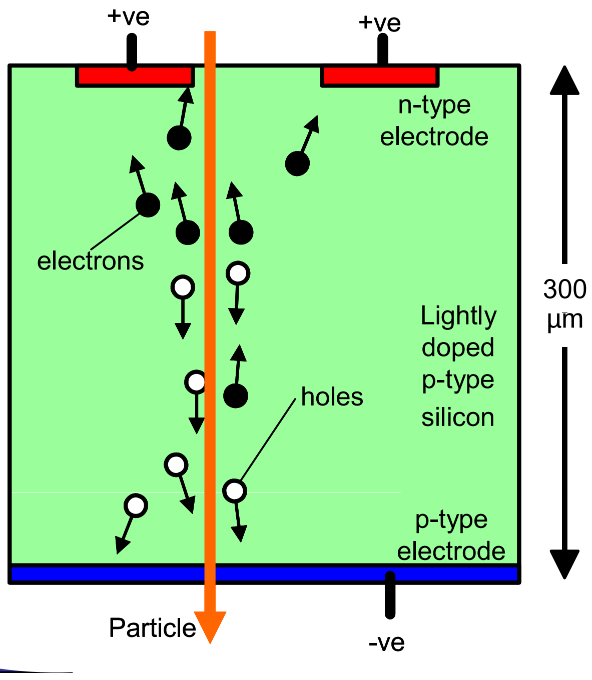
Experiment

3D

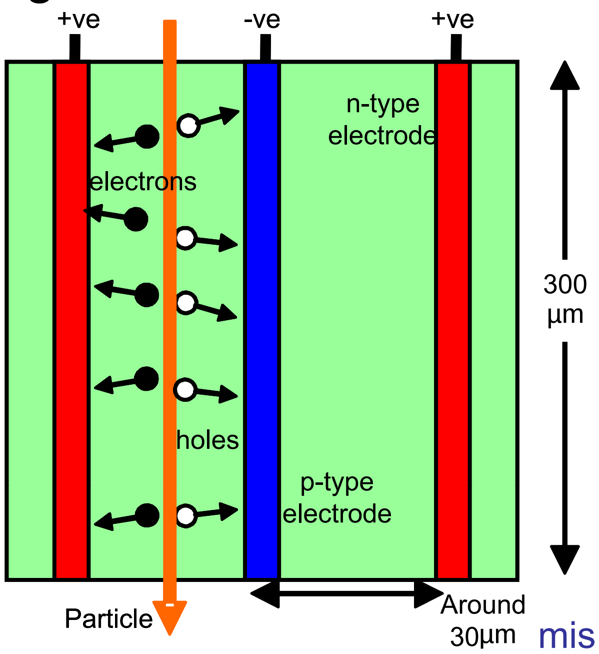


- Array of electrode columns passing through substrate
- Electrode spacing << wafer thickness (e.g. 30µm:300µm)
- Benefits
  - $V_{depletion} \propto (\text{Electrode spacing})^2$
  - Collection time $\propto$ Electrode spacing
  - Reduced charge sharing
- More complicated fabrication - micromachining

Planar

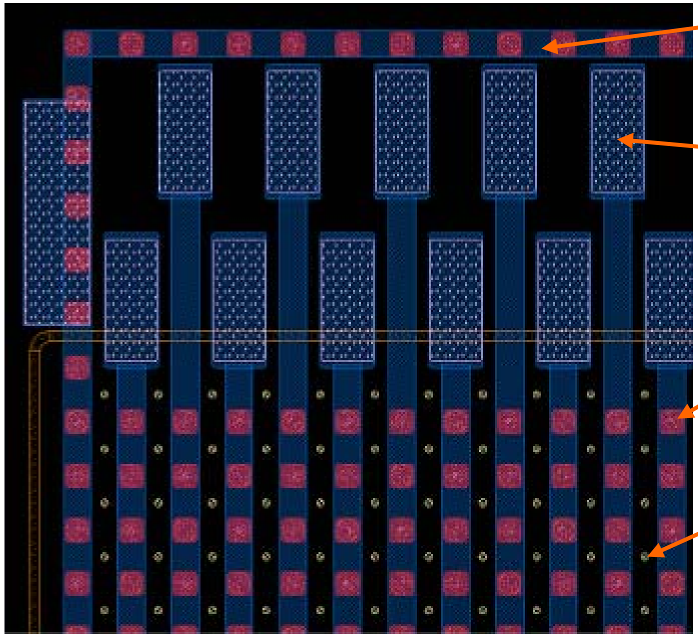


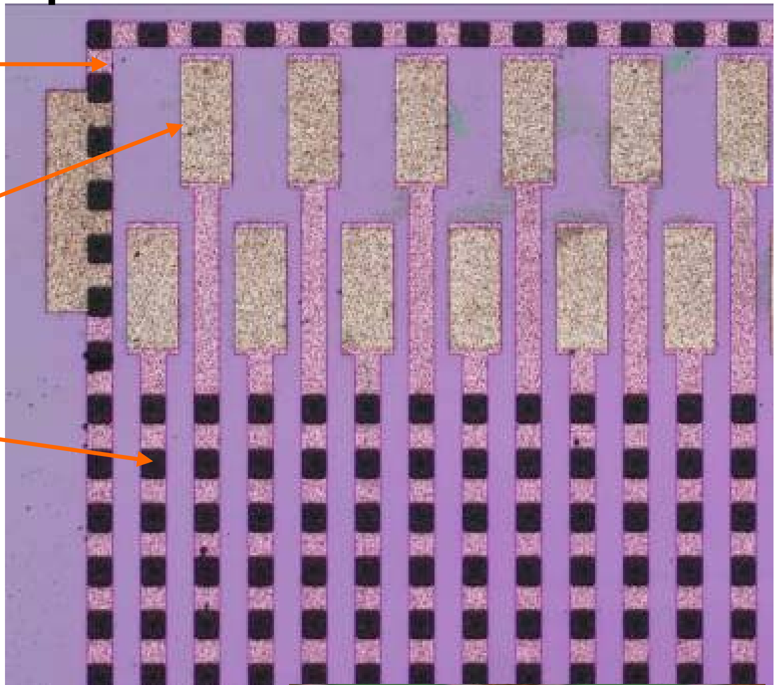
3D



Finished 3D devices

Typical device layout – Strip detector, 80µm pitch





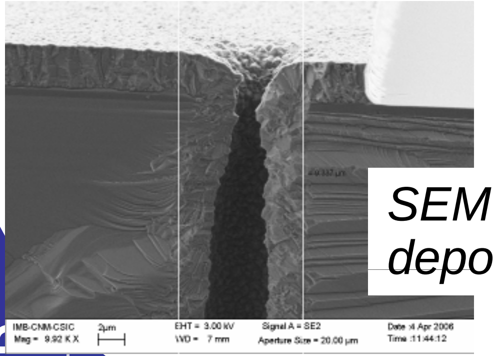
3D guard ring

Bond pads

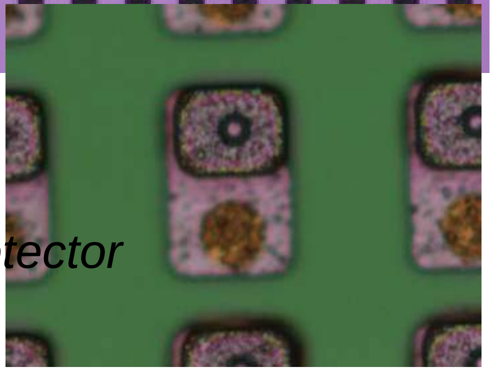
Collecting electrodes

Bias electrodes (back surface)

80µm



SEM after polysilicon deposition and etching

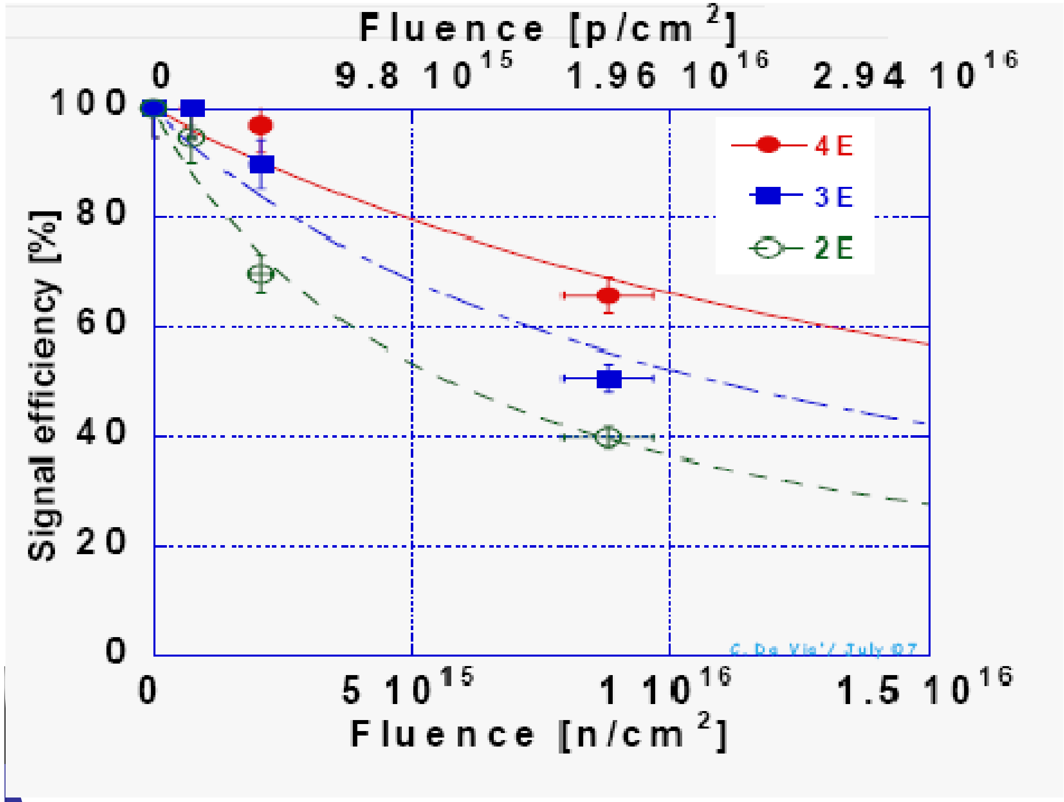


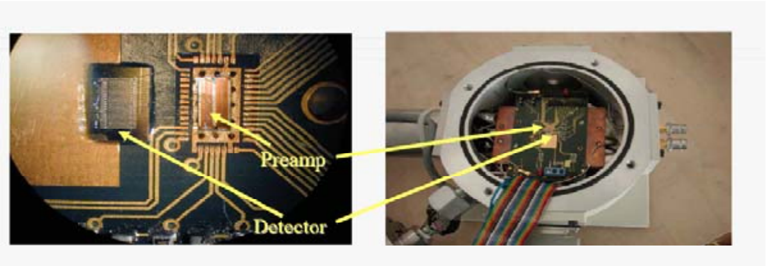
Pixel on Medipix detector

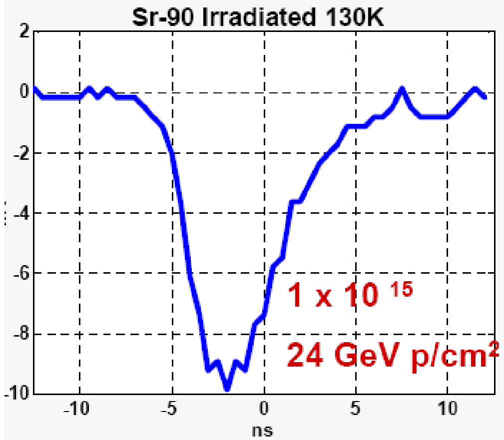
Hawaii/Stanford/Manchester cont..

Stanford fabricated devices

- •Fast timing applications
- •FP220 in ATLAS trigger





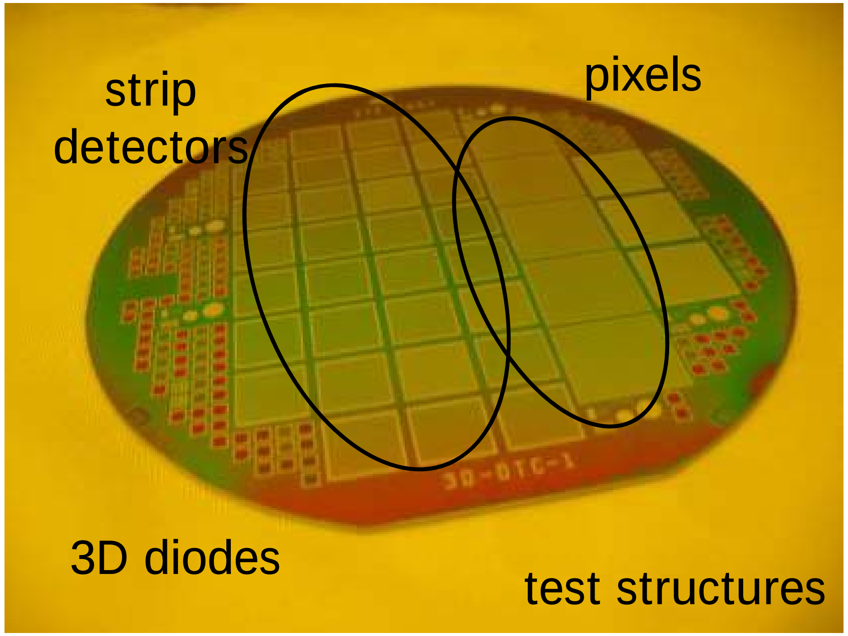


130K, RT 1.5ns
After irradiation

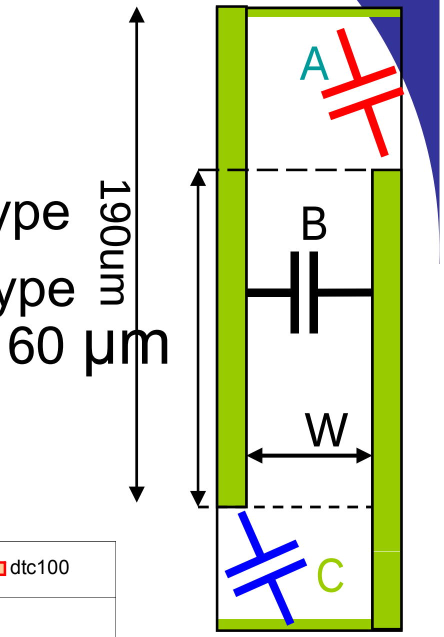
- •Most advanced radiation results
- •Results for different pixel configurations

FBK (Trento)

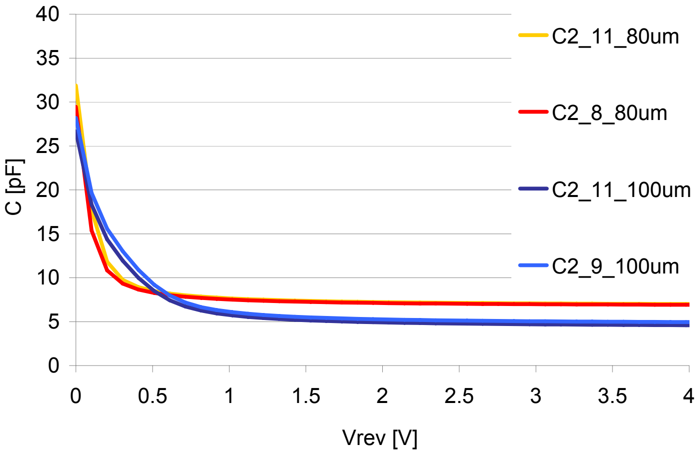
Maurizio Boscardin *et al.*

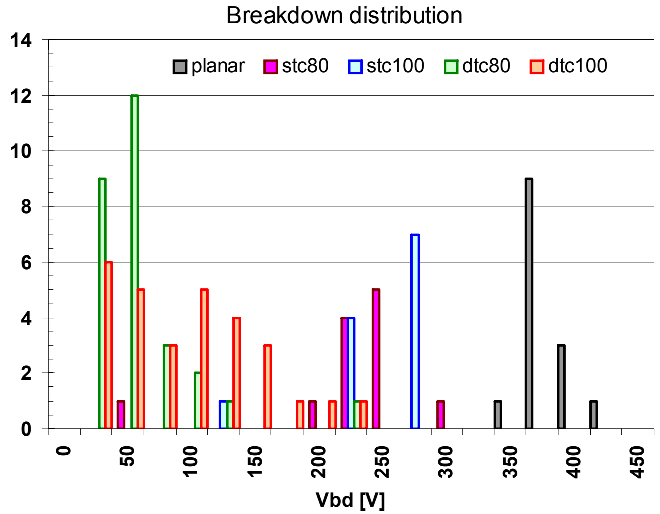


- Single Sided Single Type
- Double sided double type
  - First batch made
  - Depleted **2V**
  - Some devices



Double sided double type





Tested in CMS testbeam last week

Panja Luukka, Helsinki, Uli Parzefall, Freiburg

3D Summary

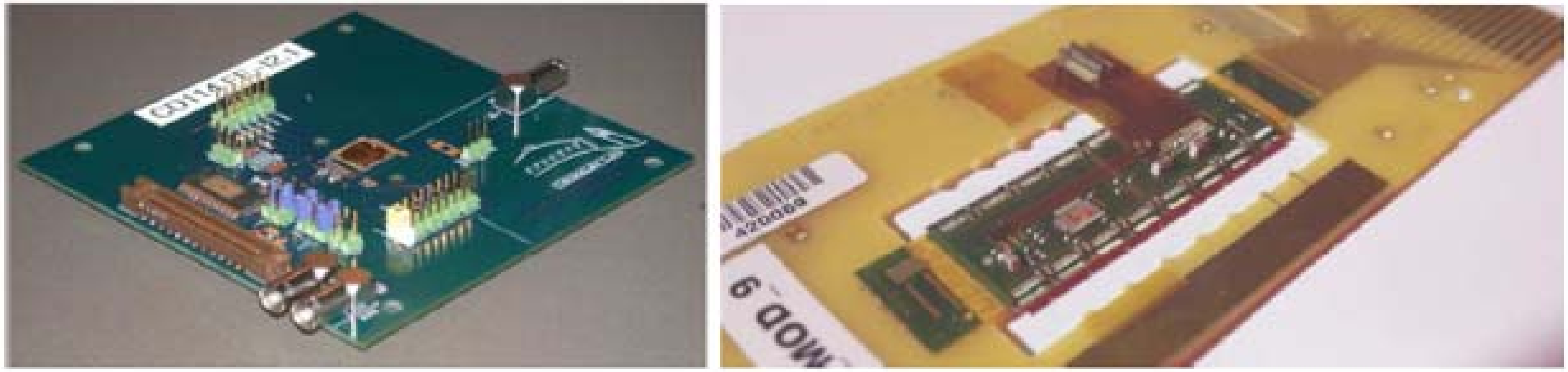
- 2008: the year 3D moved from hand-crafted to IKEA-rised ?
  - – Double sided 3D detectors
  - – (semi) commercial fabrication

- 3D strip detectors
- 3D pixel detectors

- **rad hard:** mm to cm from SLHC beam
- Reduced charge sharing, edgeless

Diamond

ATLAS diamond pixel modules



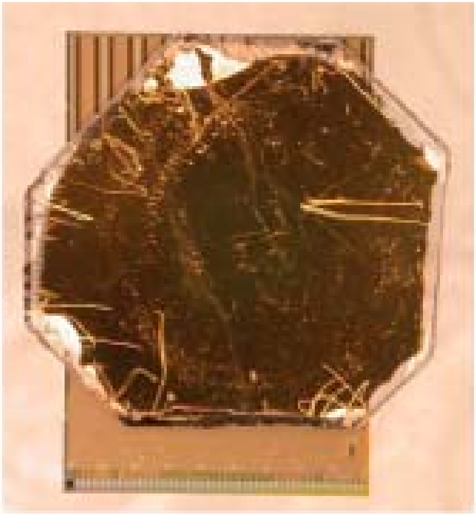
- Single chip and full modules bump-bonded at IZM (Berlin), constructed and tested in Bonn
- Operating parameters: Noise 140e,Threshold 1450-1550e, Threshold Spread 25e, Overdrive 800e

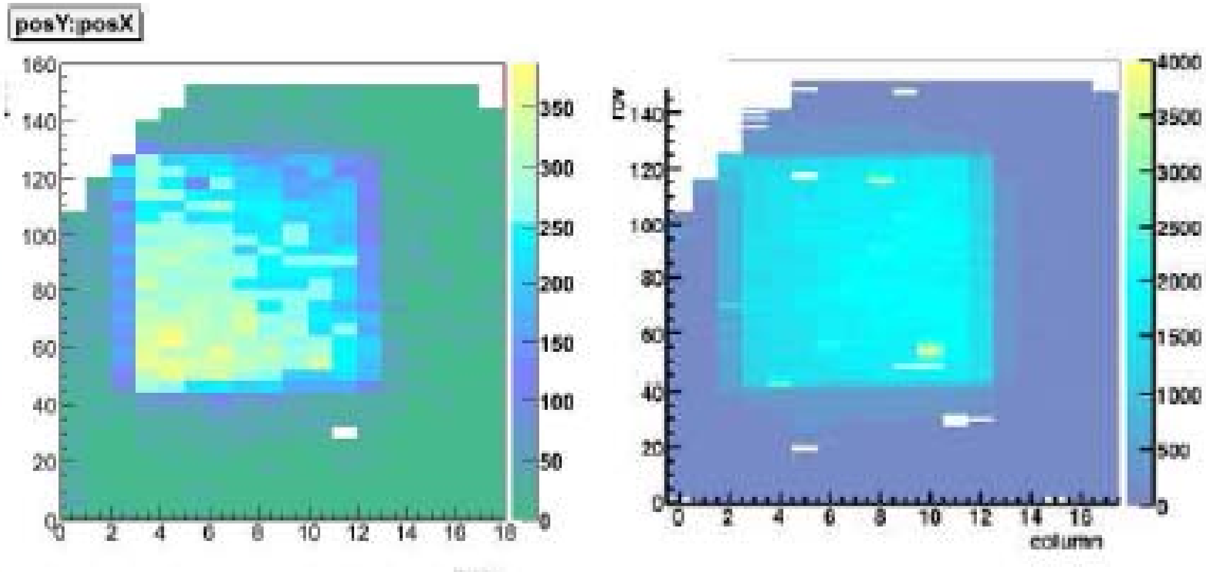
Diamonds

- Further Progress in Charge Collection
    - 300 μm collection distance diamond attained in wafer growth
    - FWHM/MP $\sim$ 0.95 – Working with manufacturers to increase uniformity
    - scCVD - Full charge collection, fast, large signals, Getting larger?
    - New manufacturers
- Radiation Hardness of Diamond Trackers
    - Using trackers allows a correlation between S/N and Resolution
    - With Protons:
        - Dark current decreases with fluence
        - E=1V/μm: 15% S/N loss at $2.2 \times 10^{15}/\mathrm{cm}^2$, 33% signal at $1.8 \times 10^{16}/\mathrm{cm}^2$
        - pCVD and scCVD have same damage curve
- Diamond Pixel Detectors
    - Successfully tested a complete ATLAS module and scCVD module
        - Excellent correlation for both between telescope and pixel data - stable op
    - Diamond R&D Approved by ATLAS for LHC Upgrade R&D
- Beam Conditions Monitoring

scCVD pixel

The First scCVD ATLAS diamond pixel detector

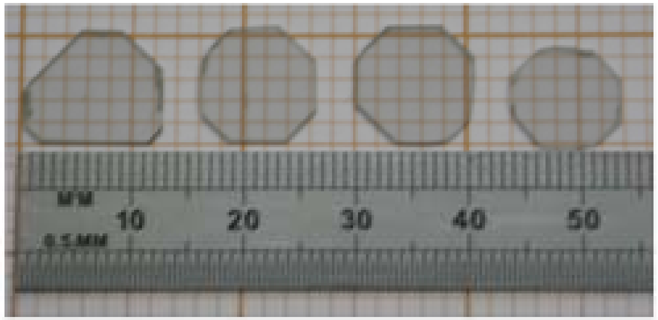




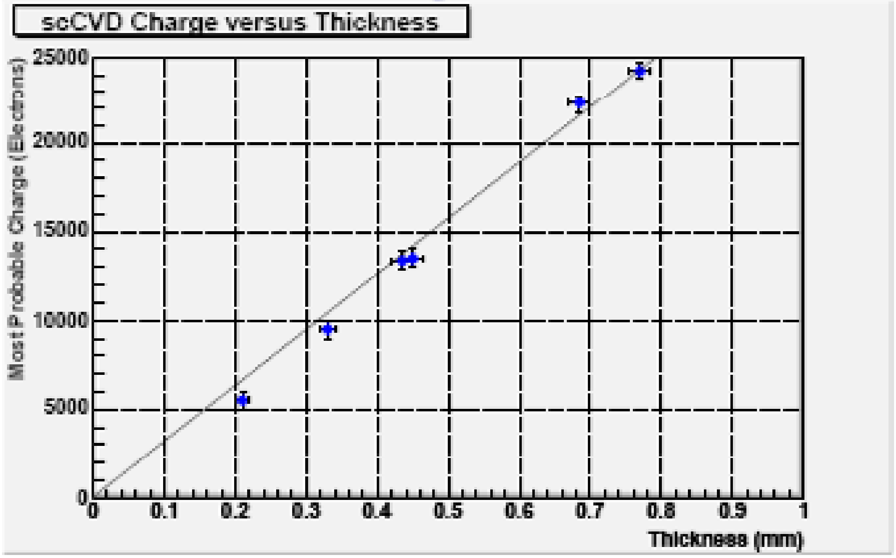
- The hitmap plotted for all scintillation triggers with trigger in telescope.
- The raw hitmap looks goods - $\sim$ 1 dead pixel

Material Status - Single Crystal CVD Diamond

Recent Single Crystal CVD Diamond

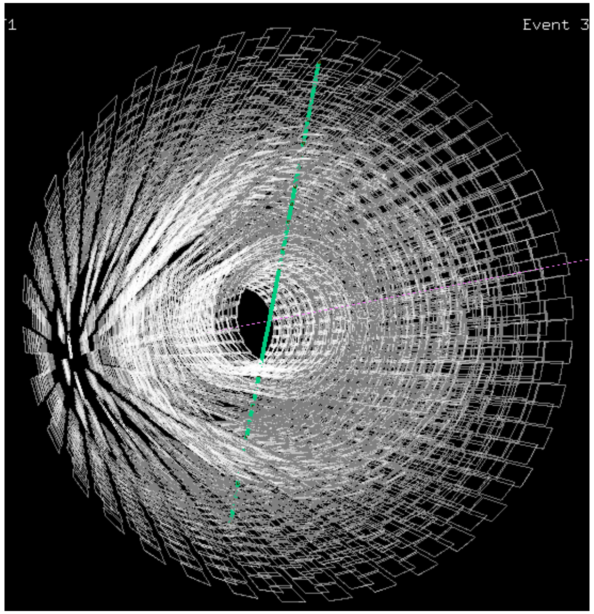


scCVD Diamond Most Probable Charge versus Thickness



- High quality scCVD diamond can collect full charge for thickness 880μm

CMS



Weakest point in present system is amount of material

- Electron & photon conversions
- Hadronic interactions

Future power estimates

- Some extrapolations assuming 0.13µm CMOS
  - Pixels 58µW -> 35µW/pix
    - NB sensor leakage will be significant contribution
  - Outer Tracker: 3600 µW -> 700µW/chan
    - Front end 500µW (M Raymond studies)
    - Links 170µW (including 20% for control)
  - PT layers: 300µW/chan - most uncertain
    - Front end 50µW (generous extrapolation from pixels)
    - Links 100µW (including 20% for control)
    - Digital logic 150µW (remaining from 300µW)
    - 100µm x 2.5mm double layer at R ≈ 25cm => 11kW
- More detailed studies needed
  - sensor contribution not yet carefully evaluated
  - internal power distribution will be a significant overhead

Power delivery

- Perhaps the most crucial question
  - although estimates of power are still imprecise, overall requirements can be estimated
  - we must reduce sensor power with thin sensors
    - finer granularity should allow adequate noise performance
  - and attempt to limit channel count to minimum compatible with tracking requirements (simulations!)
- total readout power expected to be ~25-35kW
  - in same range as present system so larger currents required
- Radical solutions required
  - serial powering or DC-DC conversion
  - neither are proven and many problems remain to be solved

Comment

- Reducing power/pixel/strip is a good feature of reduced processing sizes
- But increasing density of pixels/strips increases the density
  - Supply of power and hence requirement of cooling and minimizing mass is now limiting designs

P-type / ATLAS

- *p*-type detectors most natural solution for *e* collection on segmented side
- n-side read out → lower collection time
- No type inversion
- No backplane processing
- Easier to handle (no need to take care of special gluing on the backside due to the presence of guard-rings. Possibility of operating under-depleted before irradiation)

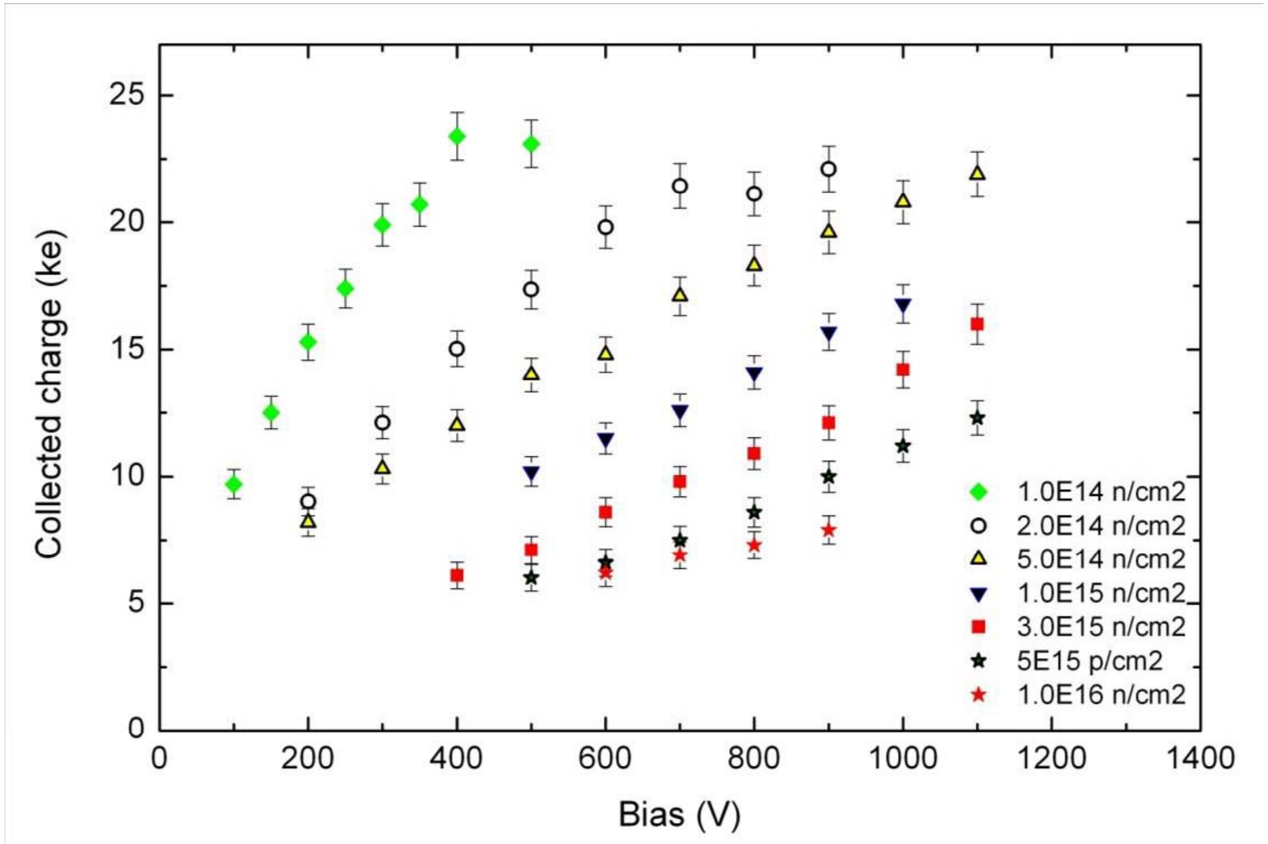
….and, up to 60% discount with respect to n-in-n!

- Thin wafers easier

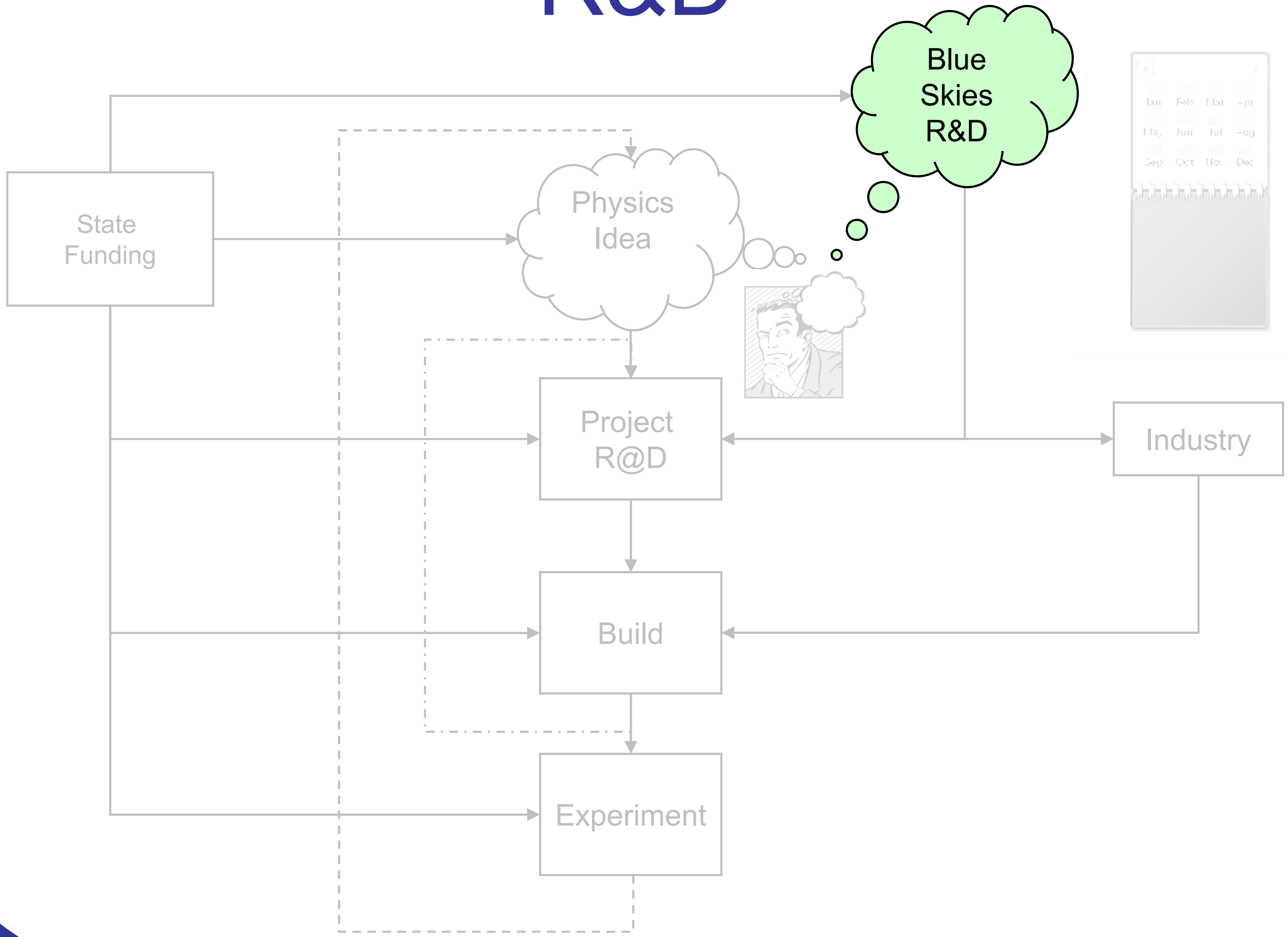
Results

Outstanding results achieved: studies of charge collection of irradiated detectors pushed to 1x10^{16} n cm^{-2}.

Prel. results at 1.5x10^{16} n cm^{-2} available. Significant signal even after these very high doses.



R&D



Blue Skies R&D

State Funding

Physics Idea

Project R@D

Build

Experiment

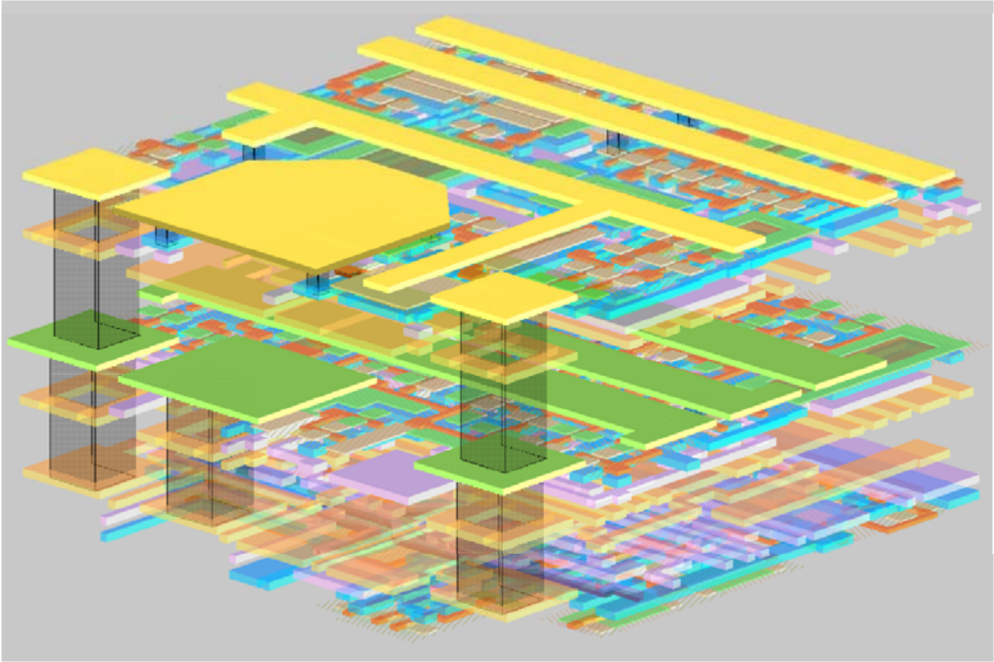
Industry

Driving forces

- Future experiments ILC
  - But also Belle Upgrades
  - Super-B etc
- High resolution
- Low mass
- Radiation tolerance
- Speed

Vertical Integration

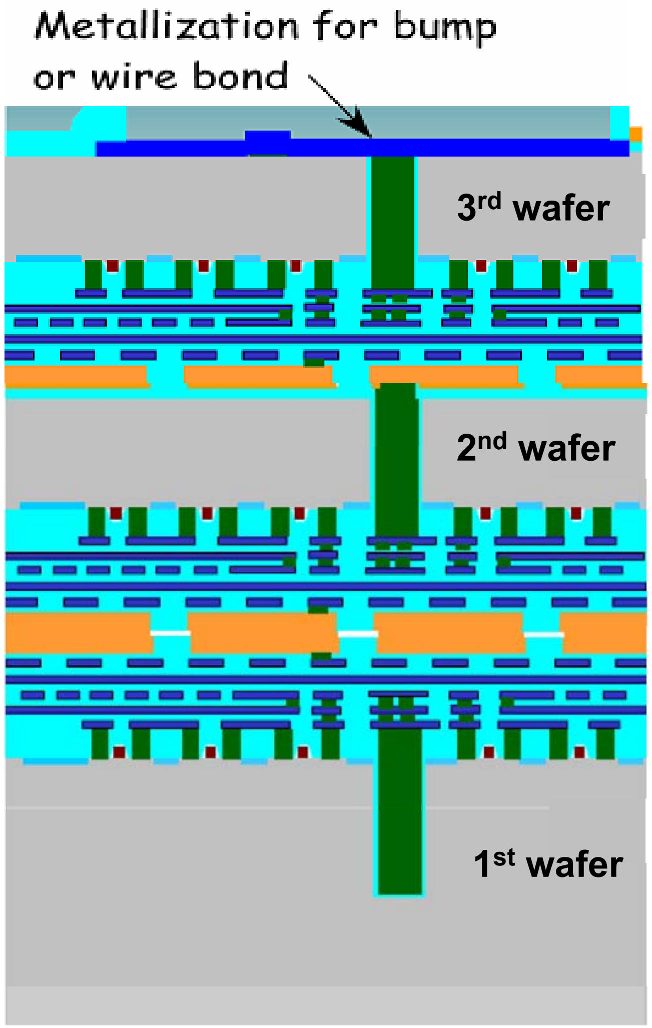
- This has been a “dream” for many years
- More complex detectors, low mass
- Liberate us from bump/wire bonding



3D integration plans with commercial vendors

- Advantages of the Tezzaron/Chartered process:

- No extra space allotment in BEOL for 3D TSV,
- 3D TSVs are very small, and placed close together,
- Minimal material added with bond process,
- 35% coverage with 1.6 µm of Cu => Xo=0.0056%,
- No material budget problem associated with wafer bonding,
- Advanced process 0.13 µm and below
- Good models available for Chartered transistors,
- Thinned transistors have been characterized,
- Process supported by commercial tools and vendors,
- Fast assembly + Lower cost (12 3D processed wafers @ $250k in 12 weeks),

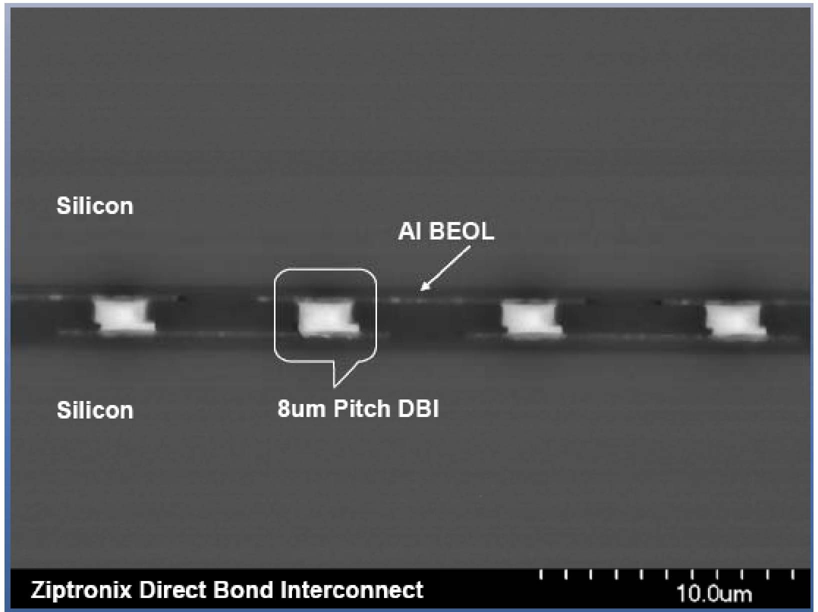


3D integration plans with commercial vendors

- Another demand for 3D assembly comes from detector/ROIC bonding; Fermilab is working with Ziptronix to do low mass bonding with DBI to detectors. (FPIX chips to 50 um thick sensors.);
- Conventional solder bumps or CuSn can pose a problem for low mass fine pitch assemblies

Ziptronix - uses Direct Bond Interconnect (oxide bonding)

- Ziptronix is located in North Carolina
- Fermilab has current project with Ziptronix to bond BTEV FPIX chips to 50 um thick sensors.
- Orders accepted from international customers



DBI® is Scaleable to < 8 um Pitch

Vertical Integration

- 3D Integration is very attractive for highly granular detector systems,
- Bonding is low temperature process, adds limited amount of high-Z material,
- 3D-Integration may extend use of certain detector type (MAPS),
- 3D-Integration is starting to be available in industry,
- Will our community be able to afford?

Other detectors concepts

- CCDs
- MAPS and DNW
- DEPFETs
- CMOS+SOI

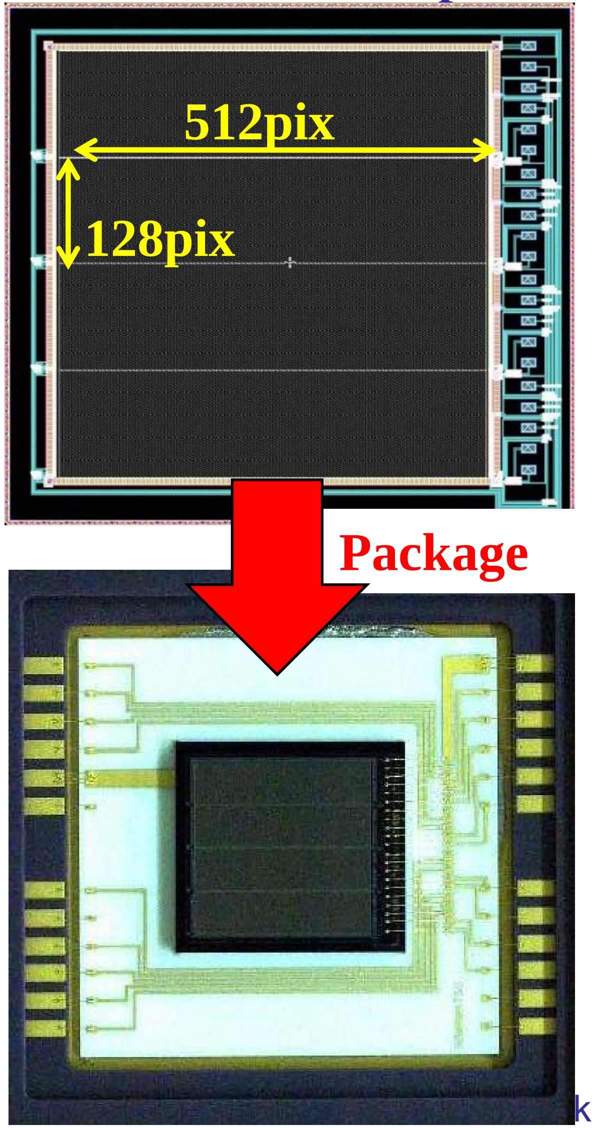
FPCCD

The test-sample of FPCCD was produced in Mar., 2008 by Hamamatsu.

FPCCD test-sample

- Chip-size : 8.2 x 7.5 mm^2
- Pixel size: 12 x 12 μm^2
- # of readout channels: 4
    - 512 x 128 pix/ch
- The several combinations of the wafer-thickness and amplifier-types were produced.
    - Wafer thickness (epi) : 15μm, 24μm
        - ✓ 24μm-ware has higher specific resistance for easy full-depletion.
    - Amplifier : 7 types

FPCCD test-sample



MAPS R&D

- Proof of principle (APSEL0-2)
  - first prototypes realized in 130 nm triple well ST-Micro CMOS process
- APSEL3
  - 32x8 matrix with sparsified readout
  - Pixel cell optimization (50x50 um^2)
    - Increase S/N (15→30)
    - reduce power dissipation x2
- APSEL4D
  - 4K(32x128) pixel matrix with data driven sparsified readout and timestamp
  - Pixel cell & matrix implemented with full custom design and layout
  - Sparsifying logic synthetized in std-cell from VHDL model
  - Periphery inlcudes a “dummy matrix” used as digital matrix emulator
- Test Beam foreseen in Sep 2008
  - Prototype MAPS module + striplets

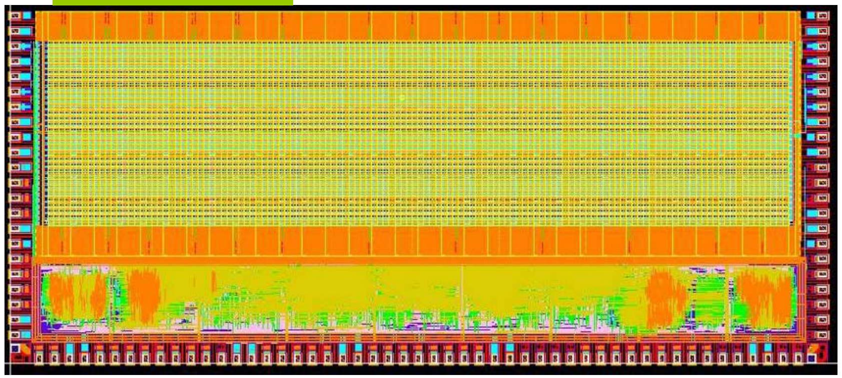
SLIM5 Collaboration

Submitted MAPS Chips

Submission	Chip	Purpose
Sub. 12/2004	TEST_STRUCT	ST 130 Process characterization
	APSEL0	Preamplifier characteriz.
Sub. 8/2005	APSEL1	Improved F-E 8x8 Matrix
Sub. 8/2006	APSEL2M	Cure thr disp. and induction
	APSEL2T	Accessible pixel Study pix resp.
Sub. 9/2006	APSEL2_90	ST 90nm characterization
Sub. 11/2006	APSEL2D	Test digital RO architecture
Sub. 5/2007	APSEL3_CT	Test chips for shield, xtalk
Sub. 7/2007	APSEL3D	32x8 Matrix. Shielded pix. Test for final matrix
Sub. 7/2007	APSEL3_T1, T2	Test chips to optimize pixel and F-E layout

Sept 12, 2007 F.Forti - SLIM5 6

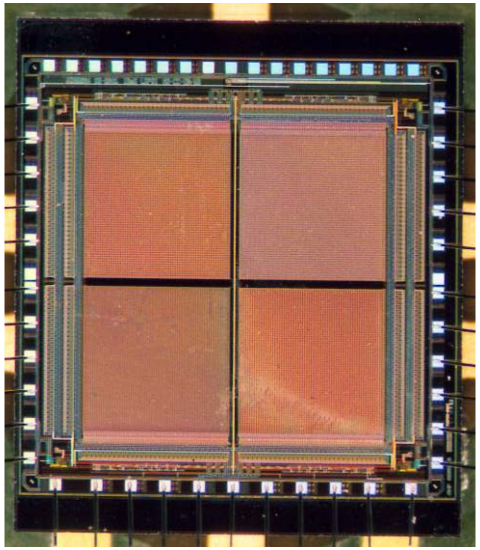
APSEL4D sub 11/2007- rec 3/2008



32x128 4k pixel matrix for beam test

Themis Bowcock

CMOS-sensors (MAPS)

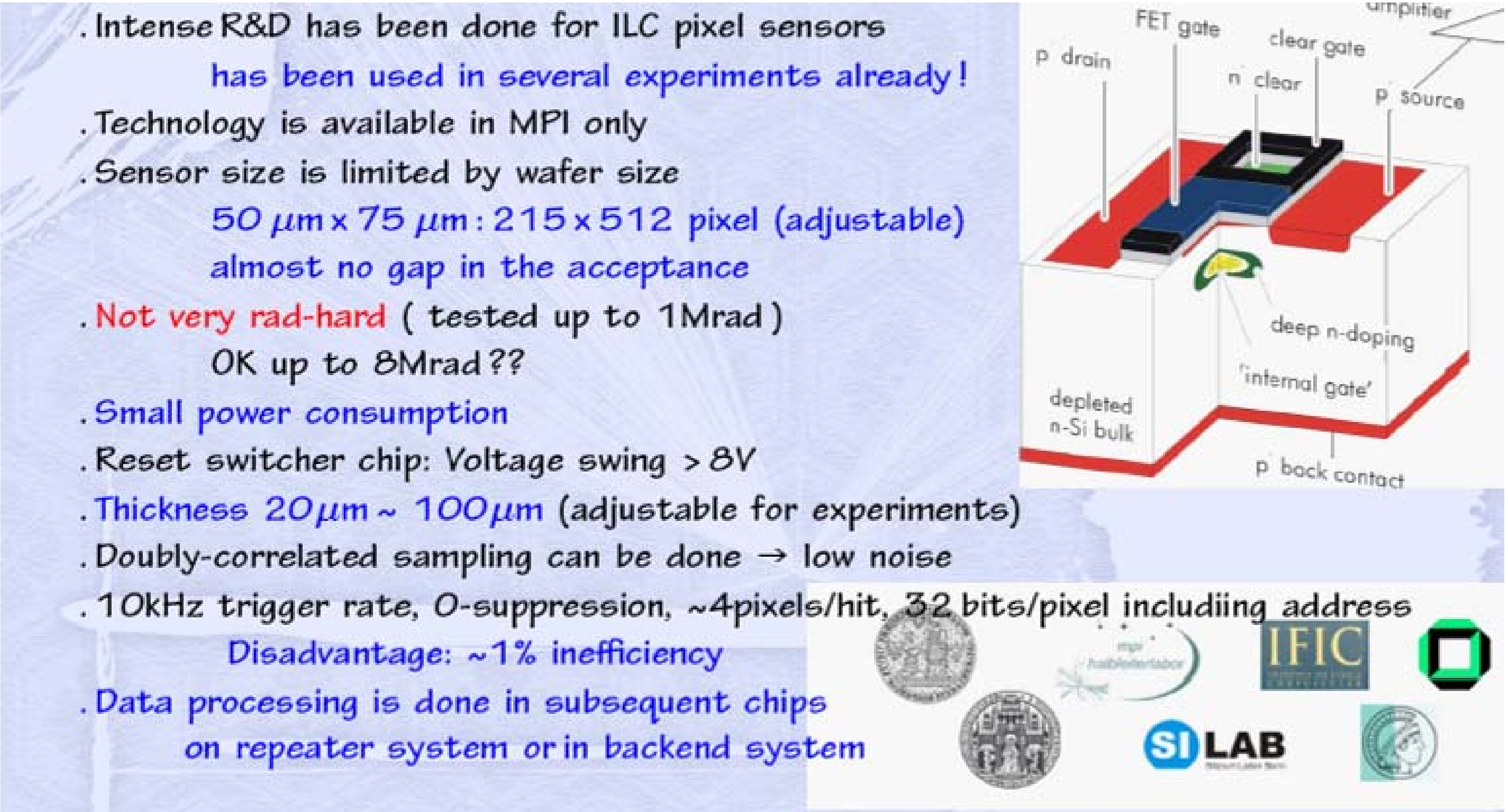


MIMOSA IV

Features of the MIMOSA – detectors:

- Single point resolution 1.5µm - 2.5µm
- Pixel – pitch 10 - 40 µm
- Thinning achieved 50 - 120µm
- S/N for MIPs 20 – 40
- Radiation hardness: 1MRad ; 1 x 10^{13} n_{eq}/cm²
- Time resolution ~ 20 µs (massive parallel readout)

DEPFET



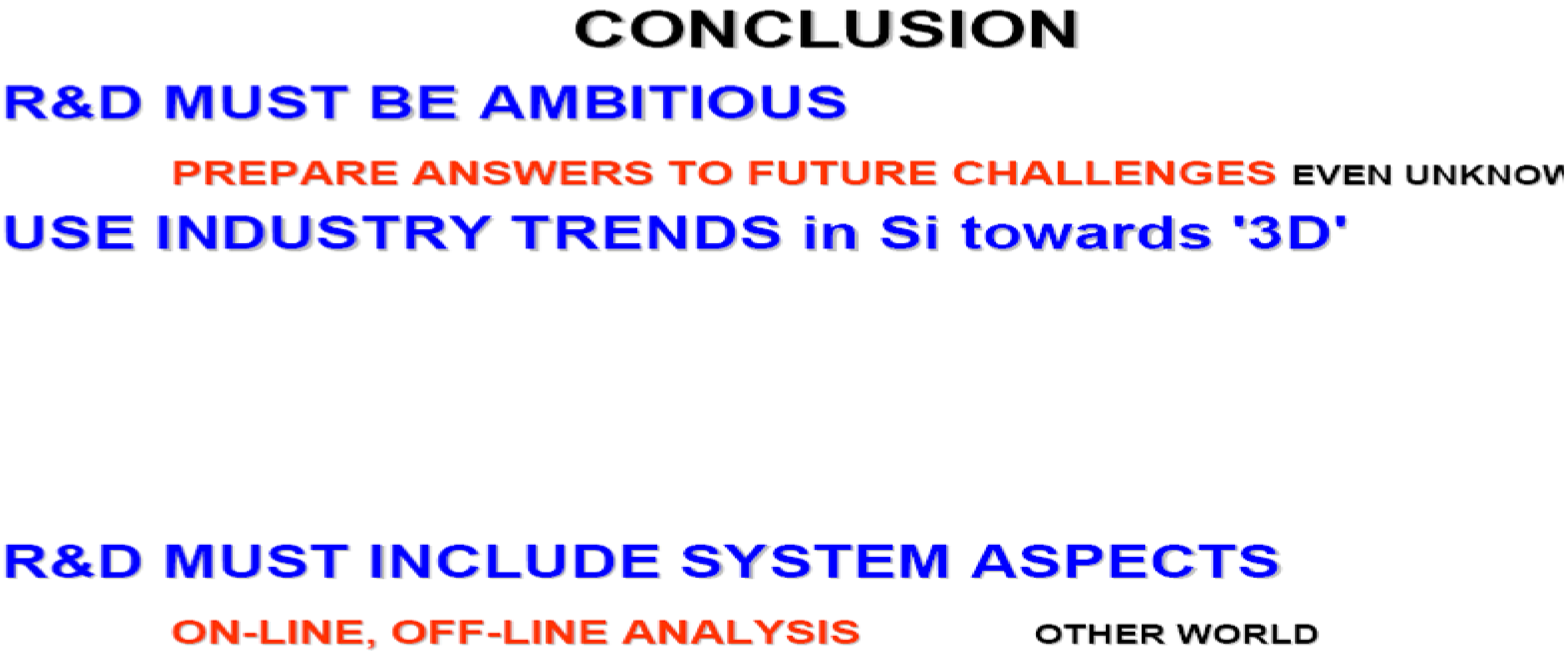
- Intense R&D has been done for ILC pixel sensors
  - has been used in several experiments already!
- Technology is available in MPI only
- Sensor size is limited by wafer size
  - 50 μm x 75 μm : 215 x 512 pixel (adjustable)
  - almost no gap in the acceptance
- Not very rad-hard (tested up to 1Mrad)
  - OK up to 8Mrad??
- Small power consumption
- Reset switcher chip: Voltage swing > 8V
- Thickness 20μm ~ 100μm (adjustable for experiments)
- Doubly-correlated sampling can be done → low noise
- 10kHz trigger rate, 0-suppression, ~4pixels/hit, 32 bits/pixel includiing address
  - Disadvantage: ~1% inefficiency
- Data processing is done in subsequent chips
  - on repeater system or in backend system

PSD

A few thoughts

- Overestimate 5 year impact and underestimate 20 year impact
  - *Vertical Integration !*

Last PSD 2005



CONCLUSION

R&D MUST BE AMBITIOUS

PREPARE ANSWERS TO FUTURE CHALLENGES EVEN UNKNOW

USE INDUSTRY TRENDS in Si towards '3D'

R&D MUST INCLUDE SYSTEM ASPECTS

ON-LINE, OFF-LINE ANALYSIS OTHER WORLD

2008

- Massive Progress in many areas
  - 3D
  - CMOS devices (following industry)
  - n^+p detectors
- Smörgåsbord of technological choices
  - Which ones will make it into detectors?
  - Practicality and COST!
  - How many can be used in non HEP applications?
- Commissioning of major LHC detectors
- Launch of LHC upgrades
  - Will this boost or stifle R&D?

Summary

- R&D healthy and innovative
- Detectors builders worry about prosaic issues
  - Power
  - Cost
  - Material
- New paradigms on the horizon…
- PSD9 should be VERY exciting!