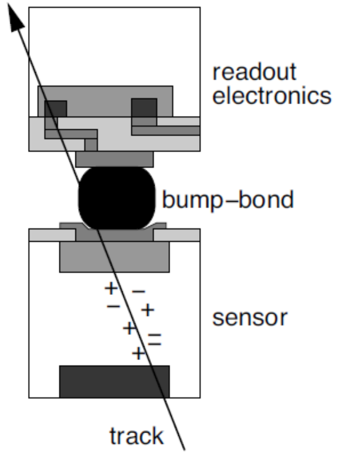
PSD8 Glasgow, September 2008

Pixel Detectors for Charged Particles

N. Wermes
Bonn University

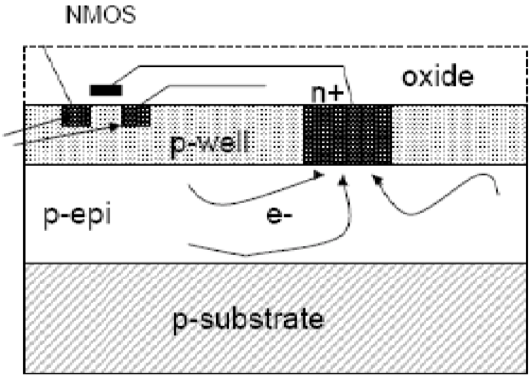
Pixel detectors for charged particle tracking/vertexing

Hybrid Pixel Detectors



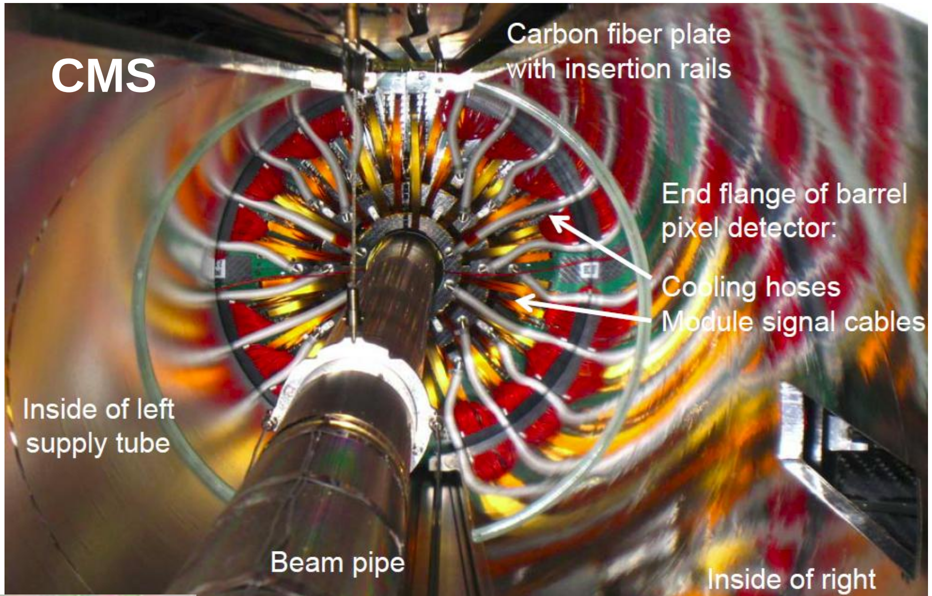
→ all large detectors (i.e. LHC) so far

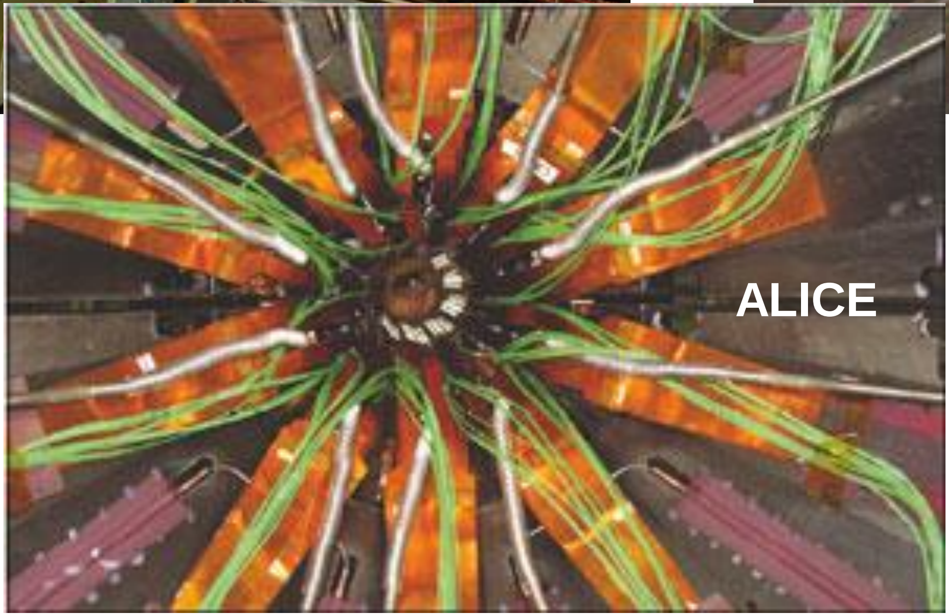
(Semi)-Monolithic Pixel Detectors



→ most new developments except for sLHC
MAPS (epi), MAPS (SOI), DEPFET, 3D-integration

The “PAST”: large area pixel detectors at the LHC





all based on

“Hybrid Pixel Detectors”

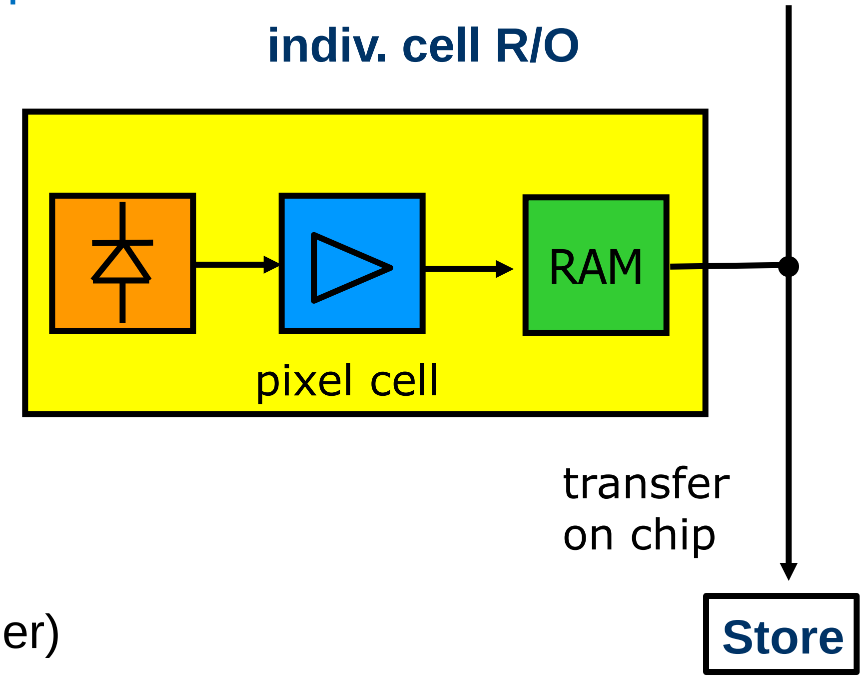
Principle of hybrid pixel detector readout

charge generation in sensor, integration in FE-chip

temporary on chip storage (digital or analog)

trigger driven readout of individual hits

- pn-diode ➔ Q_{signal}
- amplification and filtering ➔ V_{out}
- pixel-wise storage: address, charge, time (BX)
- column-wise R/O
- transfer information to End of Column (wait for trigger)



end of column
storage & logic

- address
- charge (ToT)
- time

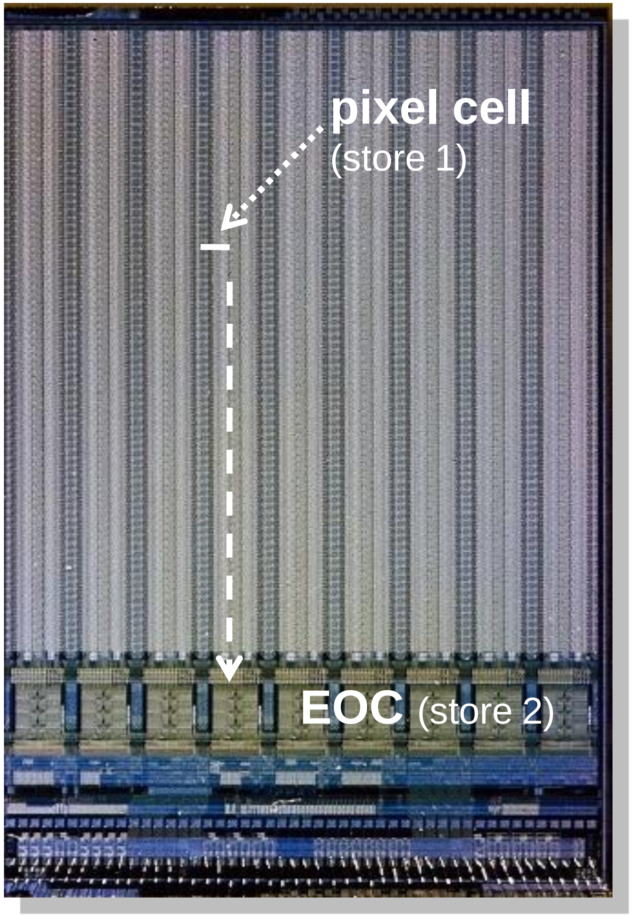
Principle of hybrid pixel detector readout

charge generation in sensor, integration in FE-chip

temporary on chip storage (digital or analog)

trigger driven readout of individual hits

- pn-diode ➔ Q_{signal}
- amplification and filtering ➔ V_{out}
- pixel-wise storage: address, charge, time (BX)
- column-wise R/O
- transfer information to End of Column (wait for trigger)



✓ **high rate capability**

✓ **radiation hard to 10^{15} n_{eq}/cm^2**

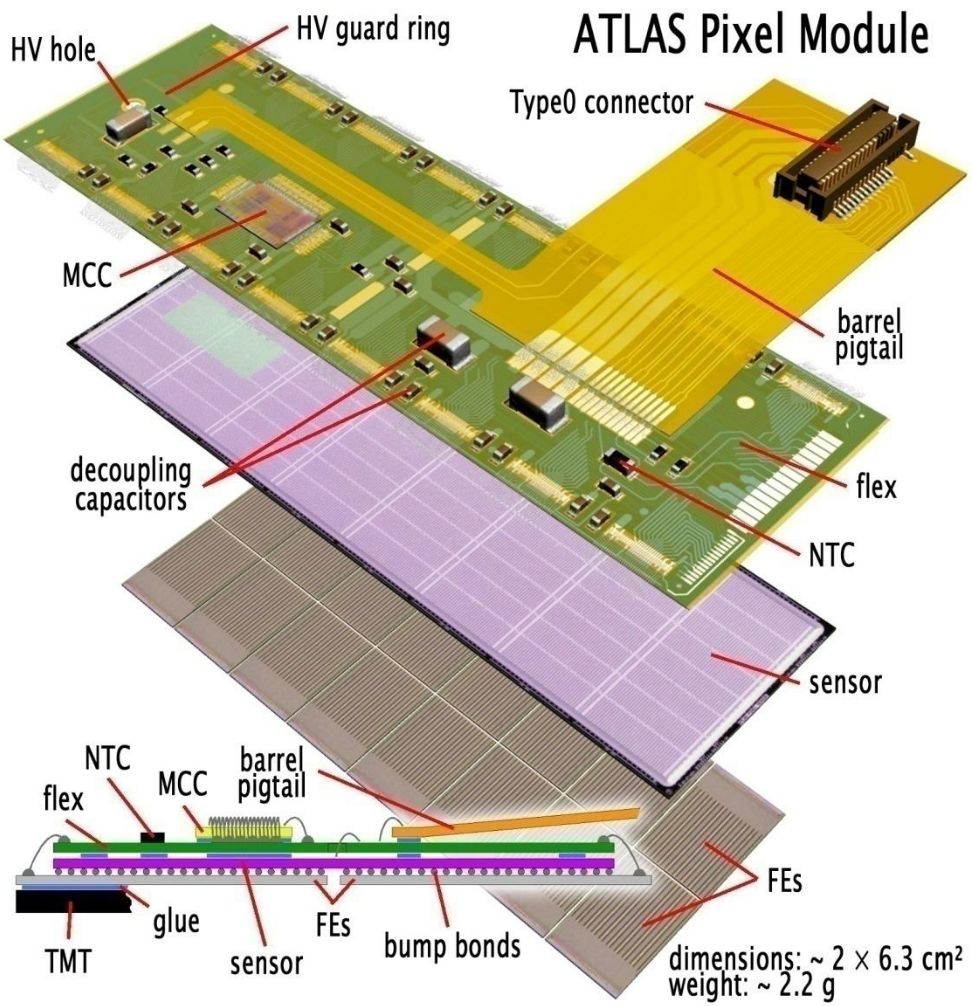
✓ **mature technology**

❖ **comparatively massive (>3% X_0, mostly due to power and "overall size")**

❖ **resolution ~10 µm (pixels sizes 50x400 µm² or 100x150 µm²)**

} → **improve**

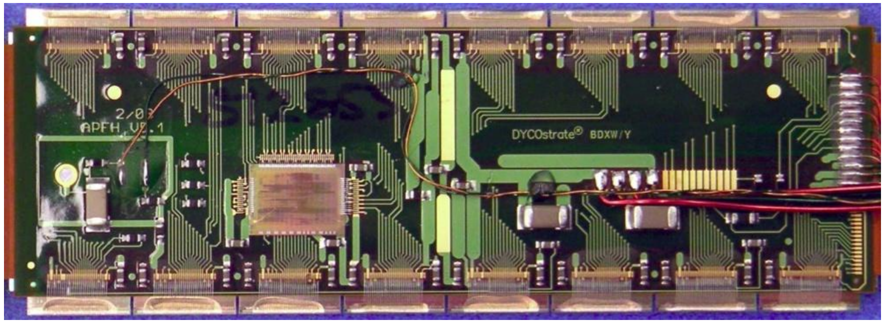
A Hybrid Pixel Detector Module



dimensions: ~ 2 × 6.3 cm²
weight: ~ 2.2 g

- **module (1.1% X_0)**
- **supports & cables (2.4% X_0)**

per layer



Principle of (semi-) monolithic pixel detectors

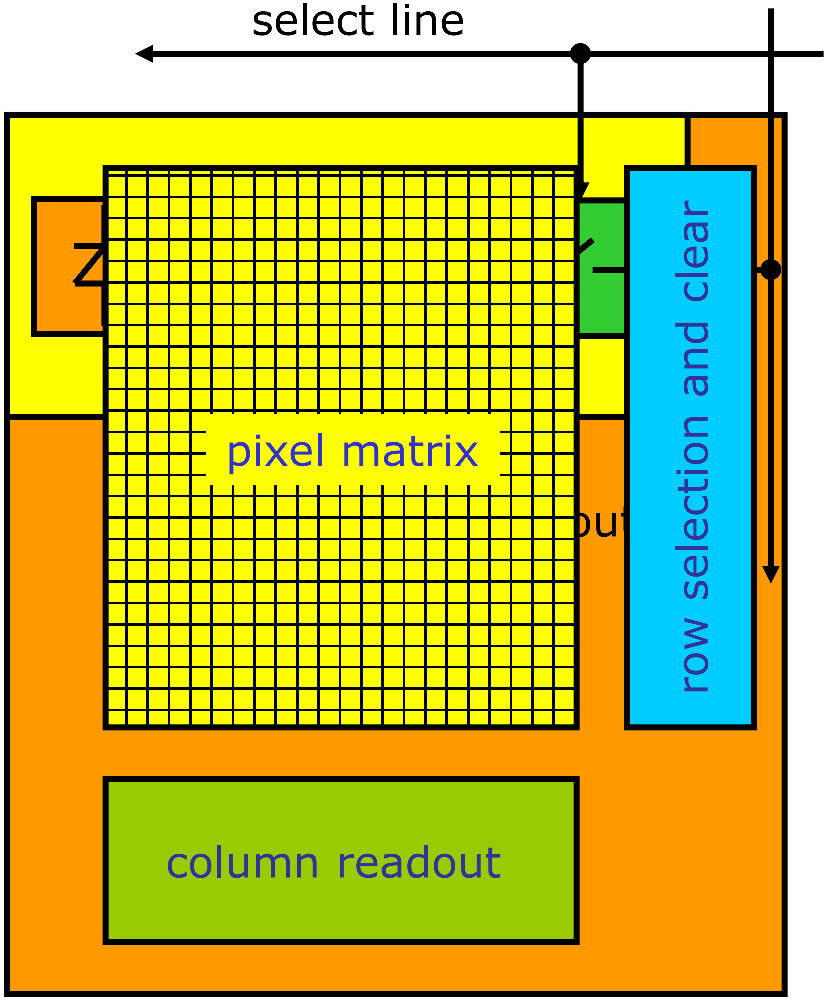
generation and processing of signal in “same” substrate

at least so far …

- pn-diode ➔ Q_{Signal}
- collection diode (transistor gate)

  ➔ $U_{Signal} = Q_{Signal} / C_g$

  or $I_{Signal} = g_m \cdot Q_{Signal} / C_g$
- row wise selection of pixels
- column wise readout
- select/reset switch



frame R/O

CMOS active pixels

- same CMOS substrate
  for steering/readout electronics
  and for Q – collection

DEPFET pixels

- one amplifying transistor on fully depleted bulk
  separate steering and R/O chips

Principle of (semi-) monolithic pixel detectors

generation and integration of signal in “same” substrate

- pn-diode ➔ Q_{Signal}
- collection diode (transistor gate)

  ➔ $U_{Signal} = Q_{Signal} / C_g$

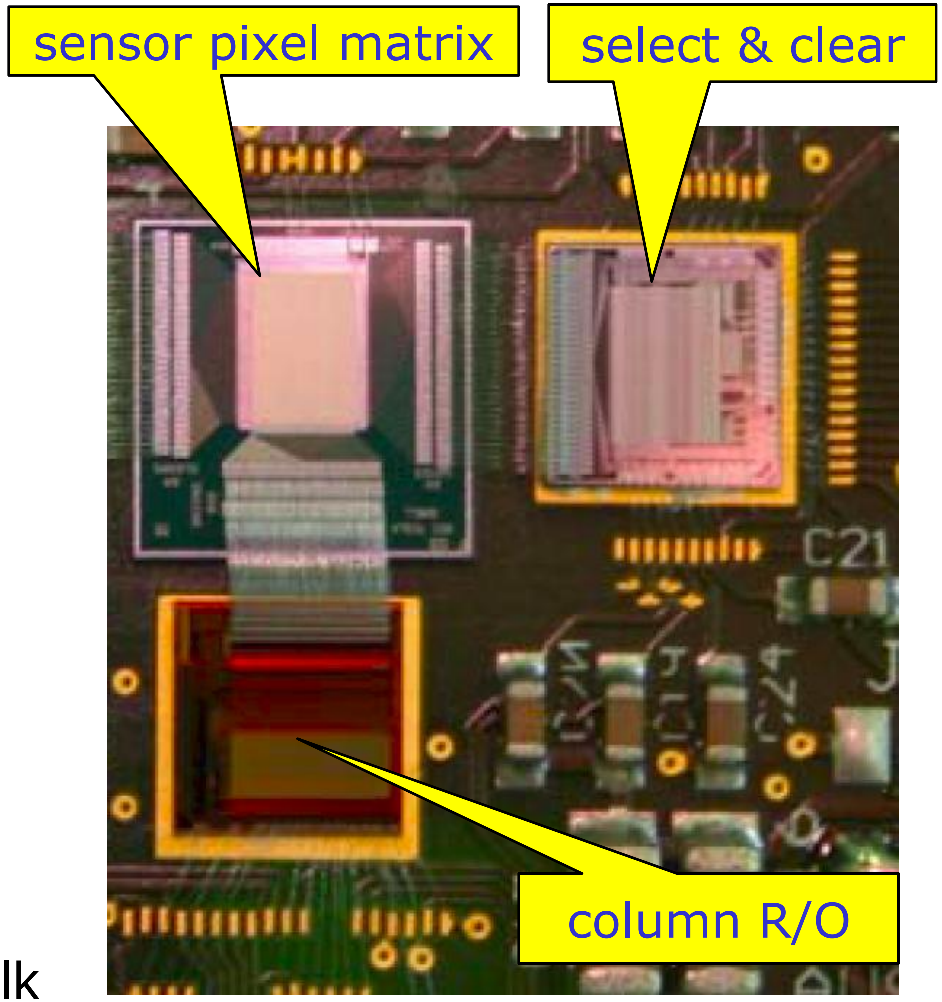
  or $I_{Signal} = g_m \cdot Q_{Signal} / C_g$
- row wise selection of pixels
- column wise readout
- select/reset switch

CMOS active pixels

- same CMOS substrate
  for steering/readout electronics
  and for Q – collection

DEPFET pixels

- one amplifying transistor on fully depleted bulk
  separate steering and R/O chips



frame R/O

Rate and radiation challenges at the innermost pixel layer

Hybrid Pixels

	BX time	Particle Rate	Fluence	Ion. Dose
	ns	kHz/mm^2	n$_{eq}$/cm^2 per lifetime*	kGy per lifetime*
LHC (10^{34} cm^{-2}s^{-1})	25	1000	1.0 x 10^{15}	790
superLHC (10^{35} cm^{-2}s^{-1})	25	10000	10^{16}	5000
SuperBelle (10^{35} cm^{-2}s^{-1})	2	400	~3 x 10^{12}	50
ILC (10^{34} cm^{-2}s^{-1})	350	250	10^{12}	4
STAR@RHIC (8x10^{27} cm^{-2}s^{-1})	110	3,8	1.5 x 10^{13}	8

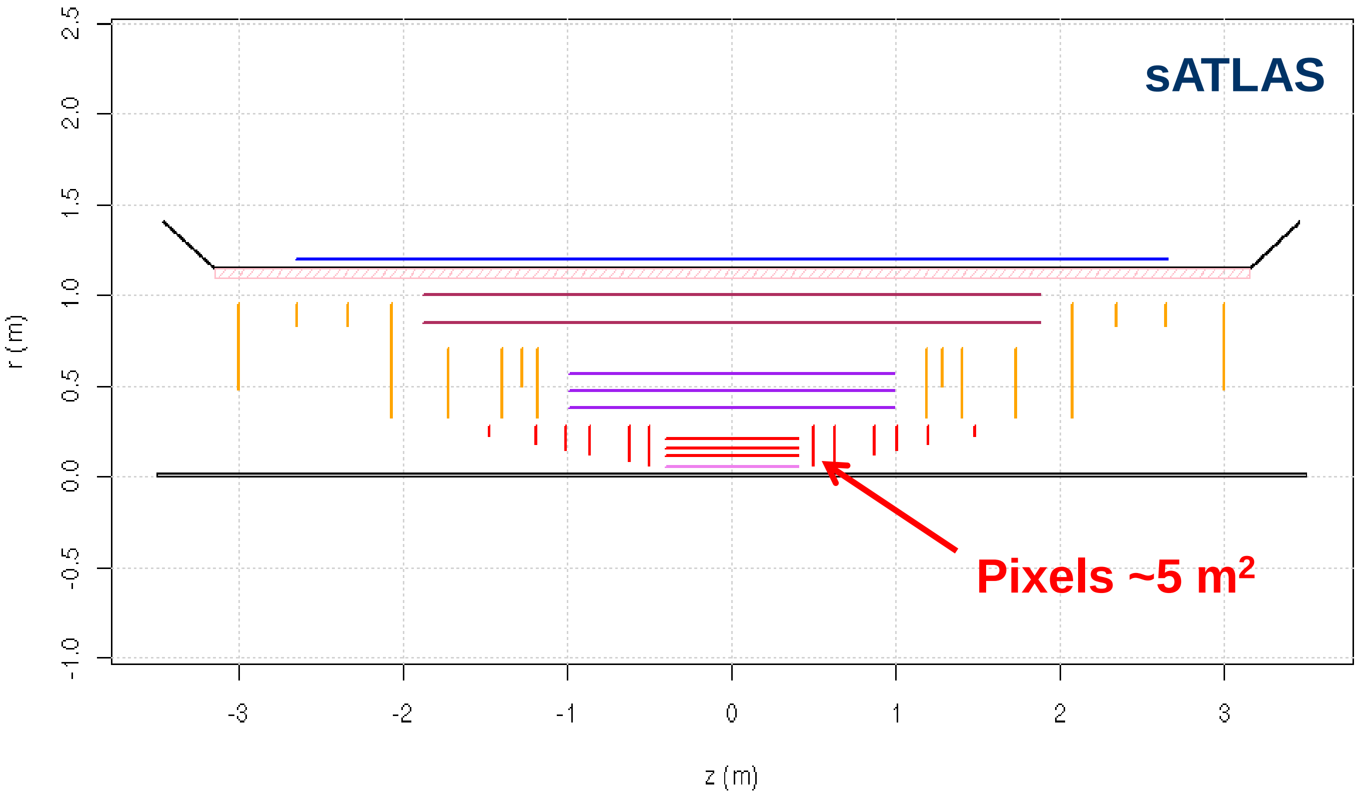
Monolithic Pixels

lower rates
smaller pixels
less material

assumed lifetimes:
LHC, sLHC: 7 years
ILC: 10 years
others: 5 years

Pixels for super-LHC (2016)

current directions



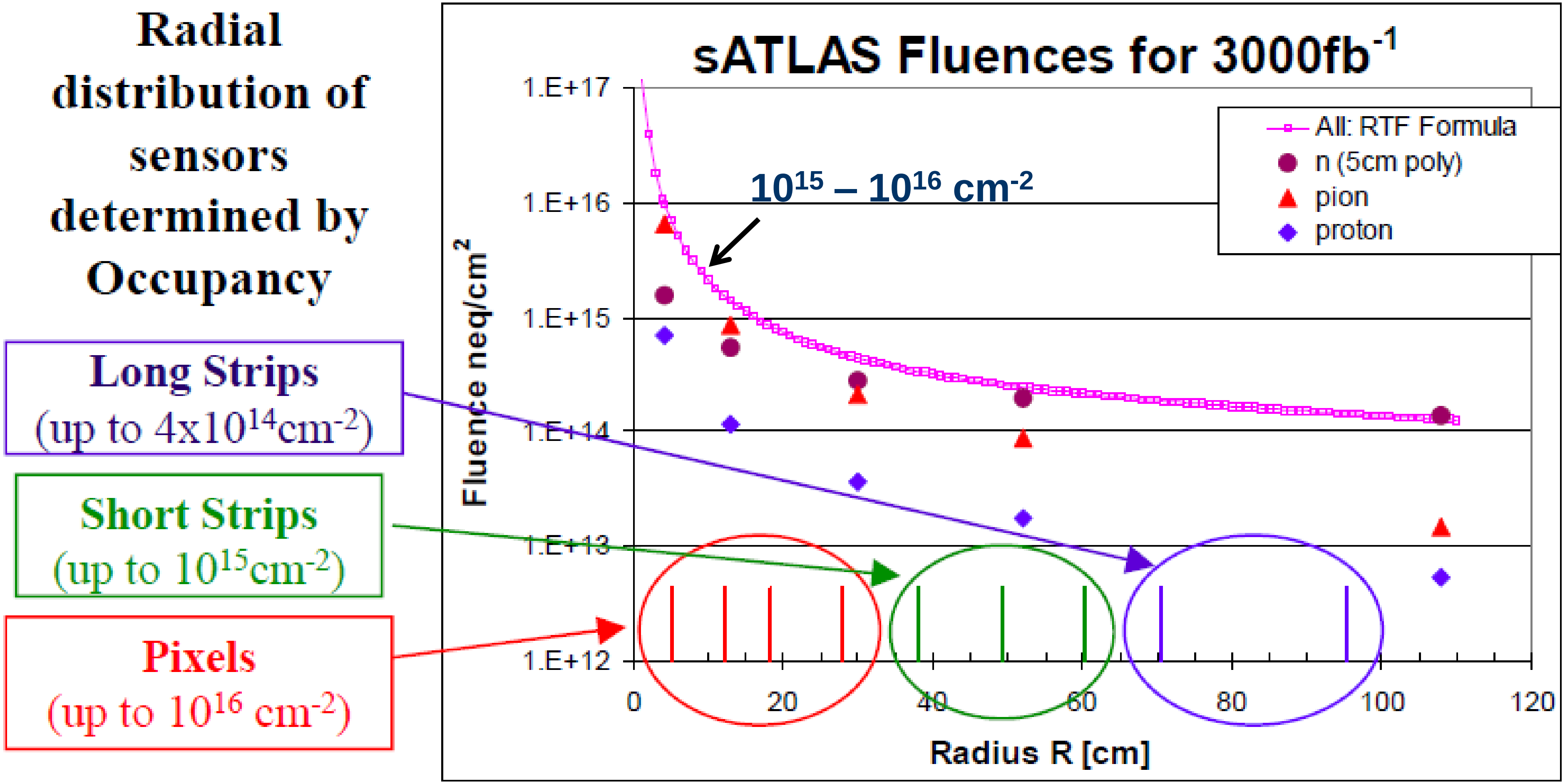
Pixels ~5 m^2

note: **intermediate step → B-layer upgrade/replacements scenarios (~2012)**

Main issues @ sLHC

- **radiation hardness**

Radial distribution of sensors determined by Occupancy



Long Strips
(up to 4×10^{14}cm^{-2})

Short Strips
(up to 10^{15}cm^{-2})

Pixels
(up to 10^{16} cm^{-2})

ATLAS Radiation Taskforce [ATL-GEN-2005-01] & H.Sadrozinski [IEEE NSS 2007]

Main issues @ sLHC

- **radiation hardness**
  - ~10^{16} n_{eq}/cm^2 @ innermost layers
  - new sensor R&D ongoing: 3D-silicon, planar (n in p), diamond

- **data rate**
  - output rate at innermost layer = 320 MHz = 4 x LHC

- **material**
  - strong interplay between: resolution – secondaries – pattern/track algorithms

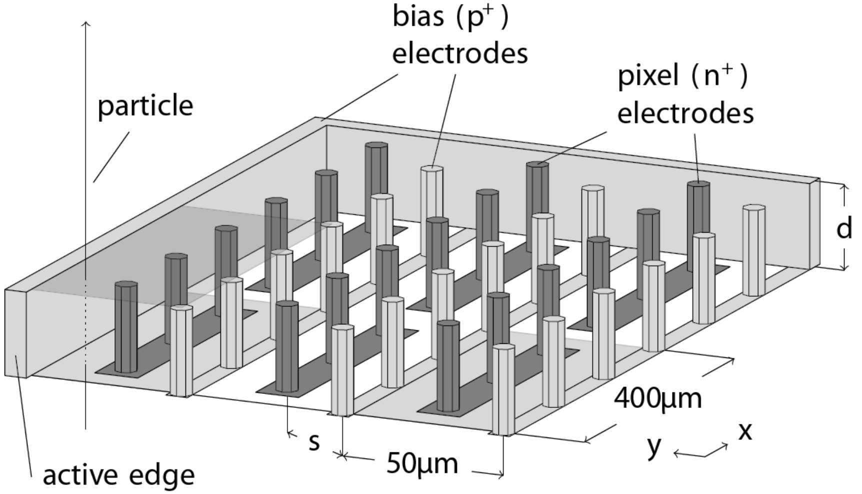
    → what is the best detector? more layers? less material?
  - new powering concepts needed (serial, DC-DC)
  - goal: 1.5-2% $X_0 \Rightarrow$ factor ~2 reduction wrt. LHC (!)

sLHC Sensor R&D

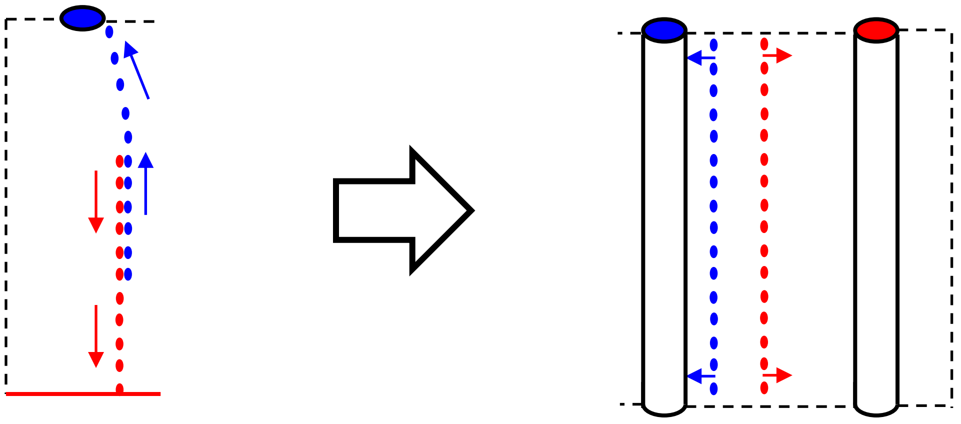
3D silicon

3D collaboration: C. da Via' , S. Parker, C. Kenney et al.

Technique: Deep Reactive Ion Etching (DRIE)



track parallel to electrode



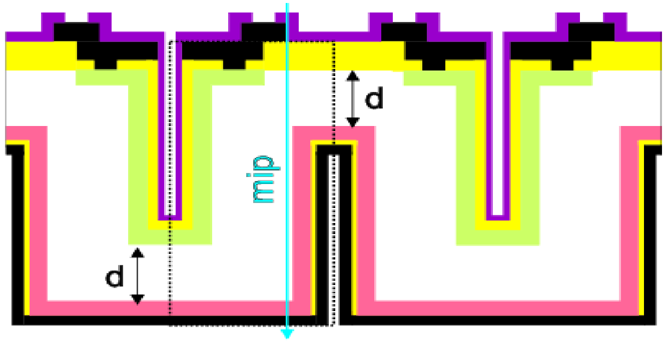
planar Si

3D silicon

- ✓ shorter drift distance → fast
- ✓ lower voltages
- ✓ better radiation tolerance
- ✓ sensor edge can be an electrode

- ❖ inefficient in area of electrode
- ❖ manufacturing yield & costs = ?

large effort
(new) vendors
Stanford
SINTEF (Oslo)
IRST (Trieste)
CNM (Barcelona)

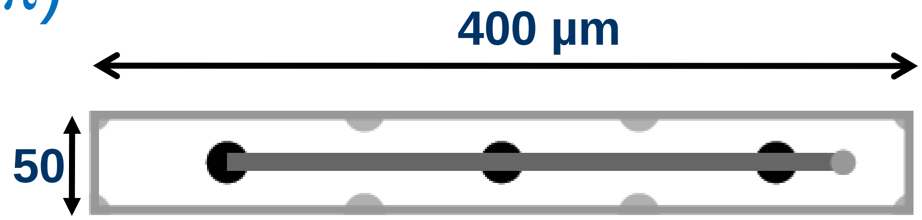


sLHC Sensor R&D

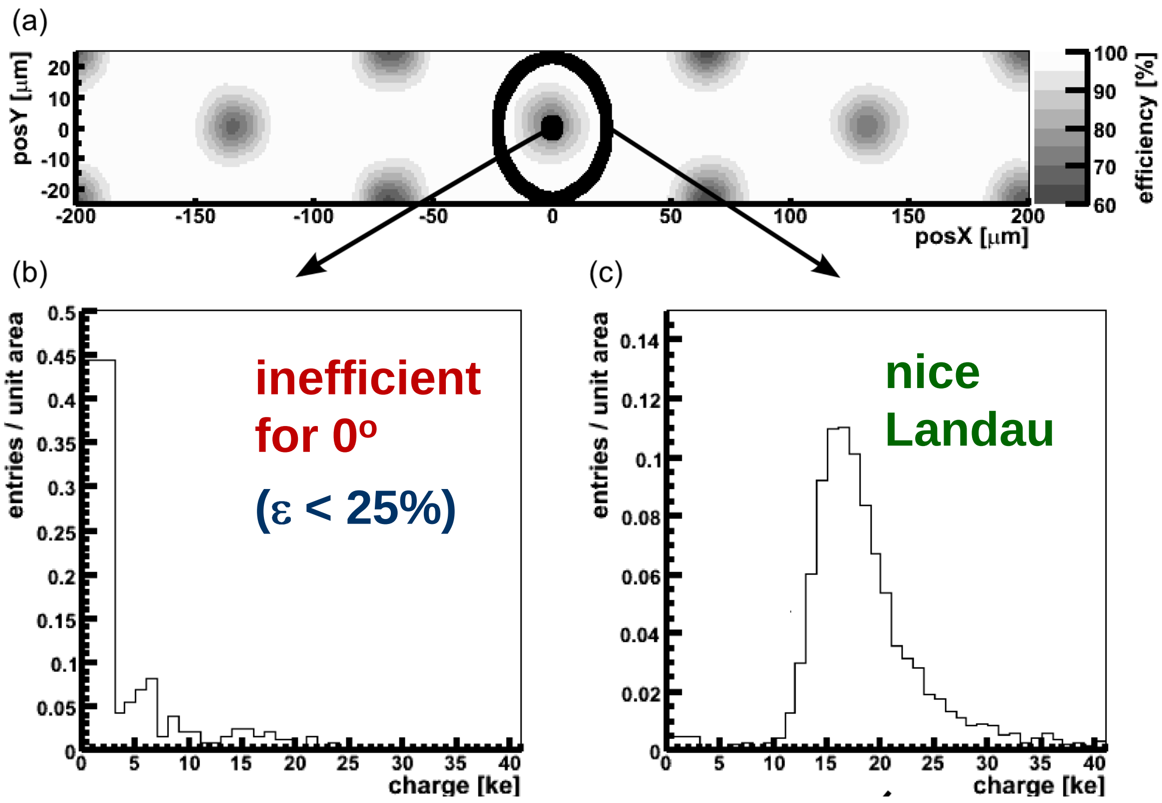
M. Mathes et al., IEEE TNS 2008 (accepted)

3D: test beam results (100 GeV π)

- Stanford devices, unirradiated
- pixel electronics (ATLAS FE-I3)



3E device = 3 electrodes/pix
with ATLAS pixel geometry
columns reach through bulk



inefficient for 0°

(ε < 25%)

nice Landau

- ✓ **V_{depl} ~ 10 V**
- ➢ **efficiency 95.6% (0° tracks)**
  99.9% (15° tracks)
- ✓ **spatial resolution as for planar pixels (~12 µm)**

sLHC Sensor R&D

diamond (poly crystalline and single crystal)

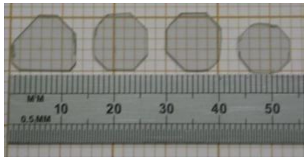
RD42 collaboration
H. Kagan, P. Weilhammer et al.

- ✓ **has finally become competitive (to Si)**
  - ✓large band gap (x5) → no leakage current → no shot noise
  - ✓smaller ε_r (x 0.5) → lower input capacitance → lower thermal and 1/f noise
  - ✓small Z=6 → large radiation length (x2 in g/cm^2)
  - ✓narrower landau distribution (by 10%)
  - ⇨ ✓excellent thermal conductivity (x15) → use as cooling structure
  - ❖large w_i (x 3.6) → small signal charge
  - ❖fabrication not standard (wafer production, cutting) … but "pixellation" almost trivial

using pixel-specific ENC formulae (CSA+filter) and measurements with 100 GeV π

S/N per 0.1% X_0 → Si : diamond ≈ 1 : ~1.4

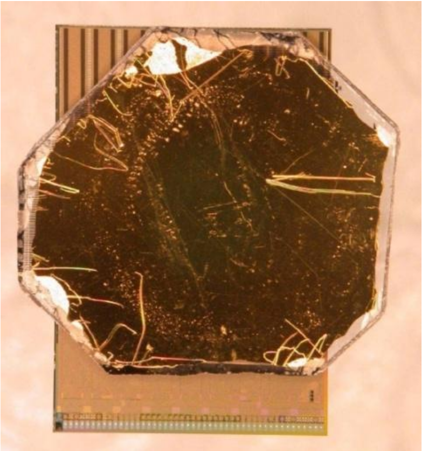
- **✓poly-CVD has been turned into 16 chip ATLAS modules**



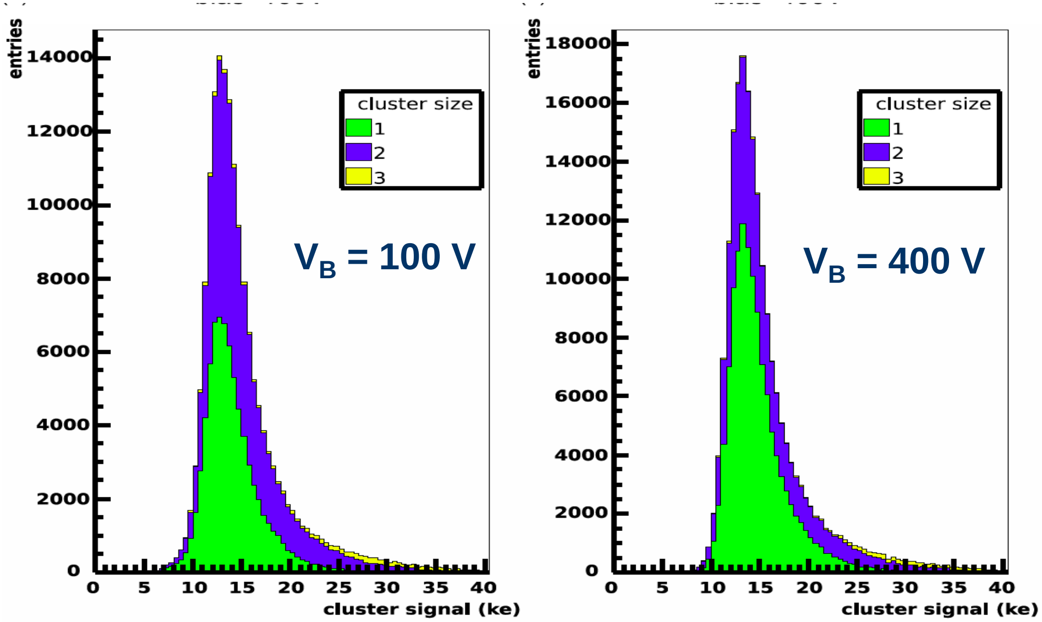
- **✓sc-CVD sensors of few cm^2 size used as pixel detectors**

sLHC Sensor R&D

<u>single</u> crystal diamond pixel detector

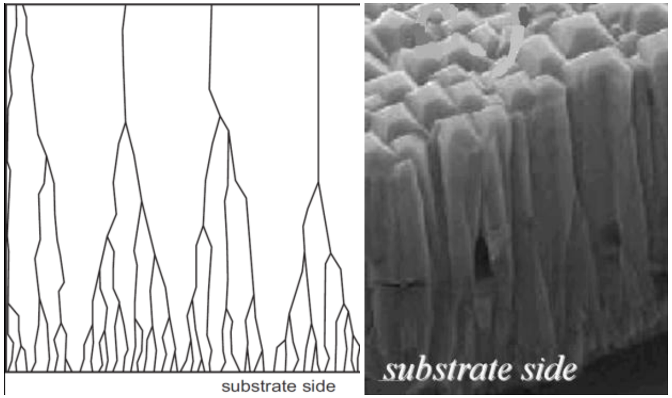


beautiful Landau distributions

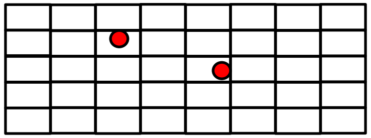


M. Mathes et al.

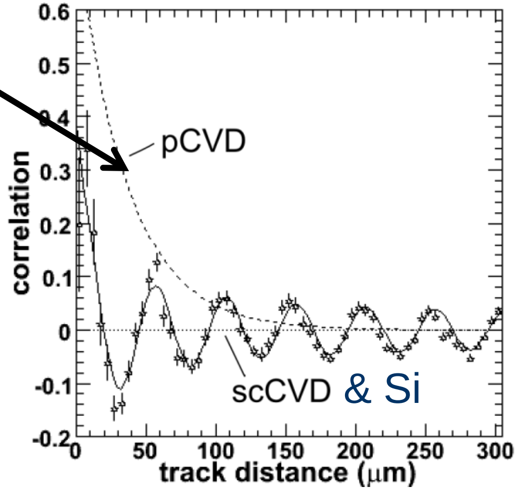
pCVD diamond (grain structure)



track 1, ev-1



track 2, ev-2



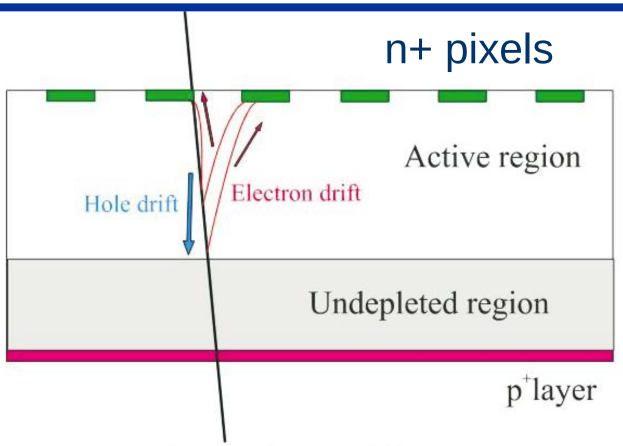
scCVD is like silicon

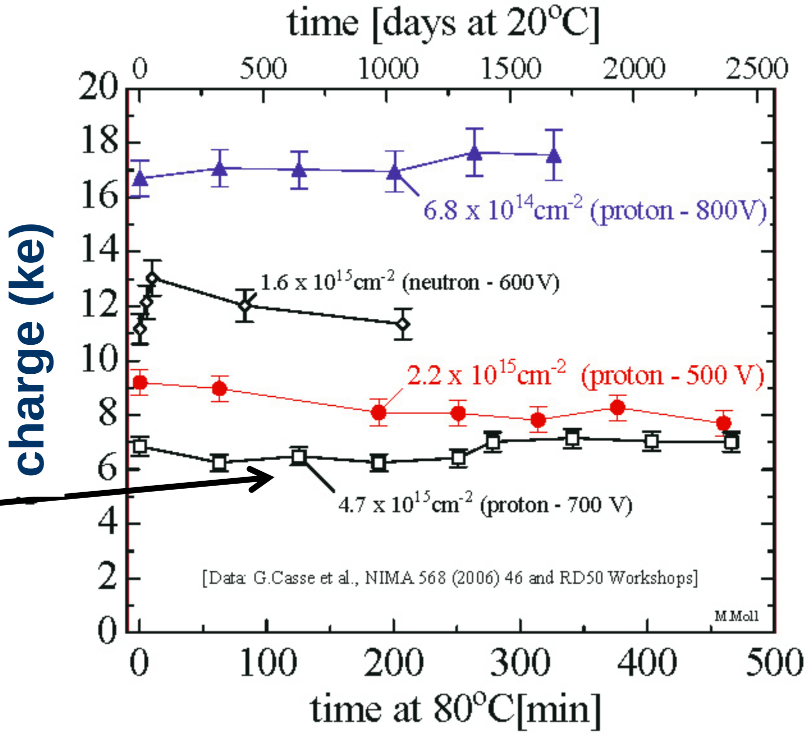
sLHC Sensor R&D

planar sensor R&D

- technology of choice for larger area (costs !)
- increase radiation tolerance (10^{16} cm^{-2} tough !)
- increase active area fraction
- large activity on Si materials
  - FZ/(M)CZ
  - p-type bulk (no type inversion)

- **trend:** n^+ on n ➔ **n^+ on p** (FZ or MCZ)
  - pixel electrodes on junction side
  - single sided wafer processing (cost!)
  - no reverse annealing for CCE meas.
  - ~30% CC @ 10^{16} cm^{-2} (~6000 e^-)

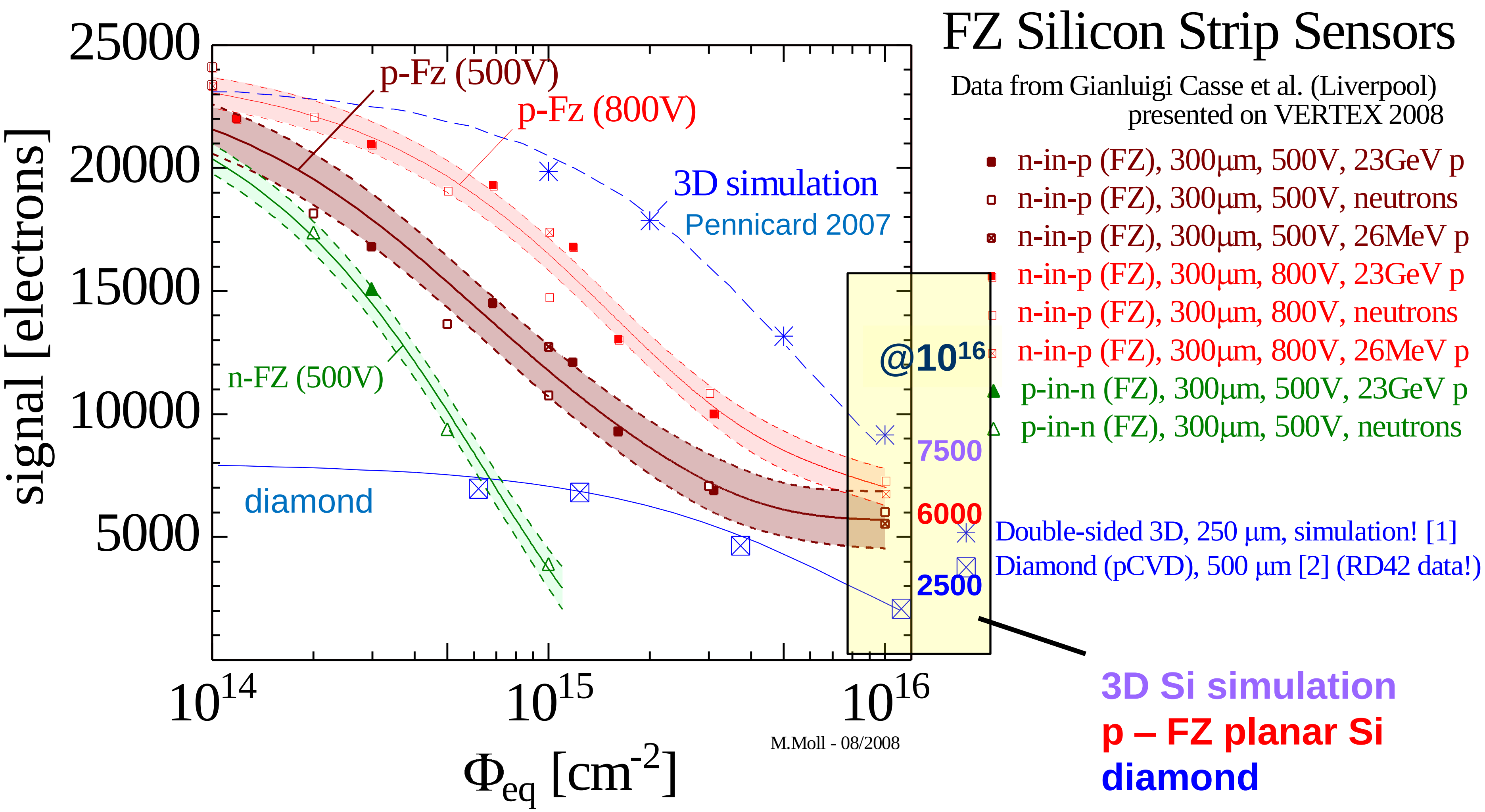




[Data: G.Casse et al., NIMA 568 (2006) 46 and RD50 Workshops]

R&D proposals and projects for sLHC

Pixels at sLHC: radiation tolerance



3D Si simulation

p – FZ planar Si

diamond

note: n_{eq} (Si) normalization (correct for diamond?) & diamond better in S/N terms

sLHC sensor R&D

a personal opinion

- 3D silicon and CVD diamond (especially scCVD) are attractive

  - ✓ for small area pixel detectors (1st layer) where costs do not play a major role
  - ✓ radiation hardness is the major issue
  - ✓ S/N counts !
  - ❖ high quality wafer production at vendors must still be shown
  - ❖ scCVD diamond perhaps not an option on the sLHC time scale? (unfortunately)
  - ❖ only small single chip pixel modules demonstrated for 3D and scCVD
  - ✓ large pixel modules made with pCVD diamond

- for outer layers (fluence < 10^{15} cm^{-2}, area >5 m^2) planar detectors are the choice

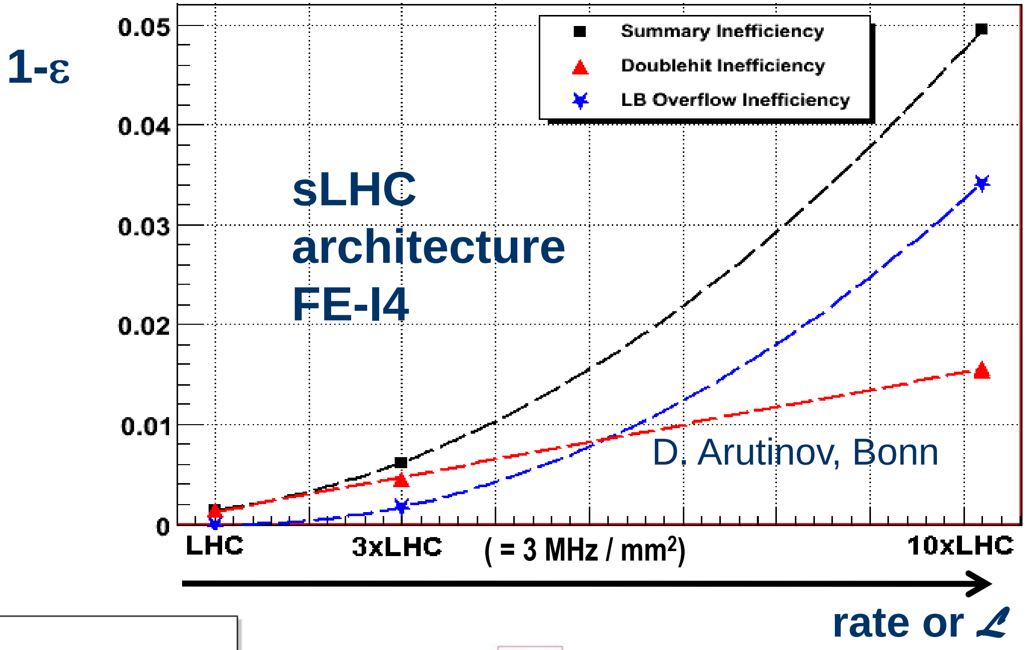
  - ✓ promising Si material studies (trend n^+ in p FZ or MCz)
  - ❖ building and radiation testing of real modules is due!

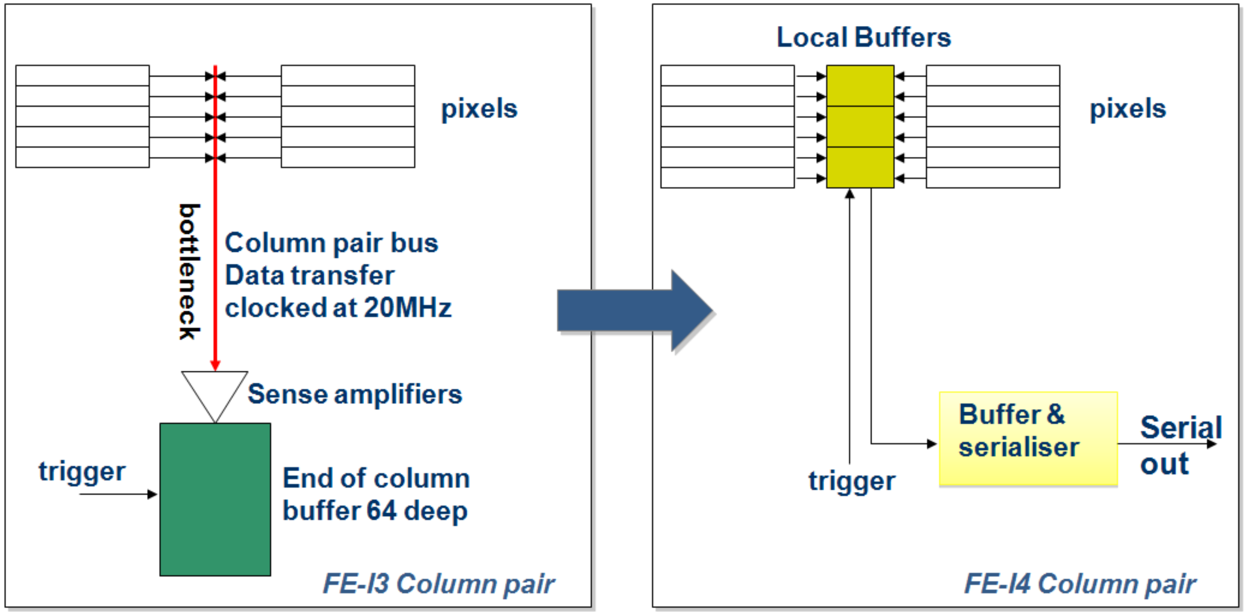
sLHC data rates

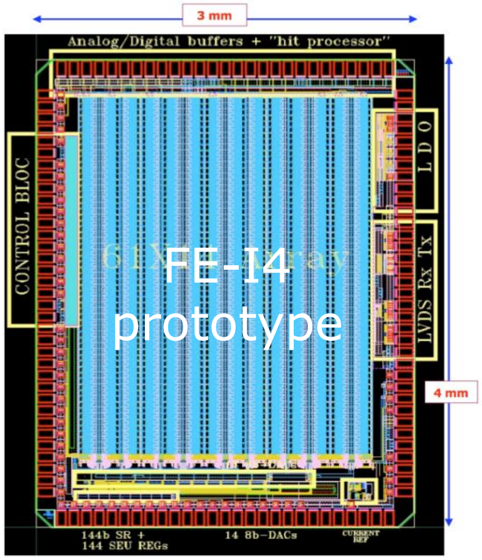
Hit inefficiency rises steeply with the hit rate

Bottleneck: congestion in double column readout

⇒more local in-pixel storage (130 nm !)
>99% of hits are not triggered
⇒ don’t move them



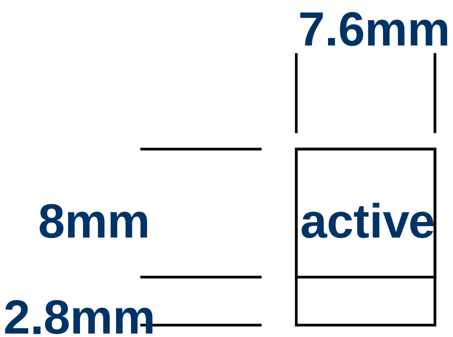




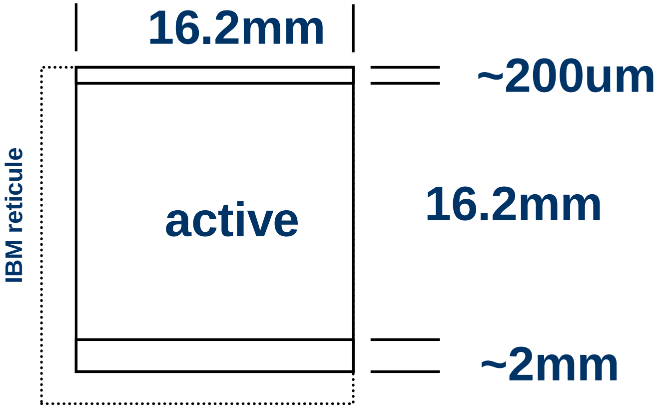
Bonn
Genova
LBNL
NIKHEF

Hybrid Pixel: sLHC FE - Chip and Modules

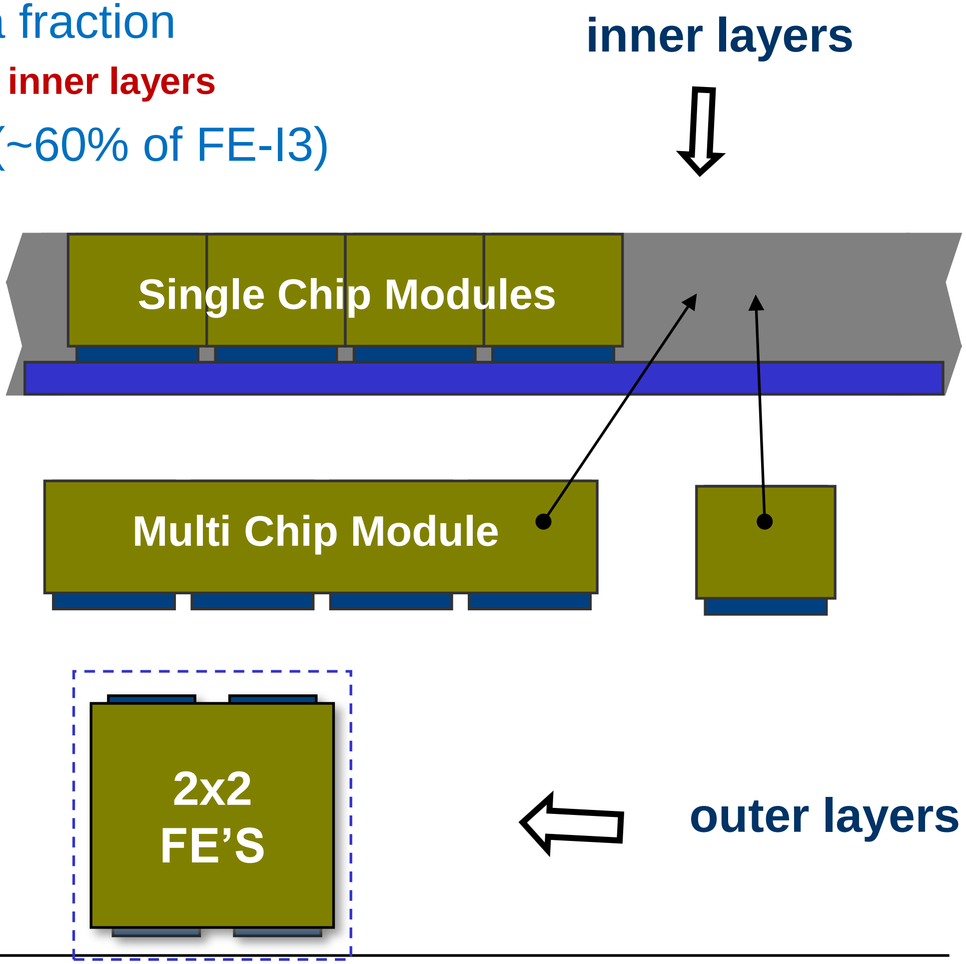
- smaller pixel area (50 x 250 μm^2)
  - **smaller occupancy, better resolution**
- larger chip (!)
  - **lower cost in BB & FC (cost driver)**
- larger active area fraction
  - **better coverage in inner layers**
- power reduction (~60% of FE-I3)



FE-I3
74%

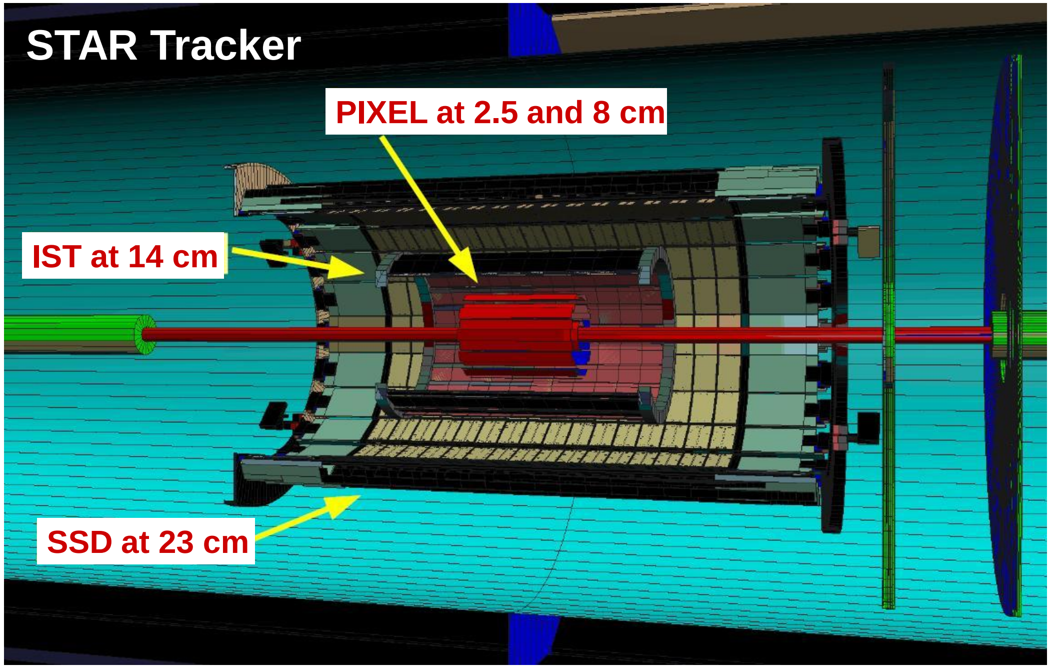


FE-I4
~87%



(semi-) Monolithic Pixels

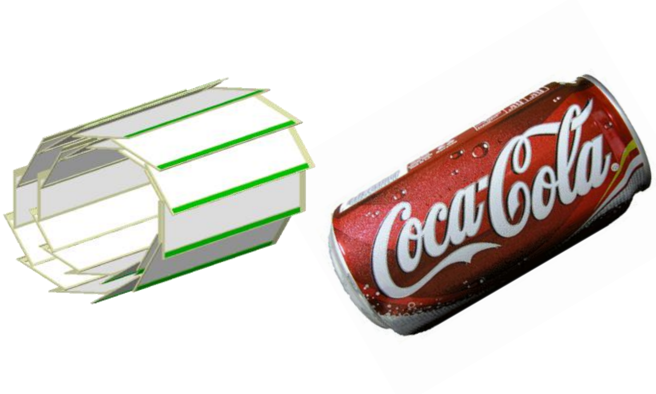
STAR@RHIC, superBelle, ILC



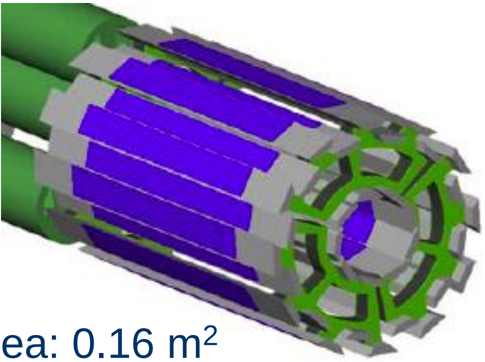
(Semi-) Monolithic Pixels Overview

- DEPFET Pixels
  - one transistor in pixel bulk
  - Q-collection in fully depleted bulk
  - R&D (for ILC) since > 10 years
  - recently (2008): a 2 layer detector for superBelle

total area: 0.014 m^2



- Monolithic Active Pixels (MAPS-epi)
  - Q collection in thin epi-layer
  - need tricks for full CMOS
  - R&D (for ILC) since ~ 10 years
  - 2 (or 3) layer detector for STAR@RHIC

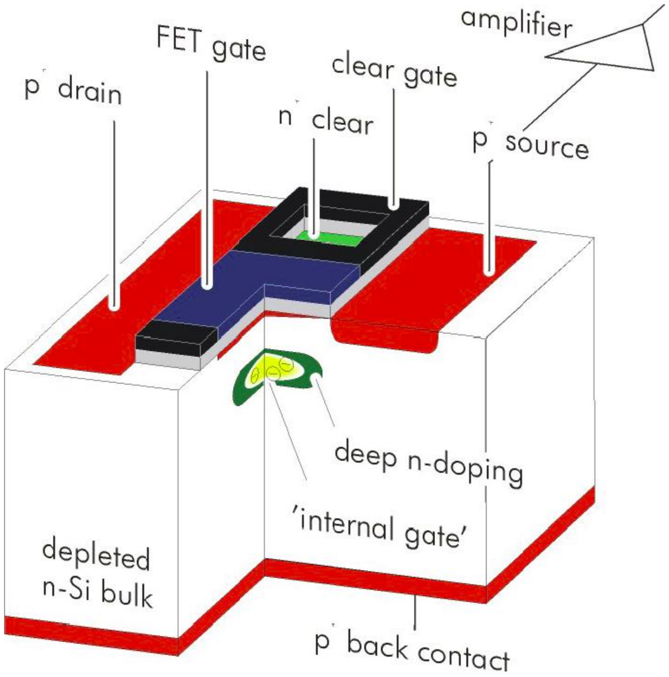


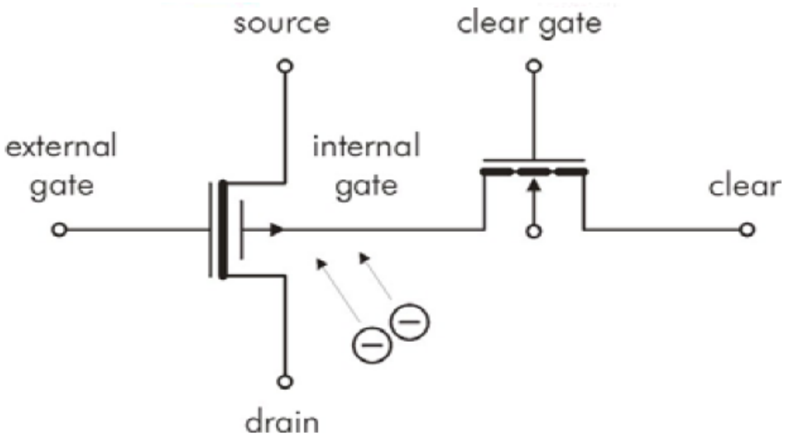
total area: 0.16 m^2

- Monolithic Active Pixels (MAPS-SoI)
  - **full CMOS in active area**
  - Q - collection in **fully depleted** bulk
  - R&D started 2006

I will show a selection of current efforts

DEPFET pixels

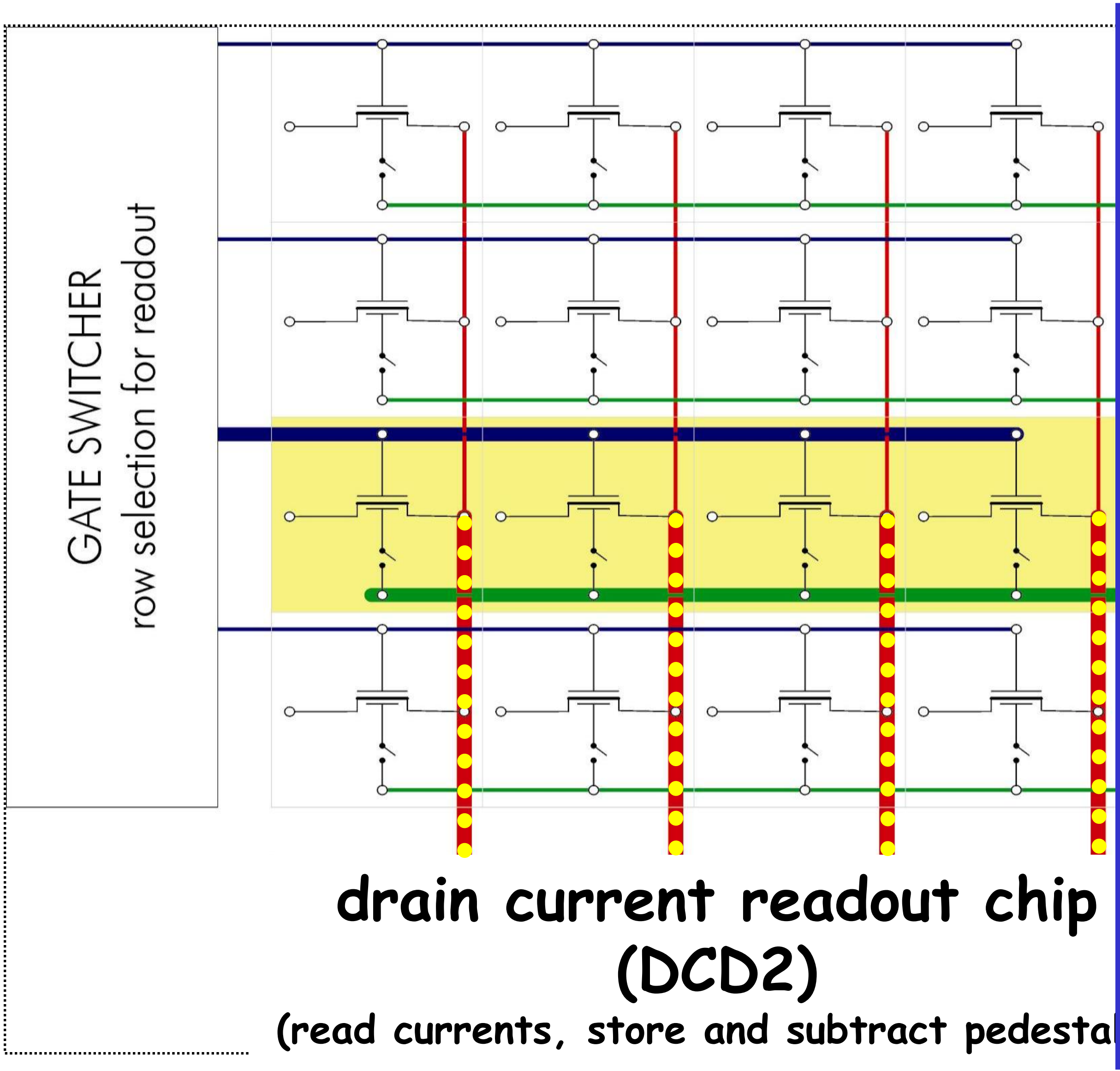




- p-channel MOSFET in pixel on a fully depleted bulk
  - ✓ large signal
  - ✓ fast collection
  - ✓ small pixels (24 x 24 µm^2)
- Internal gate (IG): deep (~1µm) n-implant is potential minimum for e^-
- Signal electrons accumulate in IG and modulate the transistor current (g_q~ 400 pA/e^-)
  - ✓ low C_{in} , internal amplification → low noise
- Accumulated charge removed by CLEAR ("reset")
  - ✓ multiple R/O possible
  - ❖ external reset needed (no reset noise if CLEAR complete)
- Transistor off during signal collection
  - ✓ low power
- R/O of the (current) signal at transistor drains
  - ❖ steering & signal processing by external ICs

Collaboration: Aachen, Bonn, Heidelberg, MPI Munich, Karlsruhe, Prague, Valencia

DEPFET pixels: „rolling shutter“ frame R/O



drain current readout chip (DCD2)

(read currents, store and subtract pedesta

- **<u>1 row active</u>**

  (1) read signal + ped current

  (2) CLEAR

  (3) read pedestal current

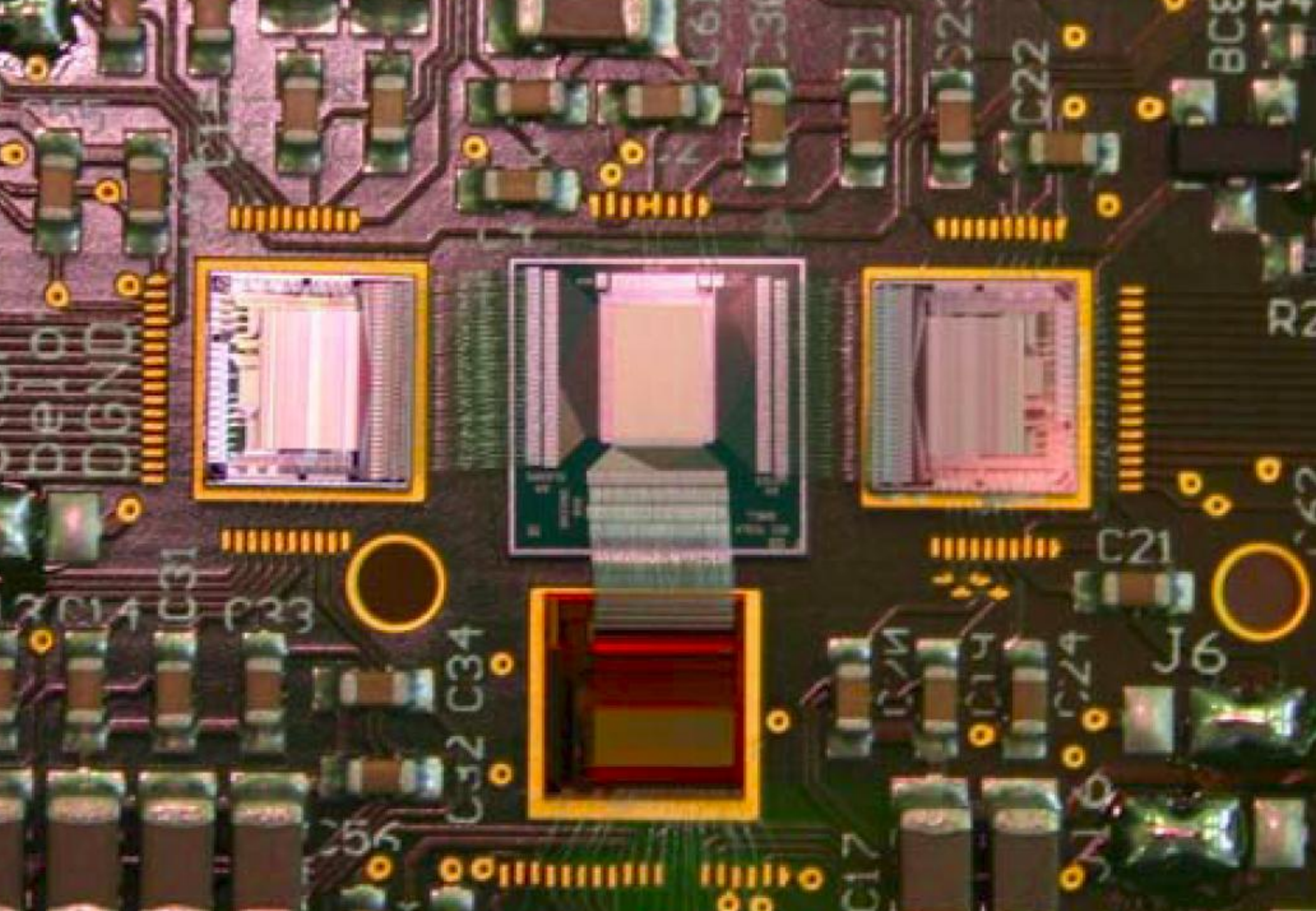
  merge currents: (1) – (2)

- **<u>all other rows OFF</u>**

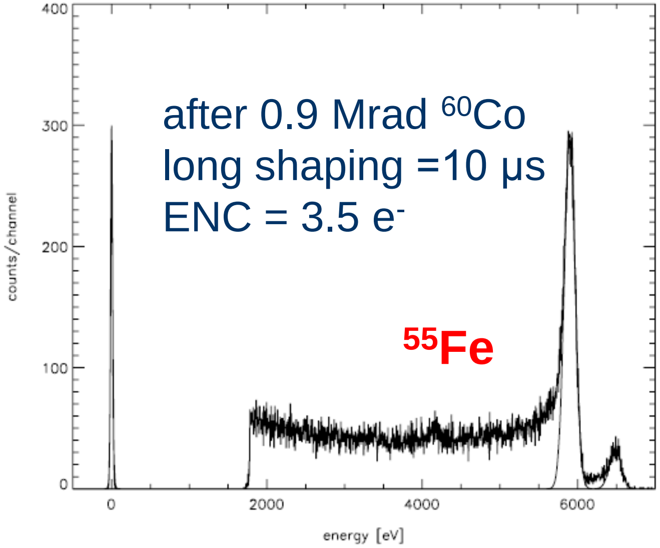
  still active for signals

  → low power !

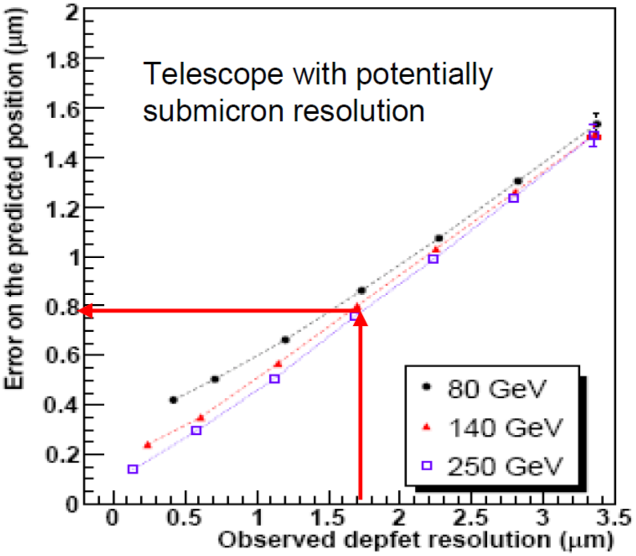
  (60 mW/cm^2)


C22
BC8
R2
C21
J6
C31
C14
C33
C34
C32
C56
C24
C17

DEPFET pixels: some features



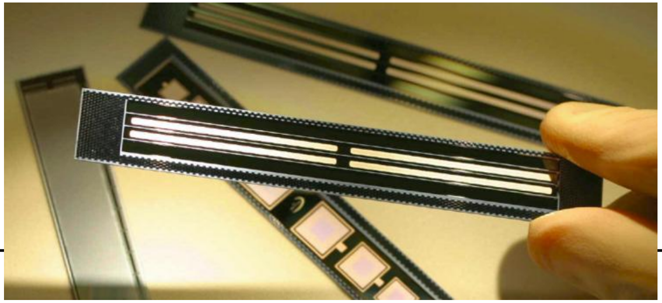
J. Velthuis et al., IEEE TNS 2007



see talk by Petr Kodys

Developments are for ILC → superBelle

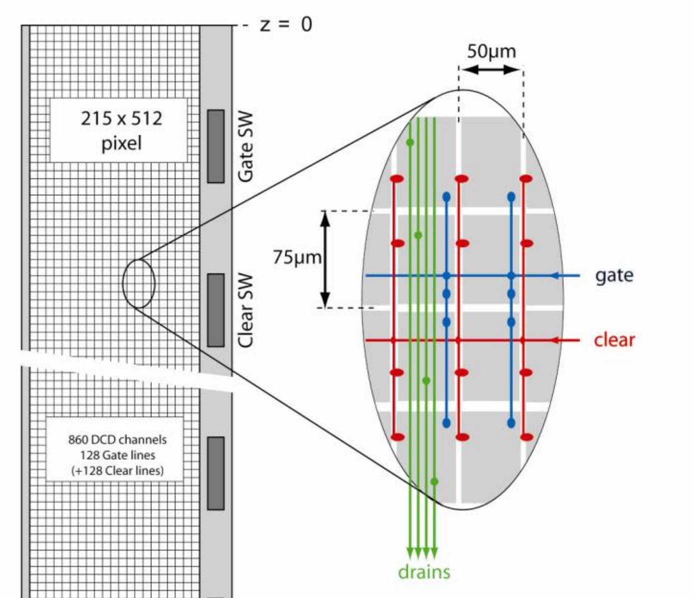
- **low noise**
  - 1.6 e$^-$ for long shaping times (μs),
  - goal: ~200e for fast R/O
  - for ILC/superBelle R/O speeds (~12 MHz line rate) S/N = 120 for 450 μm thick sensors (test beam) → goal S/N = 20 - 40 for 50 μm thick sensors
- **irradiation** (0.9 Mrad γ, 3 x 10^{12} p/cm^2, 2 x 10^{11} n/cm^2)
  - threshold shifts (~4 V) – can be compensated (note: only 1 transistor per pixel)
  - leakage current increase → 20 - 95 e$^-$
- **space resolution:** < 2 μm
- **material:** < 0.15% X_0 per detector layer (50 μm thin)

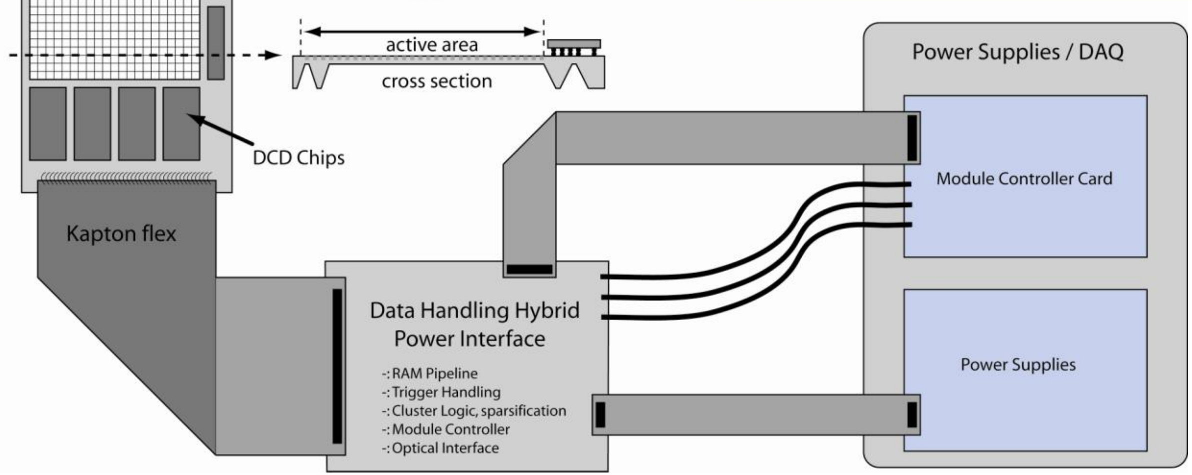


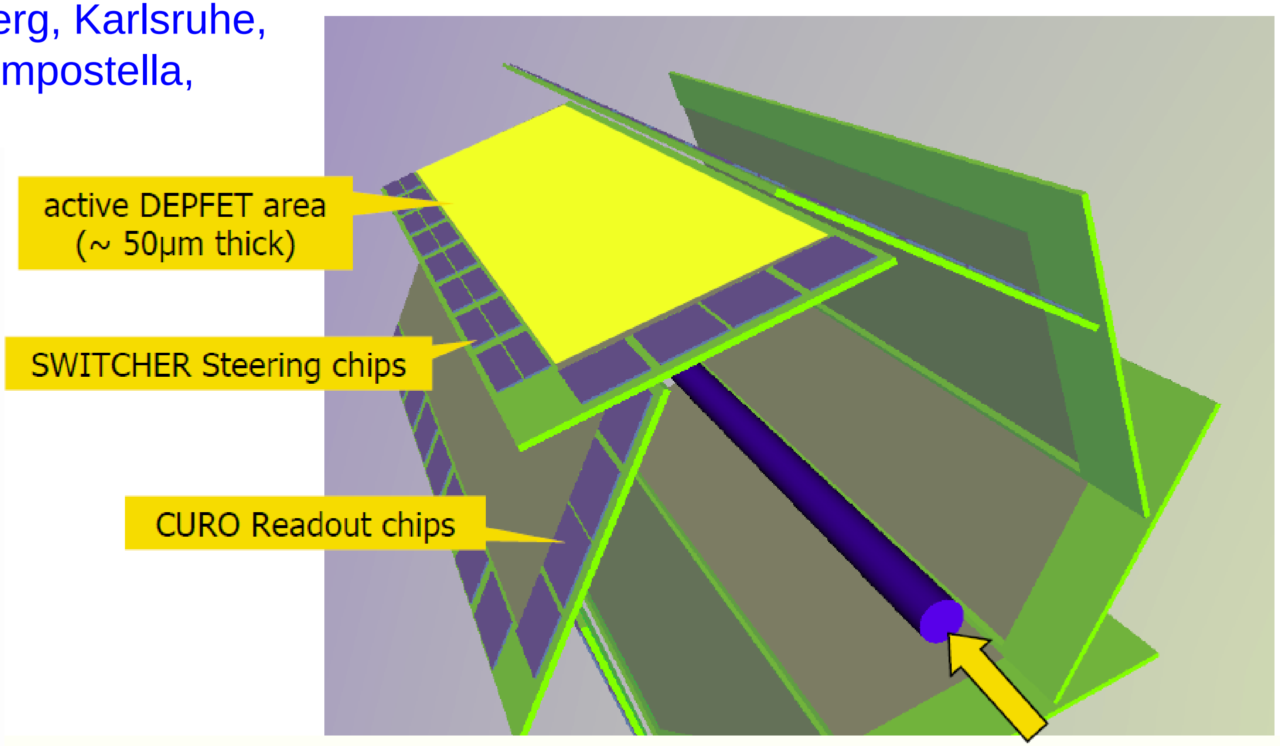
proven thinning process
(anisotropic deep etching)

DEPFET pixels for superBelle

Barcelona, Bonn, Göttingen, Heidelberg, Karlsruhe, MPI Munich, Prague, Santiago de Compostella, Valencia



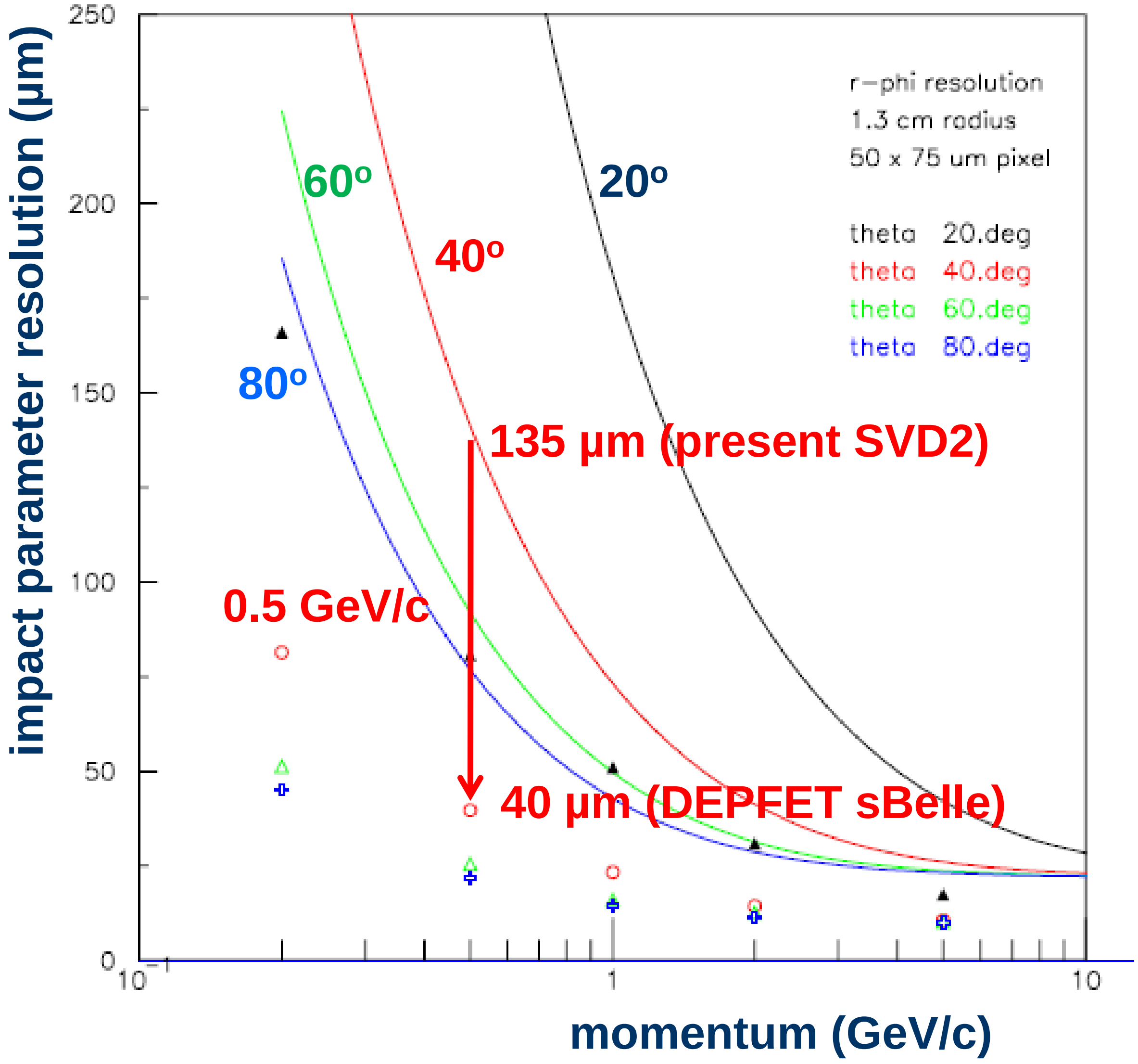




to cope with hit rate (400 kHz/mm^2) …

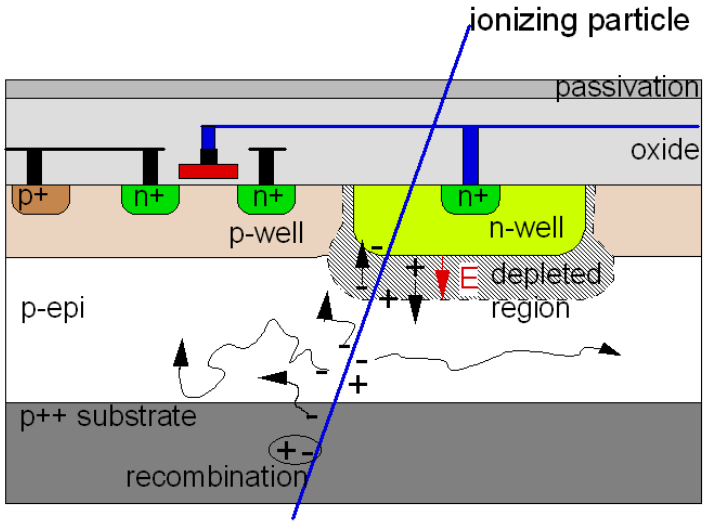
- larger pixels (50 x 75 µm^2)
- read out at both sides and 4 pixels in parallel (x 8)
- 80 ns per row (sample/clear/sample)
- 1 Gbit/s module data rate

DEPFET pixels for superBelle: IP - resolution



simulation

MAPS-epi



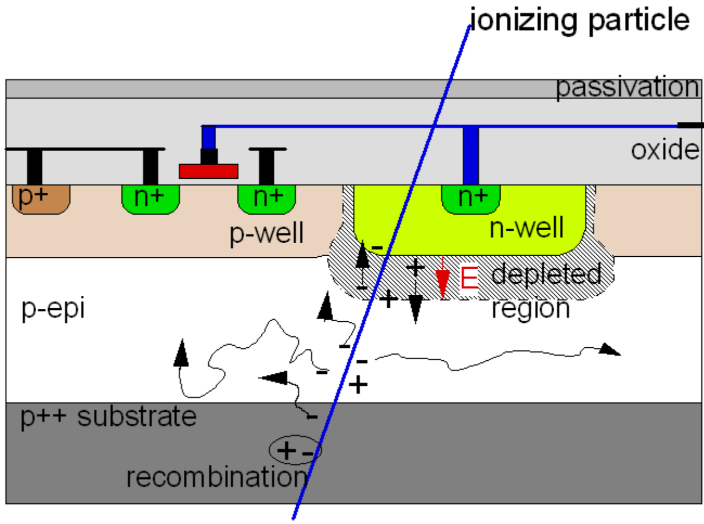
Meynants, Diericks, Scheffer, SPIE 3410:68-76 (1998)
R. Turchetta, NIM-A 458:677-689 (2001)

many activities: France, UK, US, Italy
(MAPS, CAPS, FAPS …..)

MAPS vs Hybrid Pix	MAPS	Hybrid Pixel Sensors
Granularity	+	-
Material budget	+	-
Readout speed	+-	++
Radiation tolerance	+-	++

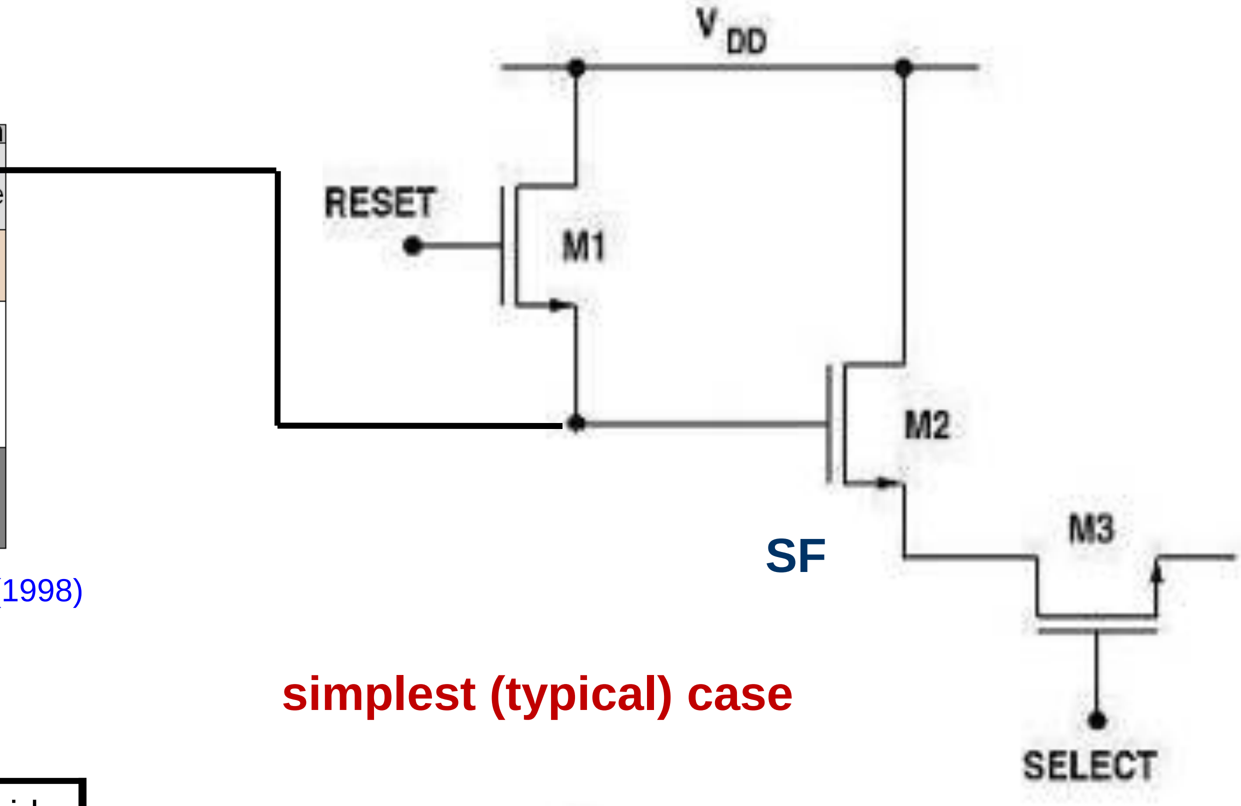
- Sensor and signal processing are integrated in the same silicon wafer
  - ✓ commercial CMOS technology standard
- Signal created in low-doped epitaxial layer (~10-15 µm, e.g. AMS 0.35 µm)
  - ❖ MIP signal <1000 electrons → challenge for IC design
- Q - collection by thermal diffusion (~100 ns), reflective boundaries at p-well and substrate, collected at n-well/epi junction
  → charge spread to several pixels
- 100% fill-factor (note definition), thin (~50 µm)
- small pixel sizes (pitch 20 – 30 µm):
  → a “must” and a virtue → few µm resolution!
- Only NMOS transistors possible in active area (due to n-well/epi collection diode)

MAPS-epi



Meynants, Dierricks, Scheffer, SPIE 3410:68-76 (1998)
R. Turchetta, NIM-A 458:677-689 (2001)

many activities: France, UK, US, Italy
(MAPS, CAPS, FAPS …..)



simplest (typical) case

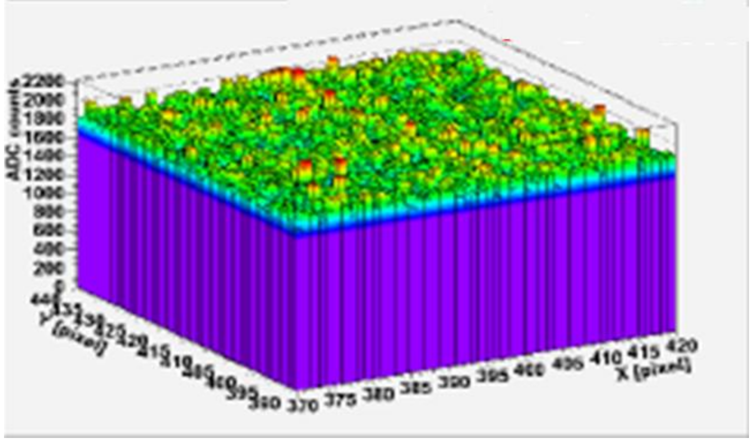
MAPS vs Hybrid Pix	MAPS	Hybrid Pixel Sensors
Granularity	+	-
Material budget	+	-
Readout speed	+-	++
Radiation tolerance	+-	++

- **readout successive frames and subtract (CDS)**
- **eliminate: base levels, 1/f noise, fixed pattern noise**

do this either offline → slow
or on-chip → current R&D

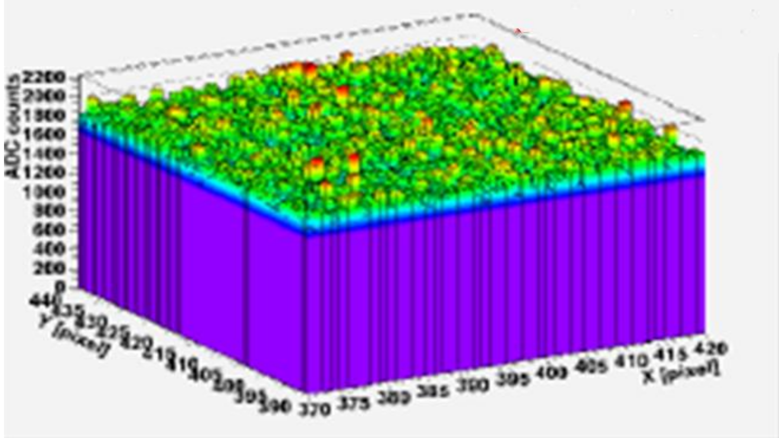
MAPS-epi: CDS correlated double sampling readout

1st frame



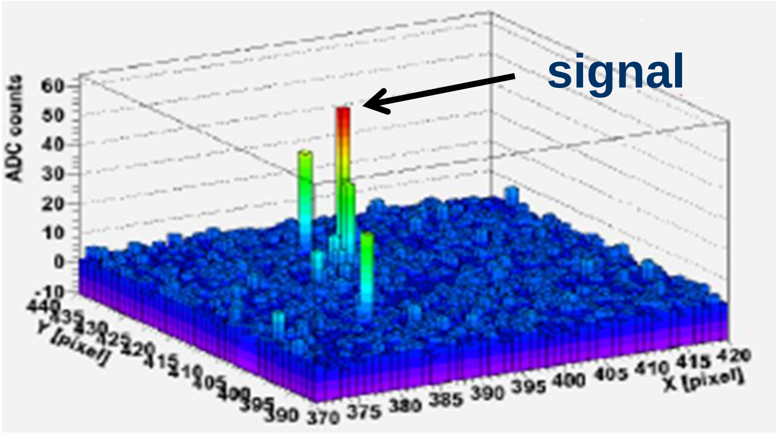
-

2nd frame



=

raw data after CDS



still: correct for pedestal and common mode

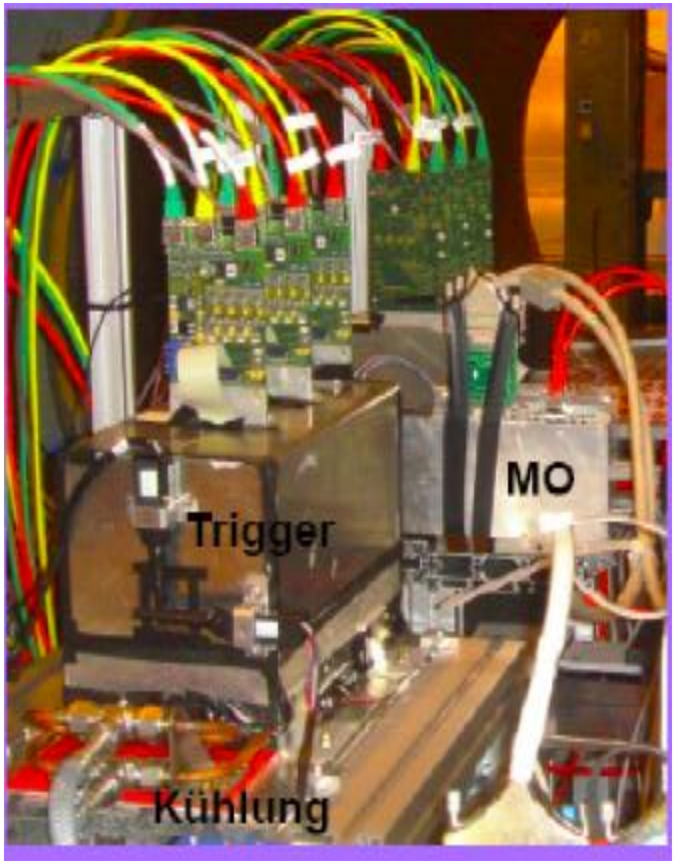
eliminate

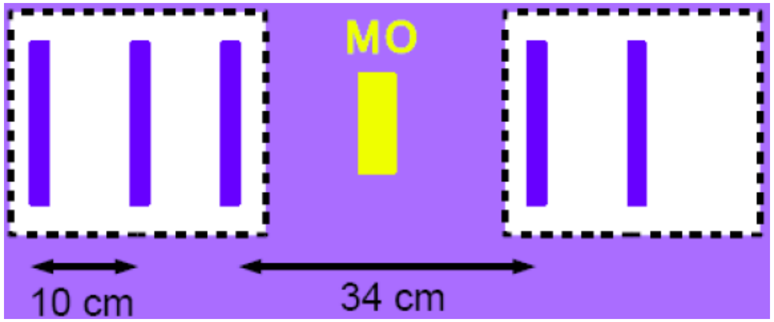
- base levels
- 1/f noise
- fixed pattern noise

so far: done offline
R&D → on-chip !

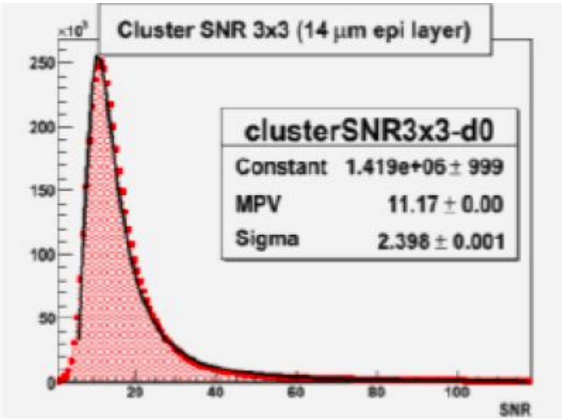
from
D. Contarato

MAPS-epi: EUDET telescope



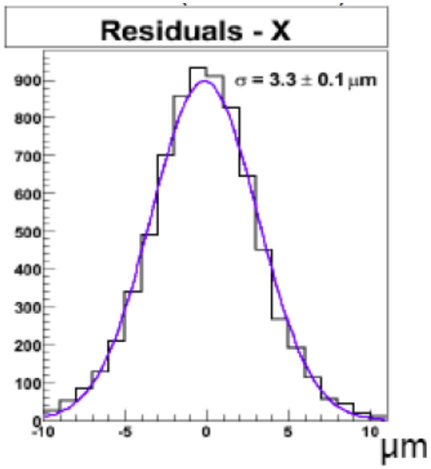


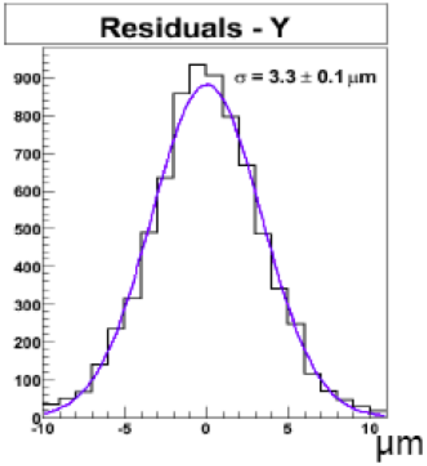
DESY, CEA, CERN, CNRS, MPI, Bonn, Heidelberg, Geneva, Bristol, INFN



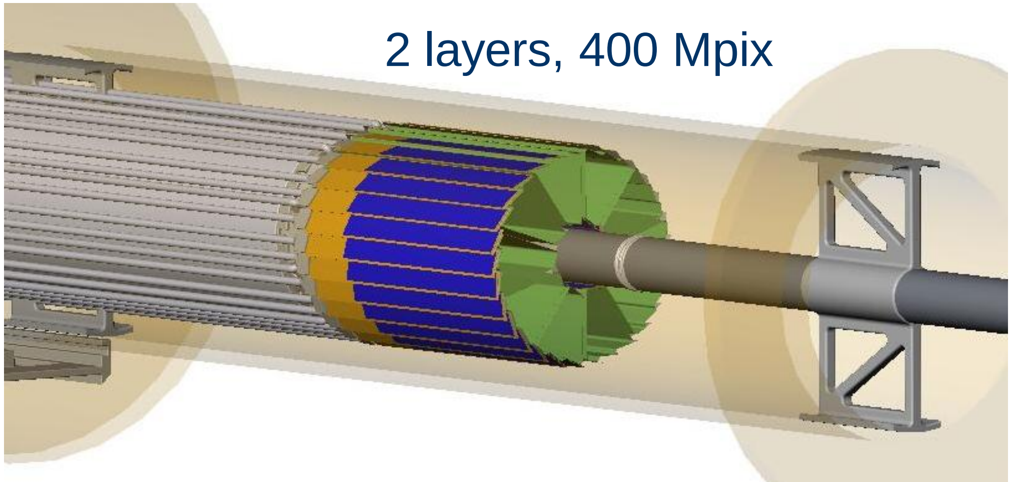
S/N ~ 11

3.3 µm resolution

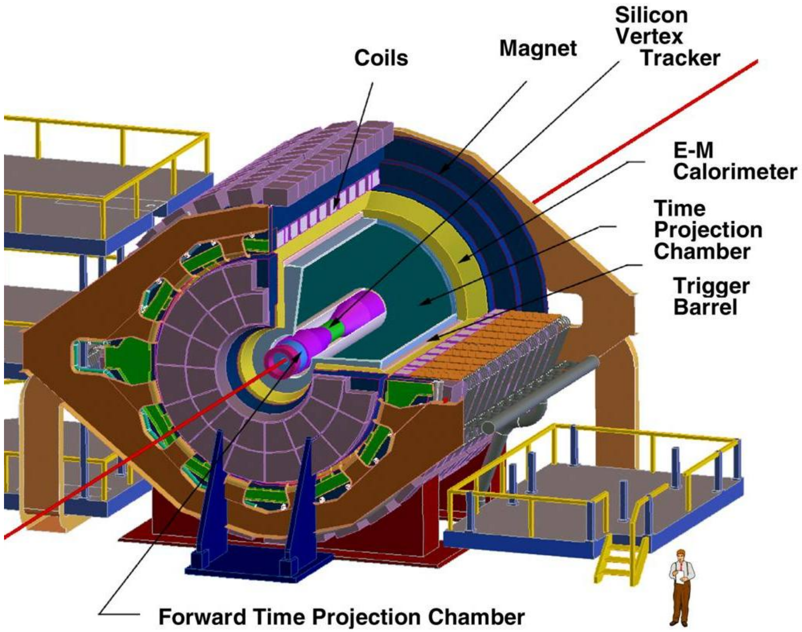




MAPS-epi → meeting the challenge: **STAR@RHIC**



ladder with 10 MAPS sensors (~ 2 2 cm each)



special feature goals

pitch 20 – 30 μm → spatial resolution < 10 μm

50 μm sensors → 0.28% radiation length/layer (!)

small power budget → 100 mW/cm^2

integration time goal: <200 μs (@ L= 8×10^{27})

must sustain 300 krad/yr and ~10^{13}/cm^2 n_{eq} /yr

groups
LBNL-Berkeley
IPHC/DAPHNIA France

MAPS-epi @STAR: current status

several prototypes

- MimoSTAR 2&3 (AMS 0.35)
- Mimosa 8/16 (TSMC 0.25/AMS 0.35)

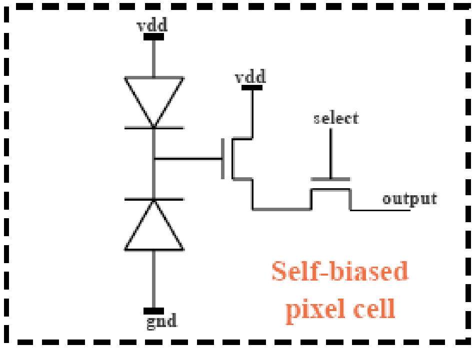
tested features

- 25 µm pitch, 128 x 32 pix
- analog versus digital R/O
  digital faster (column parallel + MUX)
  but needs discriminators

- integration time still large (~ms)
  need 200 µs

- on-chip prototyped
  - in-pixel CDS
  - column level: discrimination
    zero suppression

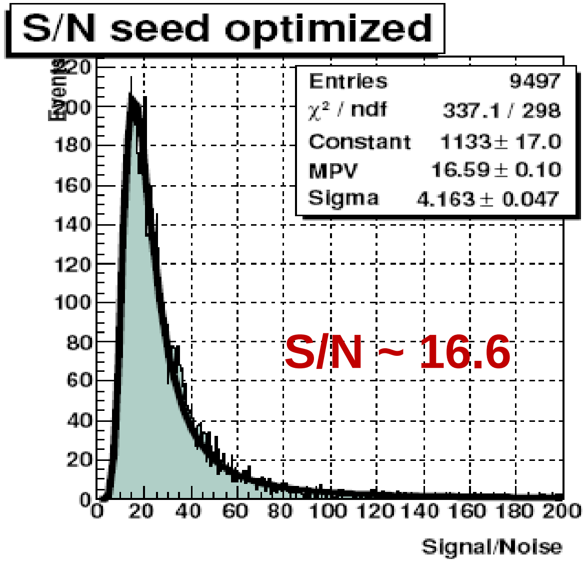
- radiation: → remove thick oxide near
  Q-collecting diode

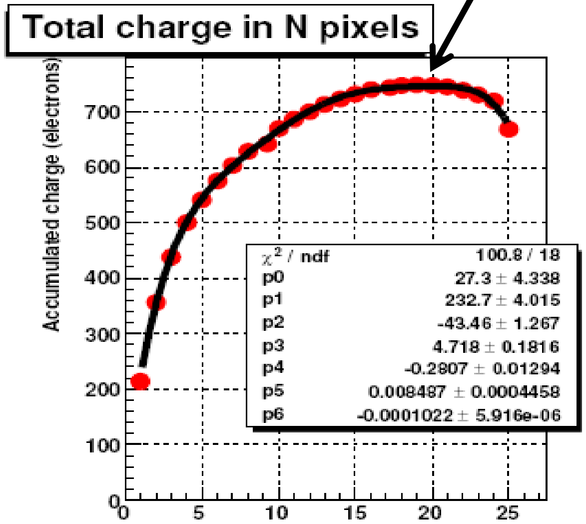


Based on tests of several different prototypes S/N>12 allows detection efficiency >99.6%

AMS 0.35

~750 e





Y. Degerli et al, IEEE TNS, vol 53, no 6, 2006, pp 3949 - 3955
Y. Degerli et al, IEEE TNS, vol 52, no 6, 2005, pp 3186 - 3193

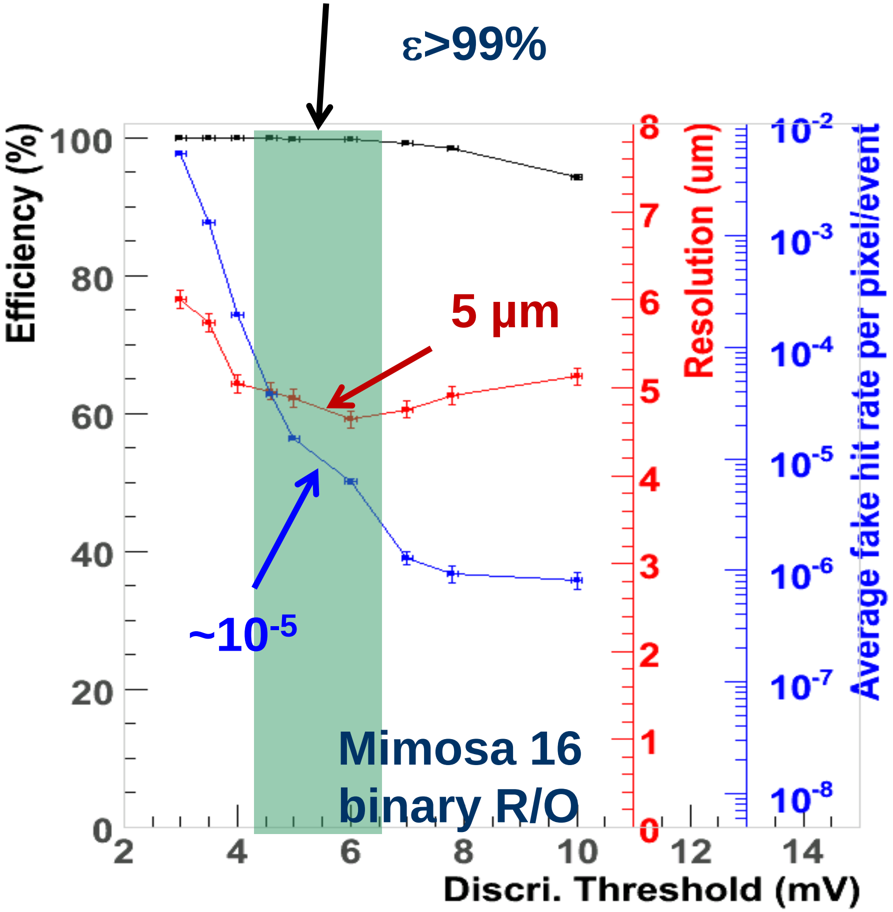
MAPS-epi @STAR: current status

several prototypes

- MimoSTAR 2&3 (AMS 0.35)
- Mimosa 8/16 (TSMC 0.25/AMS 0.35)

tested features

- 25 µm pitch, 128 x 32 pix
- analog versus digital R/O
  digital faster (column parallel + MUX)
  but needs discriminators
- integration time still large (~ms)
  need 200 µs
- on-chip prototyped
  - in-pixel CDS
  - column level: discrimination
    zero suppression
- radiation: → remove thick oxide near
  Q-collecting diode



achieved performance

Y. Degerli et al, IEEE TNS, vol 53, no 6, 2006, pp 3949 - 3955
Y. Degerli et al, IEEE TNS, vol 52, no 6, 2005, pp 3186 - 3193

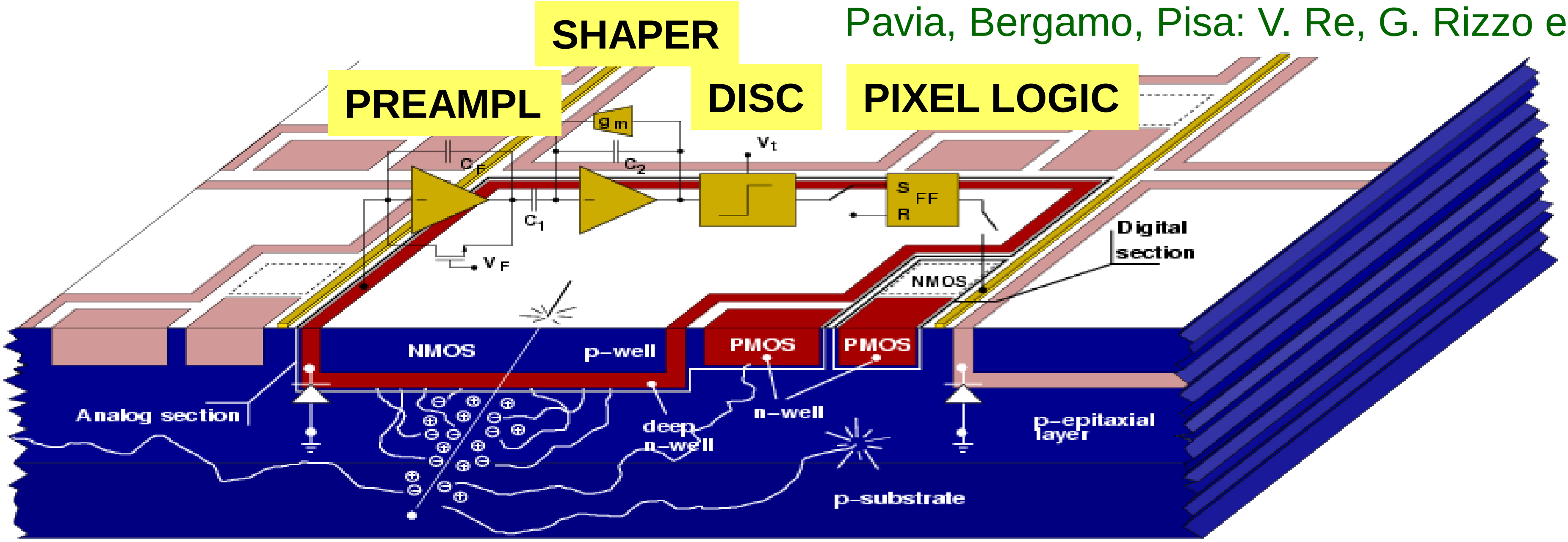
MAPS-epi: R&D trends

Main improvement R&D

1. **improve the charge collection (speed and completeness)**

2. **go to “full” CMOS also in active area**

MAPS-epi with deep n-well (→ enlarge the n-well diode)



Pavia, Bergamo, Pisa: V. Re, G. Rizzo et al.

- **Extended Deep N-well collecting electrode (STM 130 nm triple well CMOS)**
  - ✓ **obtain higher single pixel collected charge**
  - ✓ **protect charge loss to competitive N-wells**
  - ✓ **⇒ can use PMOS transistors too**

✓ **complete single pixel processing chain (CSA + Shaper + Discr. + Logic) in active area**

❖ **Fill factor (note definition) = DNW/total n-well area ~90% in the prototype structures**

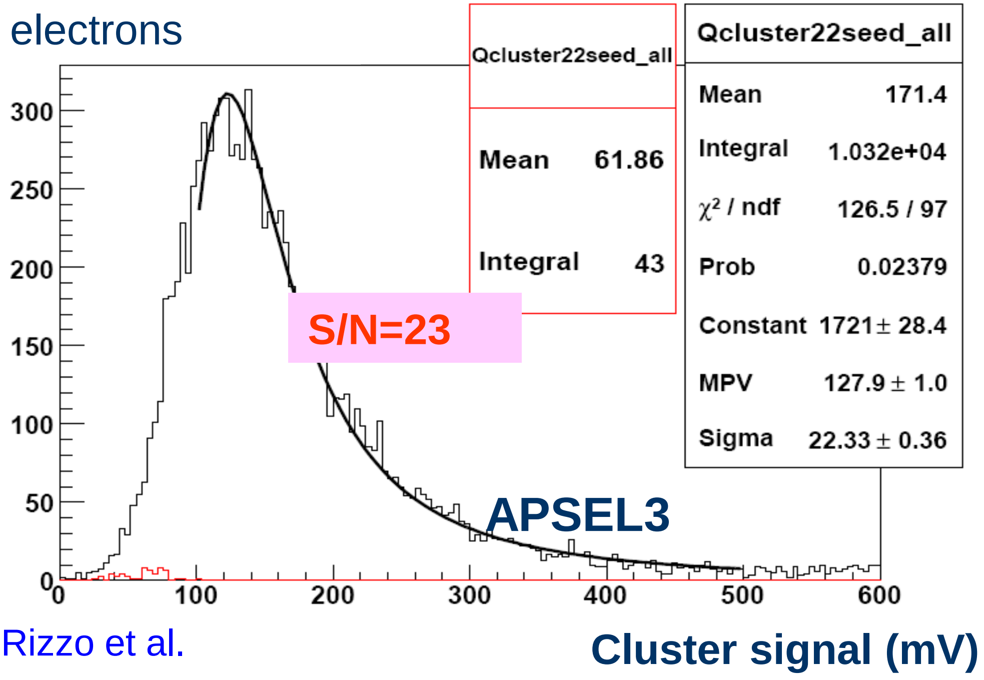
see talk by Gianluca TRAVERSI

MAPS-epi with deep n-well

Pavia, Bergamo, Pisa: V. Re, G. Rizzo et al.

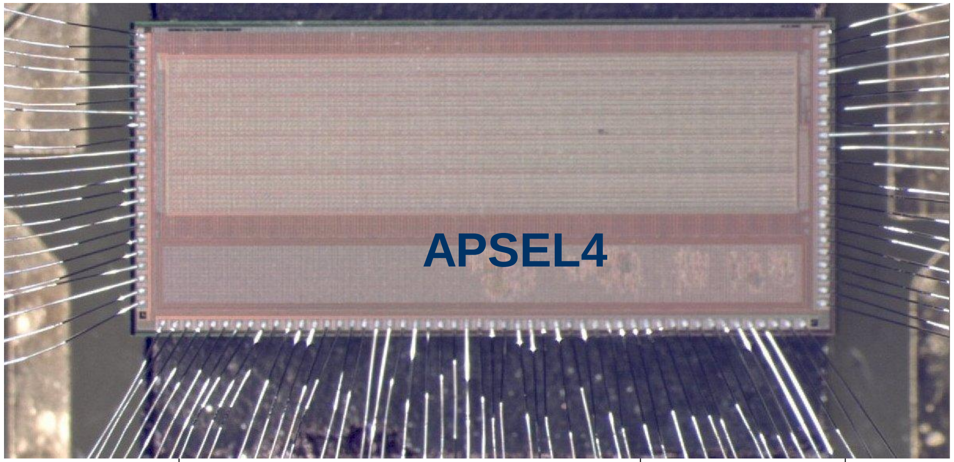
- **Ambitious goal: a monolithic pixel sensor with similar readout functionalities as with hybrid pixels (sparsification, time stamping)**
- **Proof of principle with APSEL chip prototypes (STM 130 nm triple well CMOS)**
- **APSEL4: 32x128 matrix, sparse R/O and time stamping**

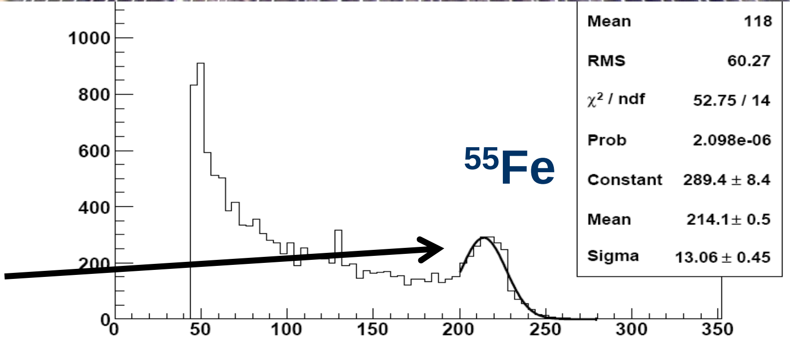
^{90}Sr electrons



G. Rizzo et al.

32x128 pixels - 50 µm pixel pitch

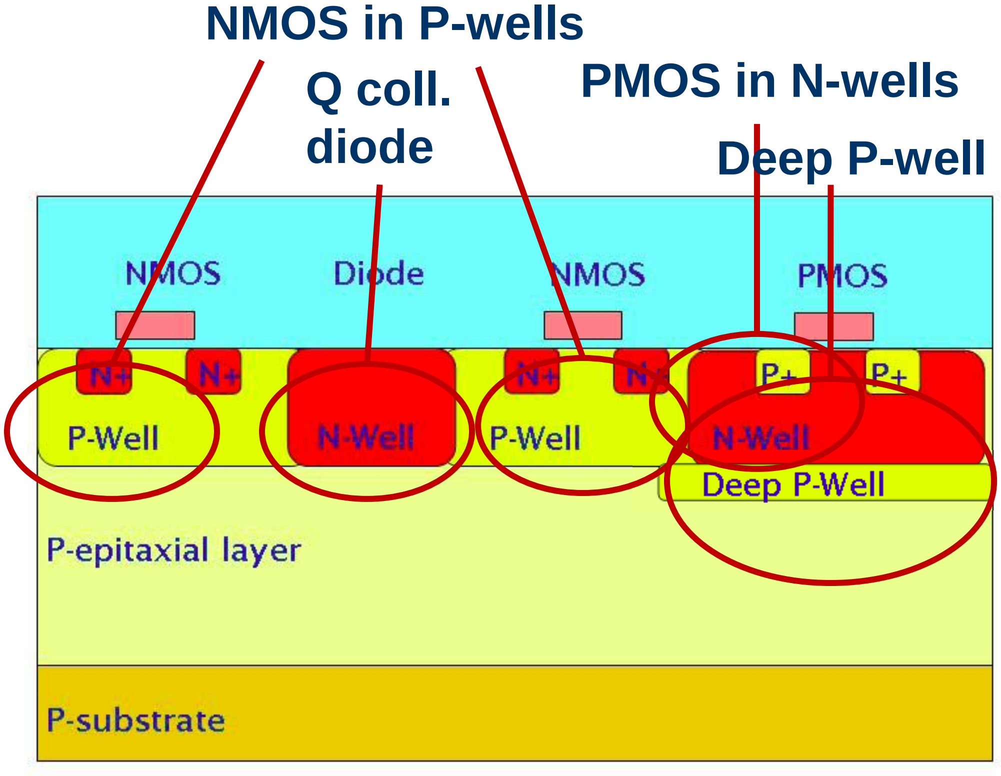




5.9 keV line (1640 e-) with charge totally collected by a single pixel

MAPS-epi with deep p-well (→ shield the PMOS N-wells)

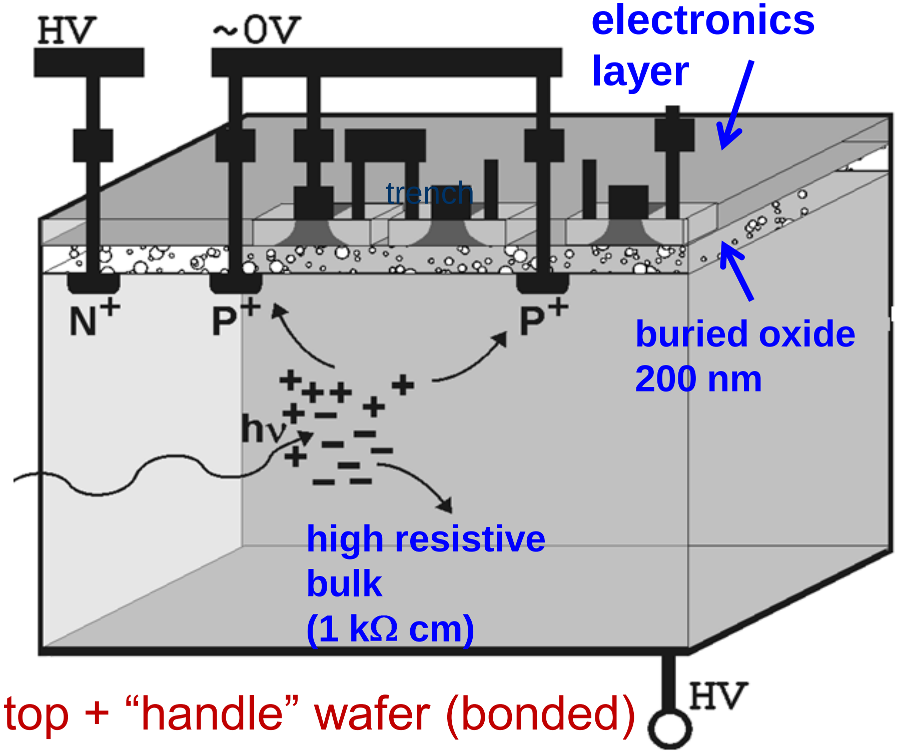
RAL, ICL, UBirmingham, J.P. Crooks, …, R. Turchetta et al. IEEE TNS 2007 & Sensors (2008), ISSN 1424-8820



INMAPS quadrupel well 0.18 µm CMOS process (6 metals)

- use deep p-implant (p-well) to shield the n-wells that contain PMOS transistors
- only diode n-well still exposed to charge from the epi-layer
- fill-factor is 100%
- deep-p cannot be made too small → pixel size not too small
- several designs with full signal processing submitted (>150 transistors) + tested o.k
  - e.g. CSA + shaper + comp. + logic
  - 50 µm pixel pitch
- first prototype tests encouraging
  - Q- collection in n-well diode increased by factor more than 2

MAPS-SoI



top + “handle” wafer (bonded)

MAPS **SoI vs epi**	epi	SoI
Granularity	+	+
Material budget	+	+
S/N	-	++
Level of maturity	+	- -

SoI

- A thin Si layer (~100 nm) isolated with SiO_2 (each transistor in its own isolated island, shallow trench isolation, no junctions to bulk)

MAPS-SoI:

- A bonded wafer with high-Ω substrate + low-Ω top Si, separated by a buried oxide layer
  - ✓ standard CMOS (NMOS, PMOS, MIM cap…) can be used
  - ✓ efficient use of area for electronics
- vertical via contacts reaching through to implants in the high resistivity wafer
  - ✓ no bump bonding
  - ✓ small pixel size possible
- use of handle wafer in partial or full depletion determined by backside voltage

➡ **full CMOS** in active area
charge collection in **fully depleted bulk**

see also talk by D. Contarato

MAPS-SoI

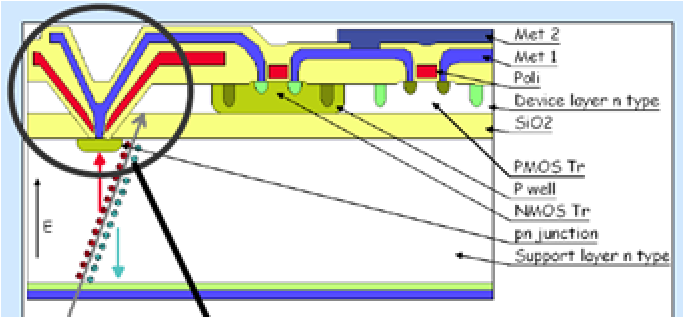
1995: F.X.Pengg, "Monolithic Silicon Pixel Detector in SOI Technology", PhD thesis, University of Linz, Austria, (1996)

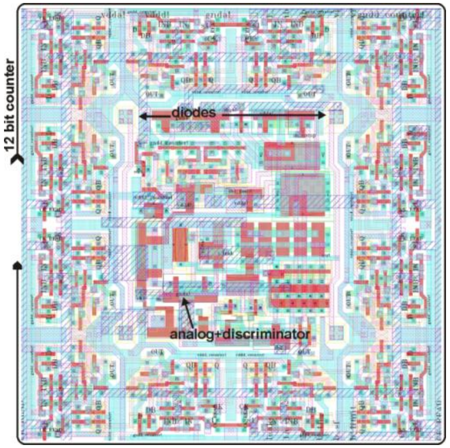
2003: W. Kucewicz et al. Nucl.Instrum.Meth.A549:112-116,2005.

New initiative:
FERMILAB (R. Yarema, G. Deptuch et al.)
+ Japan + LBNL + Hawaii

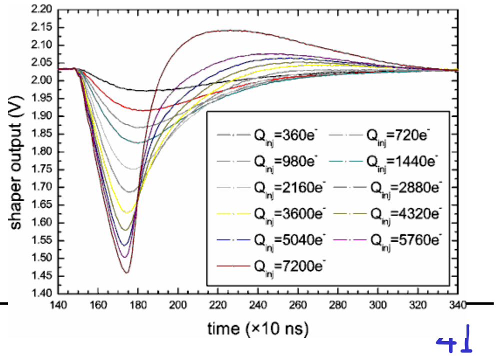
with commercial vendors (not many !! … "change in process flow")
→ OKI (150 nm & 200 nm)

Status: prototype experience → feasilibilty study
- many design variations submitted
  - for HEP applications: single particle sensitivity
  - for imaging applications: photon counting
- full blown CMOS electronics
  - CSA + shaper + discriminator + (counter)





e.g.: 64x64 pix, 26 µm
CSA + shaper + discr.

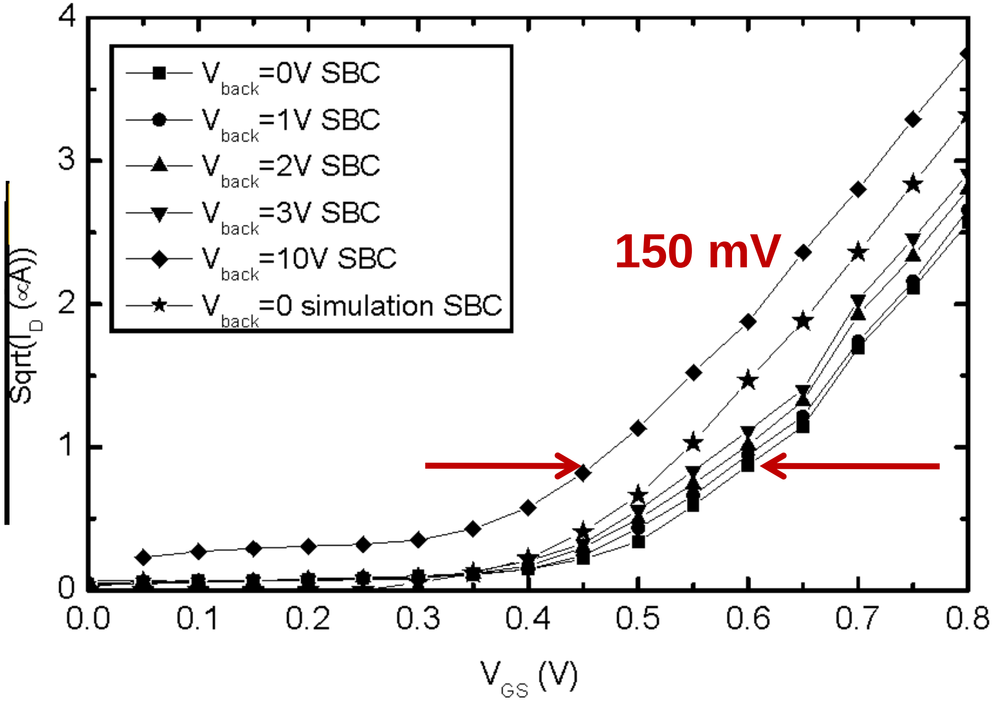


MAPS-SoI

the main problem: back gate effect

fully depleted high-Ω part couples into the channel ➔ acts as second gate
➔ substrate biasing leads to transistor threshold shifts

simplified



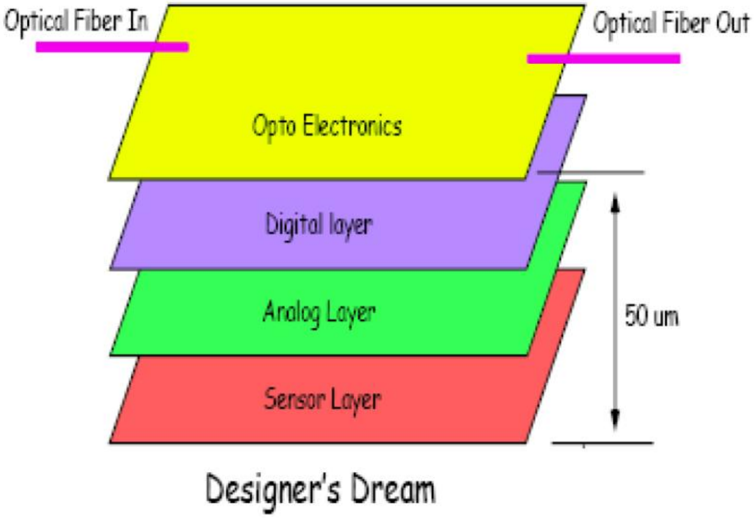
Si (low Ω)
SiO_2

Si (high Ω)

ideas:

- **need thicker buried oxide layer**
- **use less V_{back} → partial depletion**
- **use dense matrix of p^+ implants to lower potential at the surface**

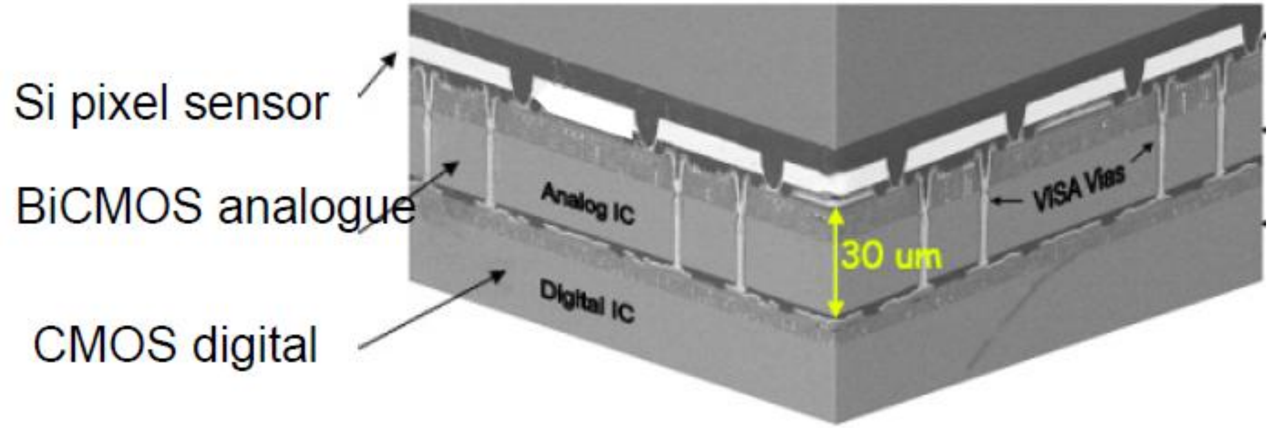
3D integration



- **several (tiers) of thinned semiconductor layers interconnected to form a monolithic unity**

- **different layers can be made in different technologies (high ohmic sensor, BiCMOS, deep sub-µ-CMOS, SiGe, opto-process, …)**

- **driven by industry**
  - ✓ **reduced R,L and C → improves speed**
  - ✓ **reduced interconnect power, x-talk**
  - ✓ **reduced size**



first initiative @ Fermilab

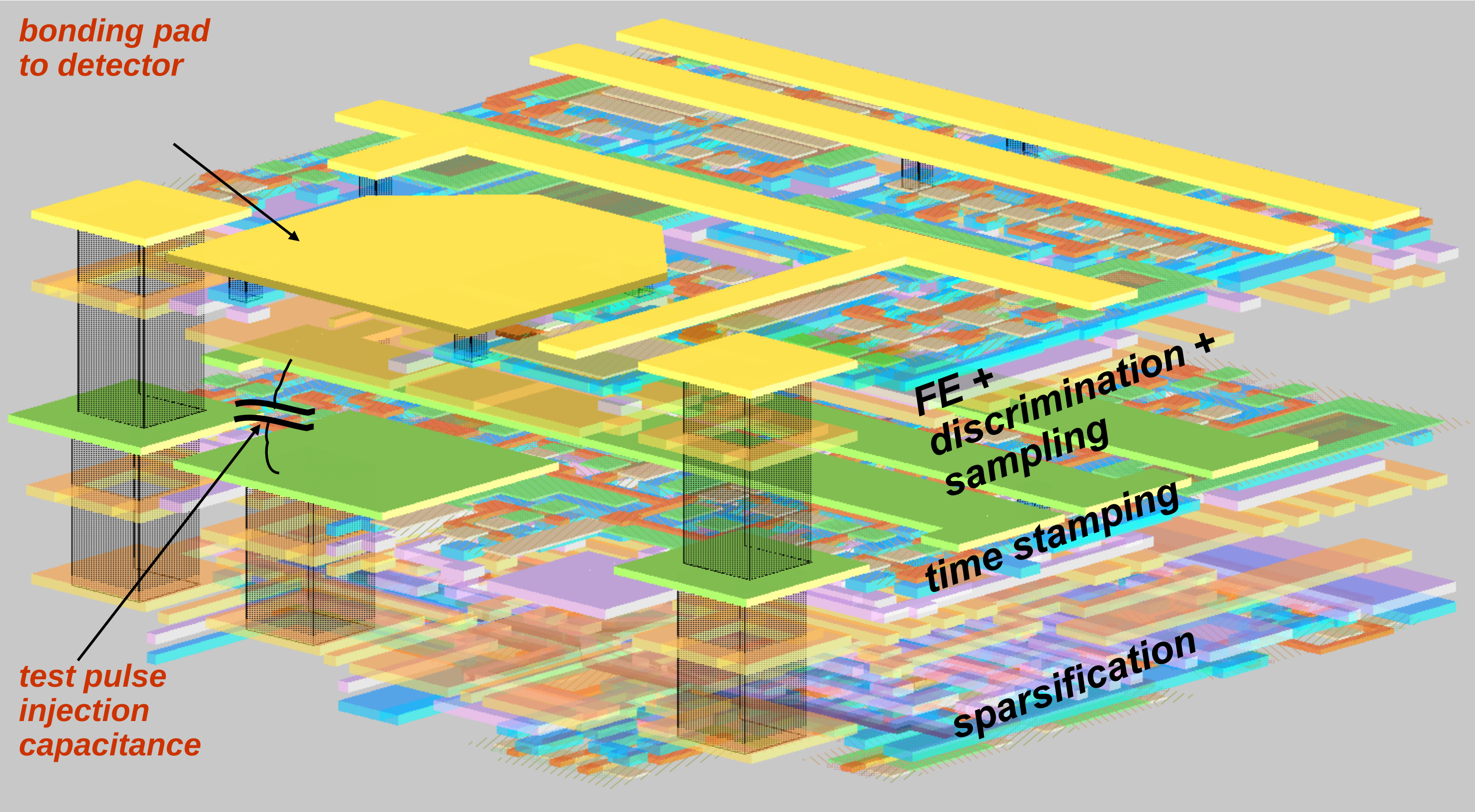
France (many groups)
Germany (MPI, Bonn)
following

3D integration

heavy R&D at Fermilab: R. Yarema, G. Deptuch et al. readout chip with time stamping and sparsification

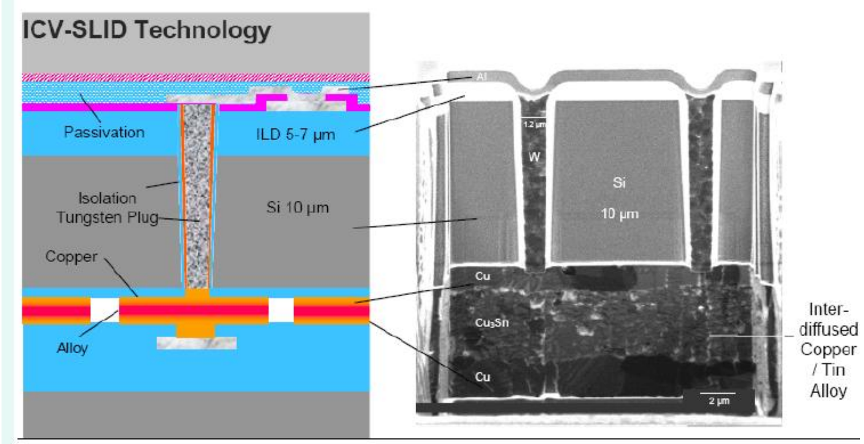
3 tiers (no sensor yet)

attempts with several foundries: Tezzaron, Chartered, IZM, RTI, Ziptronix, MITLL



VIP: layout view with 3D Design Tool by Micro Magic

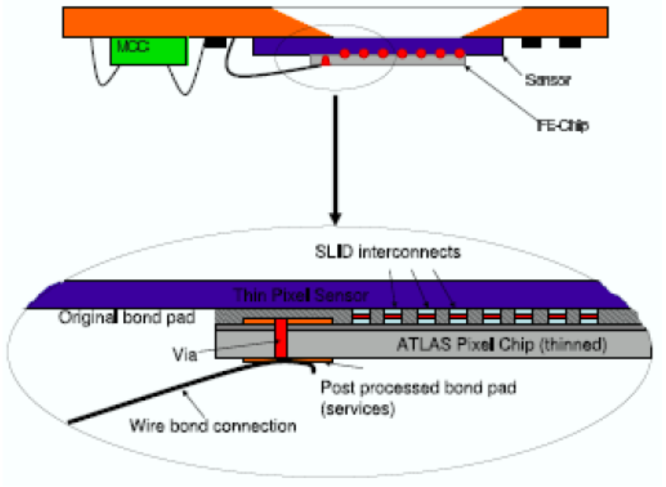
3D integration



3D integration post – processing

… ICV = Inter Chip Vias
… TSV = Through Silicon Vias

- hole etching and chip thinning
- via formation with W-plugs
- 2.5 Ω/per via



MPI-Munich & IZM/Munich

- build demonstrator using ATLAS pixel chip and pixel sensors made using ICV + SLID technology

Bonn & IZM/Berlin

–use TSV for new sLHC-ATLAS module concepts

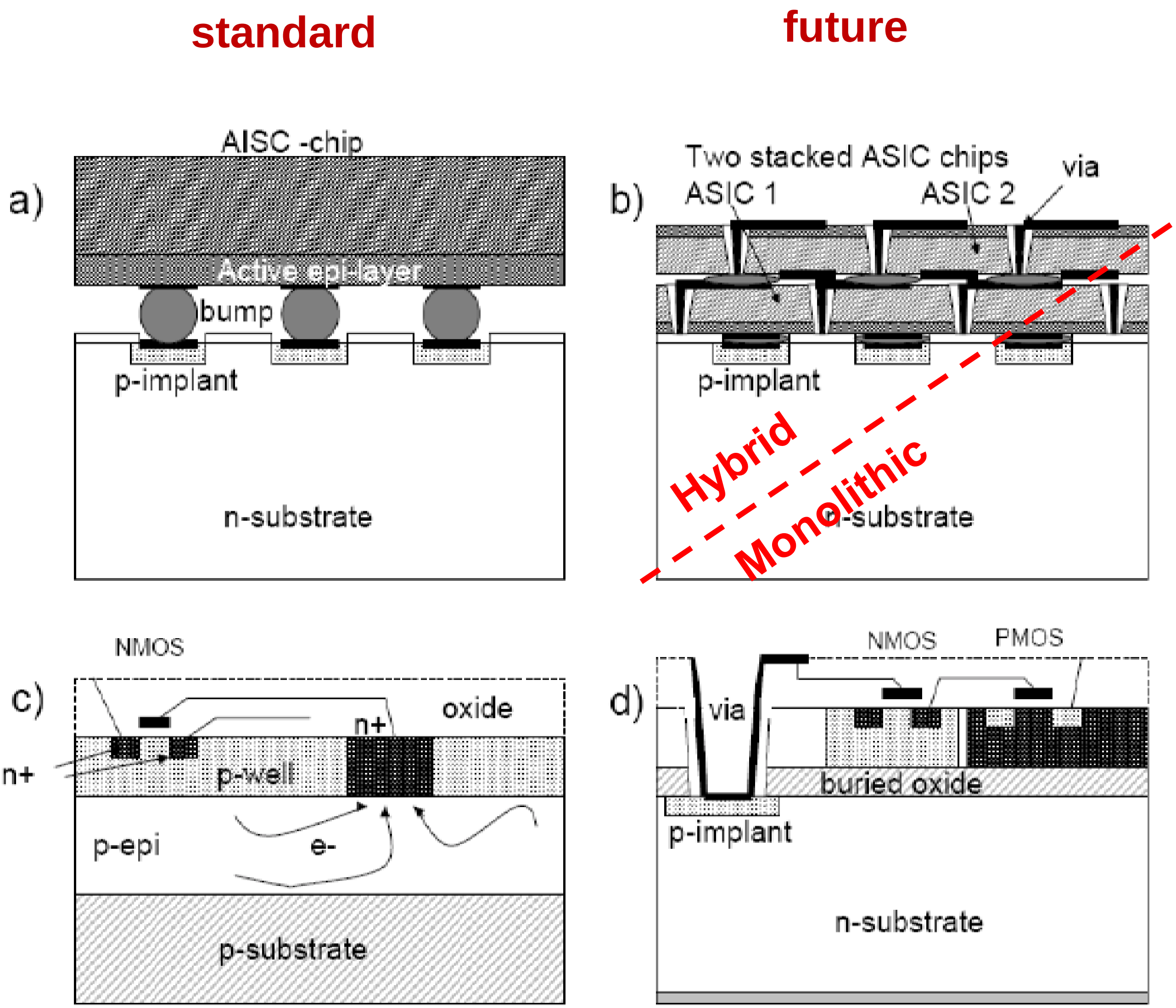
Conclusions

Hybrid pixels

- matured with LHC
- only choice for sLHC
- needs <u>heavy R&D</u> on:
  - sensor materials
  - ICs and modules
  - 3D integration

Monolithic

- first real detectors in focus
- “dream” is getting closer
- needs <u>heavy R&D</u> on:
  - full (CMOS) integration
  - radiation tolerance



Thanks for talk material and discussions

- **Woitek Dulinski**
- **Michal Szelezniak**
- **Grzegorz Deptuch**
- **Laci Andricek**
- **Michael Moll**
- **Renato Turchetta**
- **Hans-Günther Moser**
- **Hans Krüger**
- **Fabian Hügging**
- **Marlon Barbero**
- **David Arutinov**
- **Giovanni Darbo**
- **Maurice Garcia-Sciveres**
- **Cinzia da Via'**
- **Valerio Re**
- **Harris Kagan**

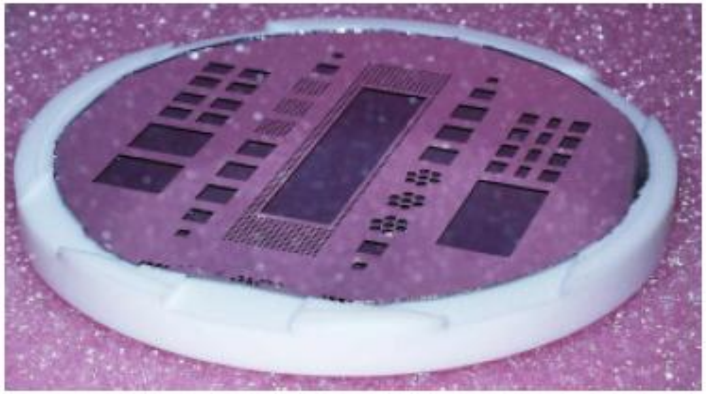
Backup Slides

Making thin Sensors

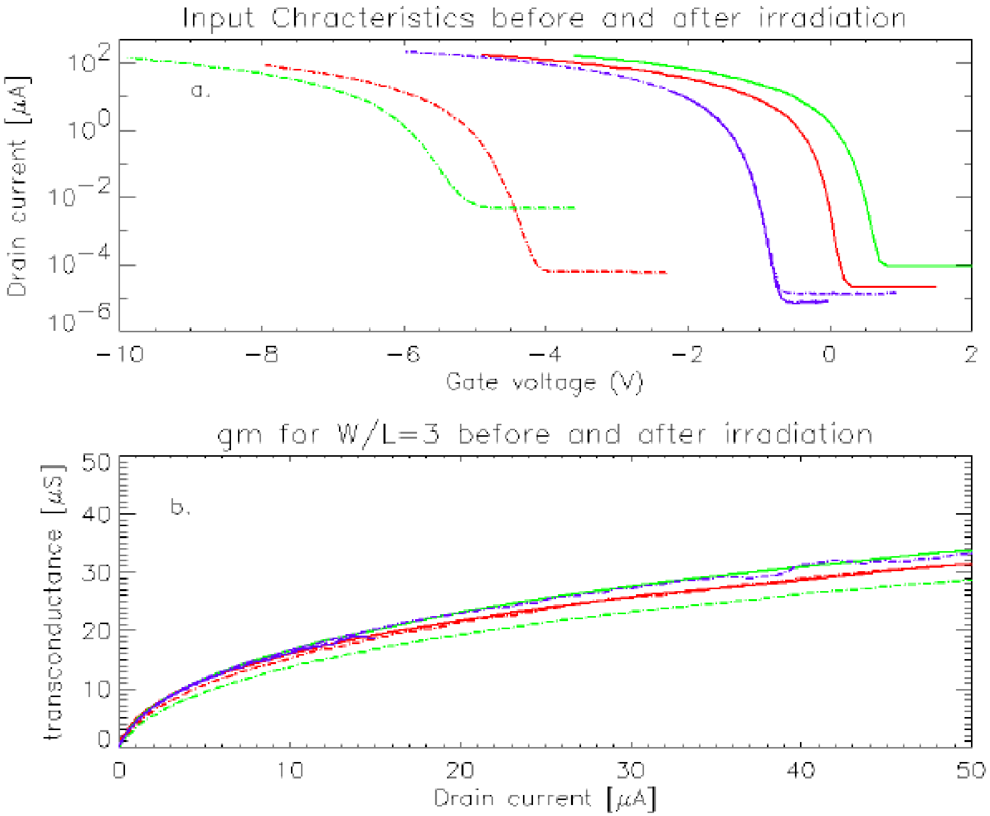
- A novel technology to produce detectors with thin active area has been developed and prototyped (L. Andricek)

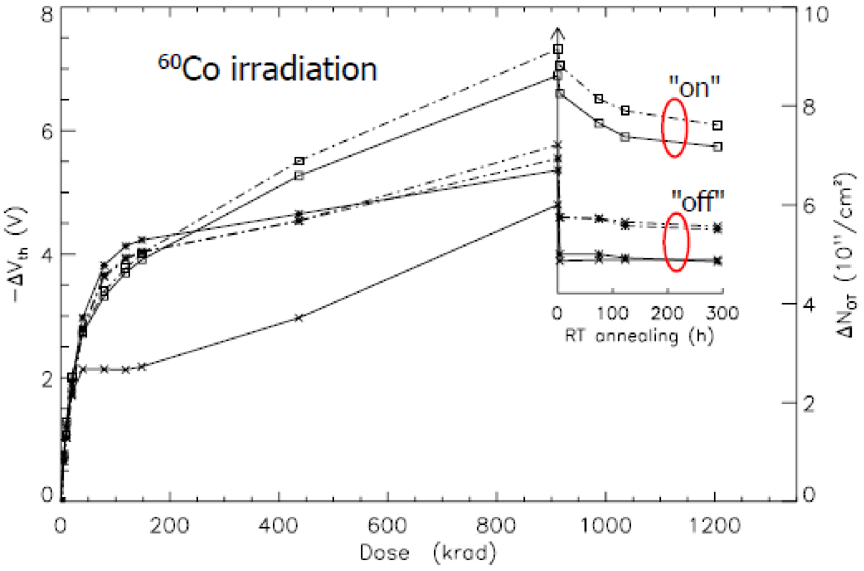
1. implant backside on sensor wafer
2. bond wafers with SiO_2 in between
3. thin sensor side to desired thick.
4. process DEPFETs on top side
5. etch backside up to oxide/implant

first 'dummy' samples:
50µm silicon with 350µm frame



thinned diode structures:
leakage current: <1nA /cm^2





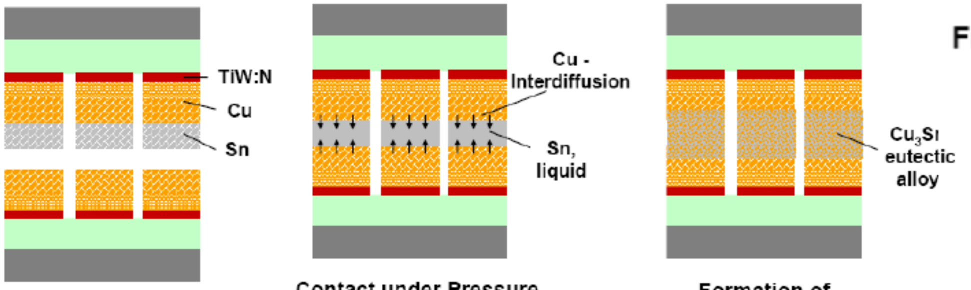
irradiation	TID / NIEL fluence	ΔV_{th}	g_m	I_{Leak} in int. gate at RT$^{(*)}$
gamma ^{60}Co	913 krad / ~ 0	~-4V	unchanged	156 fA
neutron	~ 0 / 2.4x10^{11} n/cm^2	~ 0	unchanged	1.4 pA
proton	283krad / 3x10^{12} n/cm^2	~-5V	~ -15%	26 pA

(*) 5..22 fA non irrad.

IZM SLID Process, ICV

Metallization SLID (Solid Liquid Interdiffusion)

Fraunhofer IZM
Institut
Zuverlässigkeit und
Mikrointegration

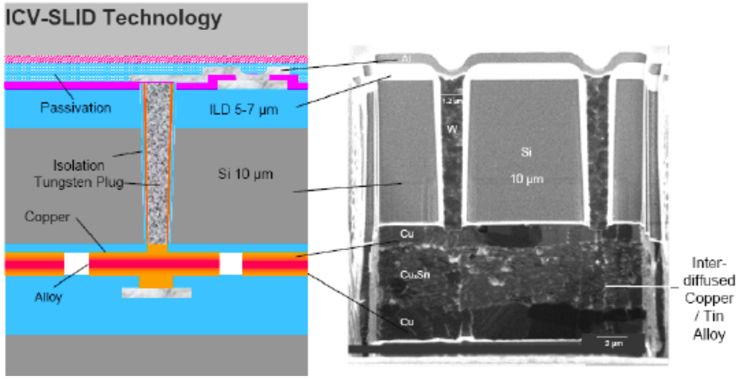


Through Mask Electroplating

Contact under Pressure and Heat
~ 5 bar, 260 – 300 °C (Sn-melt)

Formation of Eutectic Alloy; T_{melt} > 600 °C

- •Alternative to bump bonding (less process steps "low cost" (IZM)).
- •Small pitch possible (< 20 µm, depending on pick & place precision).
- •Stacking possible (next bonding process does not affect previous bond).
- •Wafer to wafer and chip to wafer possible.



ICV = Inter Chip Vias

- •Hole etching and chip thinning
- •Via formation with W-plugs.
- •Face to face or die up connections.
- •2.5 Ohm/per via (including SLID).
- •No significant impact on chip performance (MOS transistors).