

Progress on the Aberystwyth Electron Counting Array

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Abstract

An extended electron counting detector with a linear array of 1 536 pixels across an active area of 38mm x 5mm is presented. Also presented is an improved control electronics package, based on the National Instruments Compact RIO instrument programmed in Labview. Also presented is an application of the existing detector with 768 pixels, showing how the improvement in detection technology enables fresh insights into the formation of aluminium contacts on diamond.

Keywords: Multianode detector; microchannel plate, count rate, dark noise

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1. Introduction

Photoelectron spectroscopy is a technique that provides a wealth of parallel information and can be applied to a wide range of materials [1]. For example, it is widely applied to semiconducting materials to monitor changes in surface composition, electronic structure, interface energetics, interface bonding and thin film growth. The surface under investigation is illuminated with a source of X-rays in ultra-high vacuum (UHV) conditions and the electrons liberated from the material are measured for kinetic energy using an electro-static analyzer. Conventional analysis is performed by scanning the analyzer potentials causing the spectrum of dispersed electrons within the analyzer to move across one or more point detectors.

By using an efficient detector for the electrons, it is possible to apply the photoelectron spectroscopy technique with sufficient time resolution to study the dynamics of surface processes in-situ. A portion of the photoelectron spectrum is imaged onto the surface of the detector and data collected from all points within the portion in parallel.

The device presented here is based on established microchannel plate (MCP) technology coupled with modern digital readout circuitry. An electron incident on the microchannel plate gives rise to an amplified charge cloud at the opposite face that is collected by anodes on the array detector. Each anode is connected to an electronics channel comprising a charge sensitive amplifier, discriminator and 16-bit counter.

2. The Aberystwyth 1 536 pixel detector

A SPECS PhoibOS 100 hemispherical electron analyser has been acquired at Aberystwyth for use in electron spectroscopy applications. The analyzer has a mean radius of 100mm and a separation between the hemispheres of 50mm. Taking into account fringing fields there is a useable distance of approximately 40mm between the hemispheres at the focal plane. It is desirable to utilize as much of this area as possible for electron collection, both to maximize collection efficiency and also to permit the simultaneous collection of electrons across as large a section of the spectrum as possible for given analyzer potentials.

The existing detector developed at Aberystwyth University [2] offers 768 pixels arranged across a collection area of 19.2 x 3mm. The readout ASIC for this detector was designed to allow multiple ASICs to be abutted on a substrate behind the MCP stack. In this application, abutting 2 detectors to cover the focal plane would result in the gap between the two ASICs and the resultant dead spot occurring in the centre of the focal plane. It was therefore decided to produce a single long readout ASIC to cover as much of the focal plane as possible.

The current family of silicon detector chips are fabricated on the AMI Semiconductor 0.5 μ m CMOS process accessed via the Europractice IC service and it was desired to utilize this process for the 1 536 pixel device. In common with many silicon processes, the AMI process uses a photolithography reticle which allows a maximum device size of up to 20mm on a side. It is possible to accommodate larger devices by producing more than one set of reticles which are then stitched together on the wafer in the photolithography stages to create a device limited only by yield and wafer size considerations. In such a stepped design, an additional set of tolerances manifest themselves at the reticle boundaries, resulting in a number of restrictions on the design process. In particular, no active devices are allowed to cross a stitching boundary and coarser tolerances must be employed for conductors in these locations.

The Aberystwyth detectors were designed with a multi-level bus structure to permit long arrays to be constructed by connecting the appropriate number of anode/amplifier and counter blocks at the layout stage, however the design required modification to result in a design which can be successfully separated into multiple reticles for stitching together on the wafer.

In previous versions of the detector, it was noted that the pixels at the extreme edges of the array appeared to be more responsive than the pixels towards the centre of the array. It is thought that this was due to slightly different environments surrounding the collection anodes. During fabrication, an insulating nitride layer is grown over the surface of the device and then etched back to reveal the collection electrodes and I/O pads. This results in an insulating area adjacent to the edge anodes on the array which will charge up as clouds of

electrons arrive from the rear of the MCP. This charging of the areas adjacent to the edge pixels will act to deflect subsequent charge clouds from the edges of the array onto the edge pixels. Thus the edge pixels will register events from a larger area of the focal plane than those in the centre of the array, making them more responsive.

In order to combat this effect, a conducting border is defined in the top metal layer and connected to the reference potential for the collection anodes. The opening in the insulating nitride layer is extended to include the conducting border.

A completed design for fabrication was assembled, comprising the 1 536 pixel device and a variant of the existing 768 pixel device, modified to include the modified border around the collection anodes as detailed above. A completed wafer is shown in Figure 1.

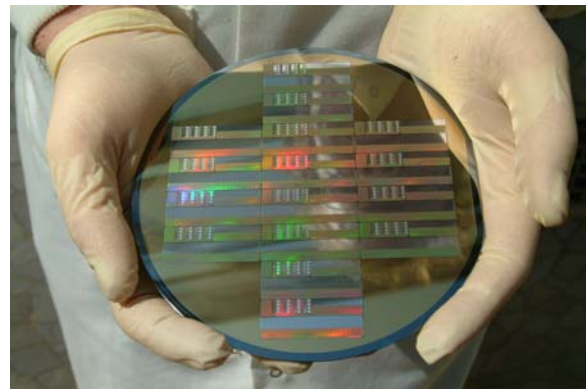


Figure 1 Wafer of Readout Devices

Initial bench testing of completed die shows the modified design to work successfully. Ceramic substrates to mount the extended array in the SPECS analyzer for in-vacuo testing are currently being procured.

3. Modified Control Electronics.

The existing control electronics for the detector were designed by the STFC Instrumentation Department and are based on an embedded iPEngine control computer [3]. The iPEngine is a Motorola power PC running Linux with I/O performed via an

Altera EPF6016 16 000 Gate FPGA. The embedded processor is connected to the detector chip via a custom circuit board containing power supplies, D/A converters and buffers. The power PC chip is programmed in C, with the FPGA programmed via the Altera Quartus software.

In order to reduce the size of the control electronics and increase performance and flexibility, a new system based on the National Instruments Compact RIO [4] hardware has been implemented. The Compact RIO system is built around a high-performance embedded processor running a real time operating system. The I/O uses plug in modules which communicate with the processor through a FPGA with 3 000 000 gates. The processor and FPGA are both programmed by means of the National Instruments Labview language.

The embedded processor communicates with the host PC by means of a fibre-optic TCP/IP link, providing electrical isolation. As well as providing the I/O path between the embedded processor and analogue and digital I/O modules, the FPGA is used to implement time-critical functions, such as the integration timer. Data from the readout chip is accumulated in a DMA buffer on the FPGA before being downloaded to the embedded processor. The FPGA may readily be re-programmed, for example allowing different readout strategies to be implemented for applications requiring the fastest possible data readout.

The new control electronics package is shown in Figure 2 alongside the existing control electronics

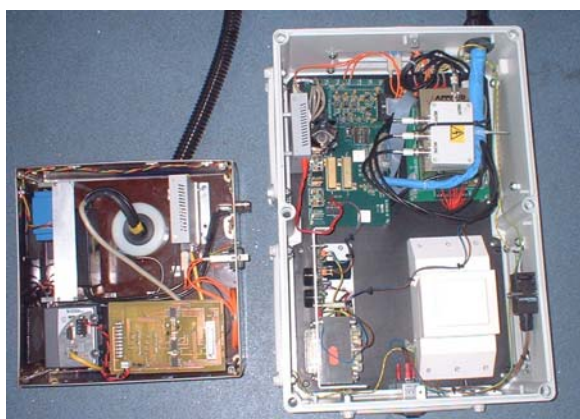


Figure 2 Control Electronics Package - New(left) and old (right)

The data readout speed has been increased by a factor of approximately 2 in the new interface. The new control electronics reads out a frame data from the 768 pixel detector in approximately 750 μ s compared with approximately 1.5ms for the existing electronics.

4. Formation of contacts on Diamond

The existing 768 pixel device in combination with a VG CLAM4 analyzer has been used in a number of applications which demonstrate the power and versatility of the in-situ XPS technique. The application presented here uses a laboratory X-ray source to study the formation of contacts between aluminum and diamond[5]. This application is believed to be the first time in-situ XPS has been demonstrated using a laboratory X-ray source rather than a synchrotron.

Synthetic diamond is becoming an increasingly important semiconductor material for devices such as high-temperature diodes and transistors as well as several detector applications. A key requirement for the use of a semiconducting material for devices is the ability to form ohmic contacts between the material and a metal layer.

Aluminum is the material of choice for diamond device applications. Aluminum forms a Schottky barrier on initial deposition on the diamond surface and may be annealed to form an ohmic contact but there is disagreement in the literature as to the temperature required to do this.

A polished/acid-cleaned B-doped (001) chemical-vapor deposited single crystal diamond was used as the substrate. Prior to metallization the surface was heated to 1100K to remove surface contaminants using an indirect heater. A shuttered Knudsen cell was used to deposit Aluminum on the diamond substrate at a rate of 0.2 nm min⁻¹.

A thin layer of aluminum was grown on the diamond surface, whilst using snapshot mode XPS to monitor the C1s core level peak during deposition. The attenuation of the C1s peak allowed the film thickness and growth mode to be estimated during deposition.

Following deposition, the temperature dependence of the AL/diamond interface was studied by

recording the C1s core peak during the application of a programmed temperature ramp, as shown in Figure 3.

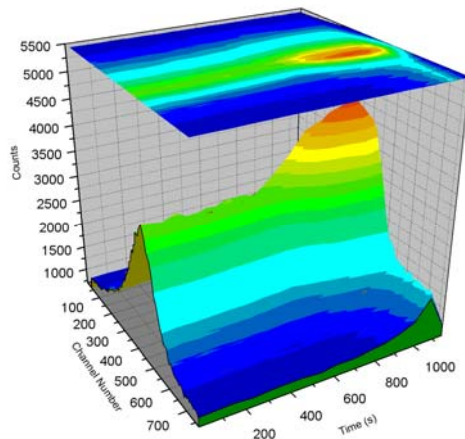


Figure 3 C1s peak during temperature programmed anneal

The C1s peak exhibits complex changes in amplitude, shape and position during the heating process. By fitting appropriate curves to the data, and plotting peak position and intensity, it is possible to examine the kinetics of the reaction as it takes place.

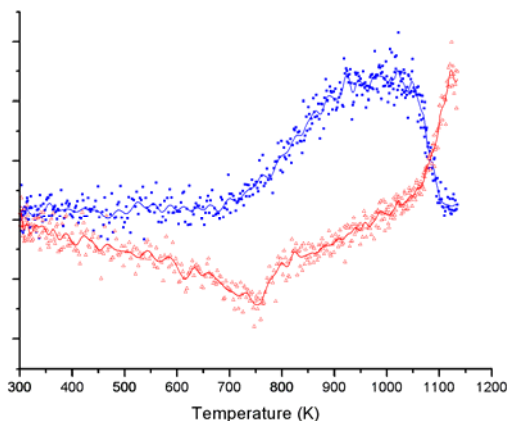


Figure 4 Amplitude (upper trace) and position (lower) of C1s photoelectron peak during anneal

Figure 4 shows the amplitude (upper trace) and peak position (lower trace) of the C1s core level peak during the annealing process, with the fitted data

plotted against temperature. The rise in peak intensity at approximately 755K corresponds to clustering of the Aluminum, revealing the underlying diamond surface. At the same time, there is an abrupt shift in the peak position, corresponding to the onset of the transition from Shottky to Ohmic behaviour of the contact. At approximately 1020K there is a second transition due to the formation of bulk carbide, indicated by the fall in intensity of the C1s peak.

5. Conclusions.

An extended detector array based on an existing design has been presented, together with a modified controller based on the National Instruments cRIO hardware. An application of the existing detector array has been presented, demonstrating how the improved detection capability permits in-situ XPS to be performed using a laboratory X-ray source.

6. Acknowledgements.

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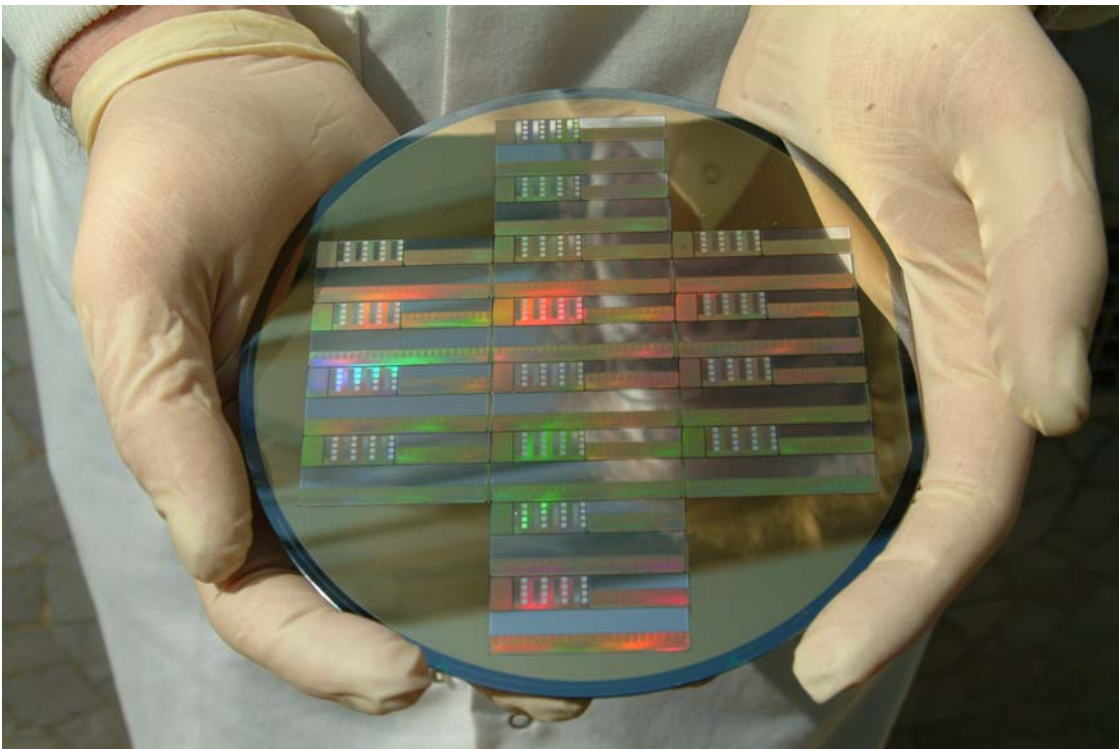
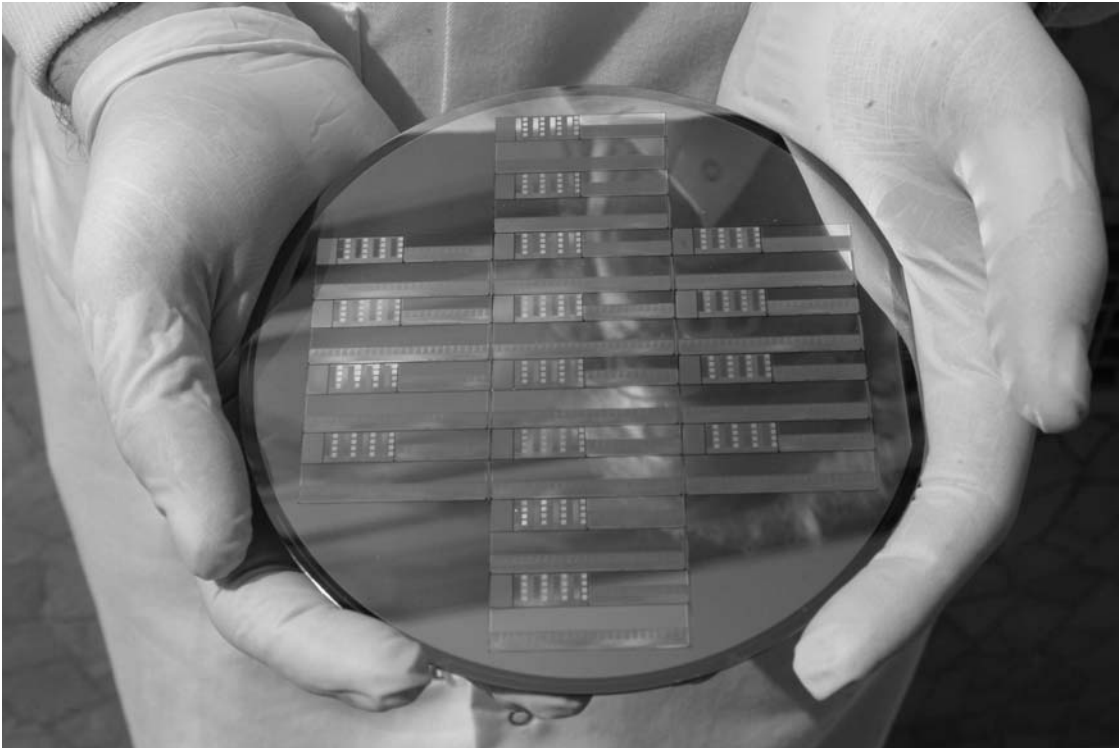


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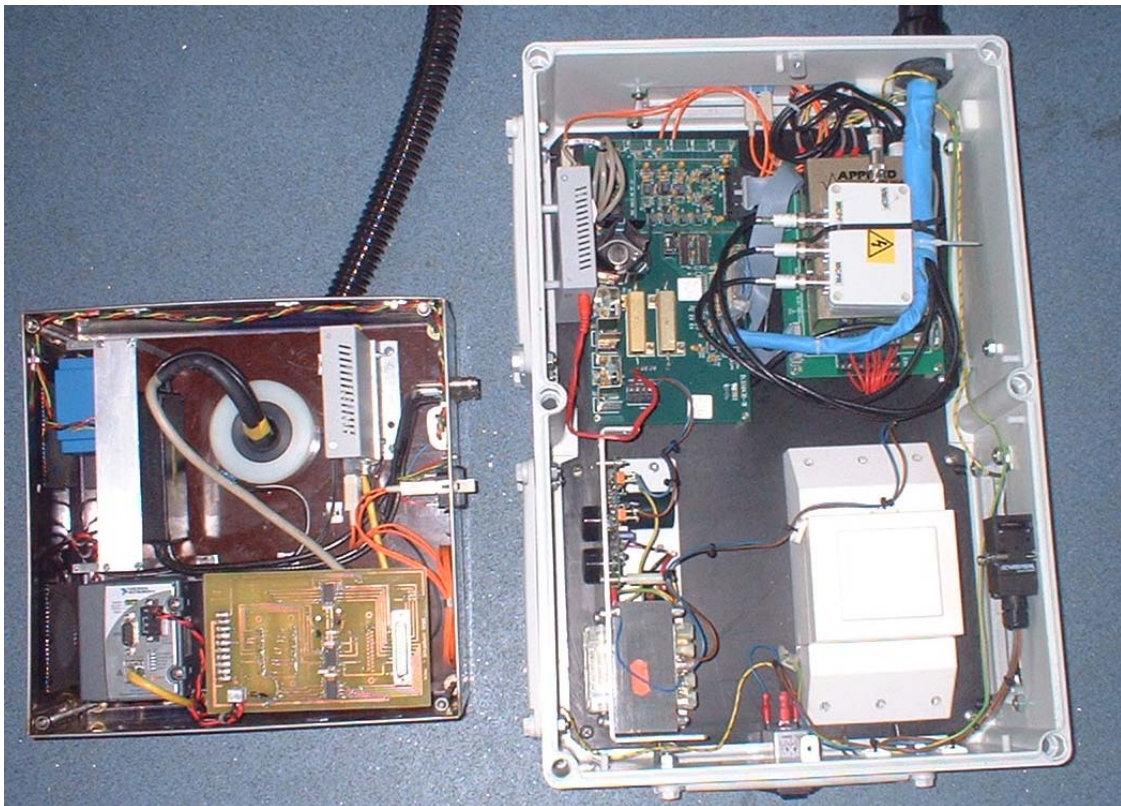
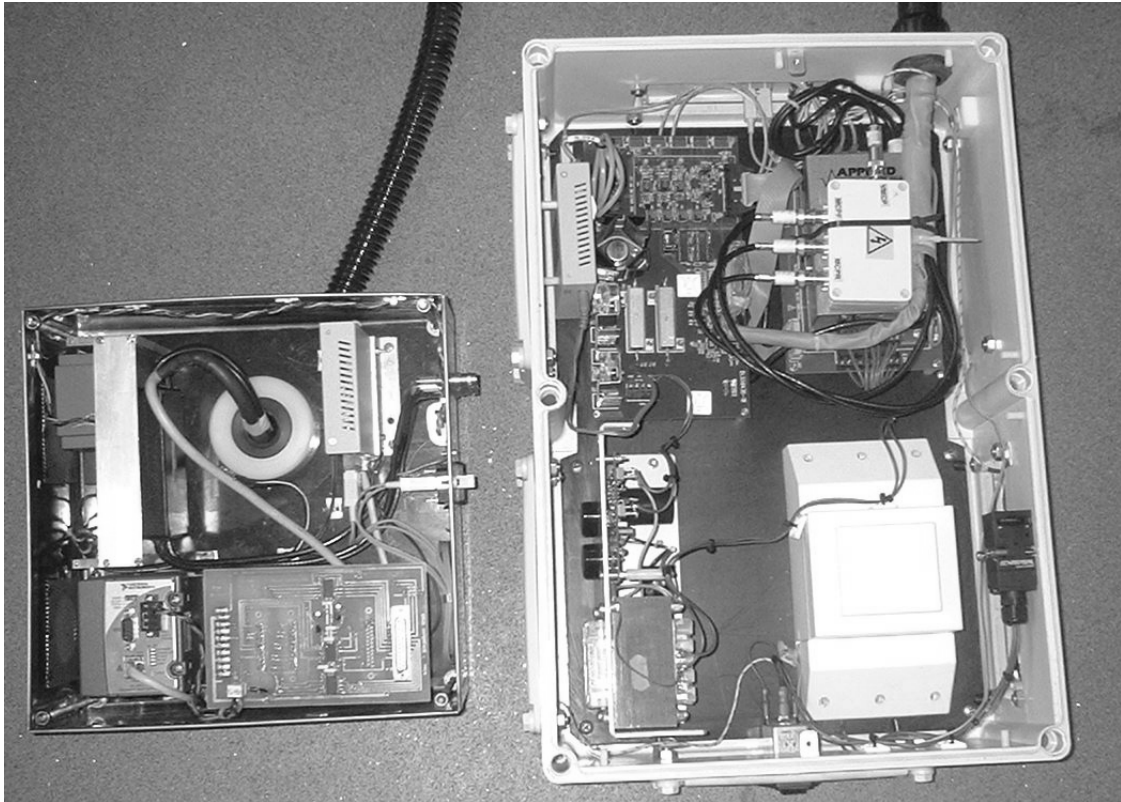


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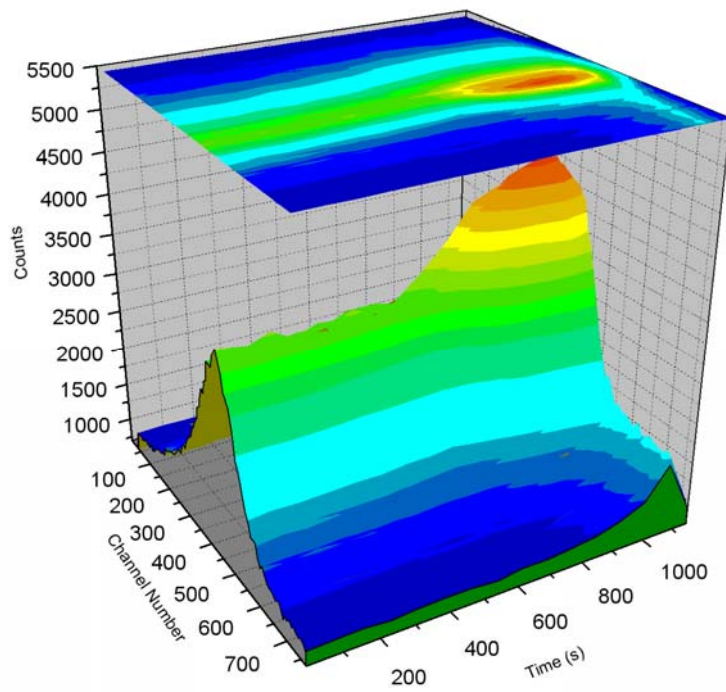
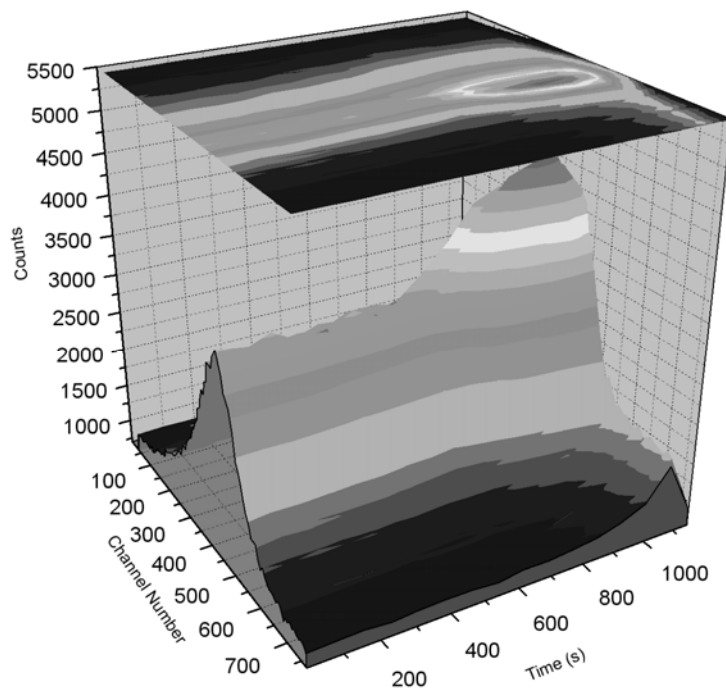


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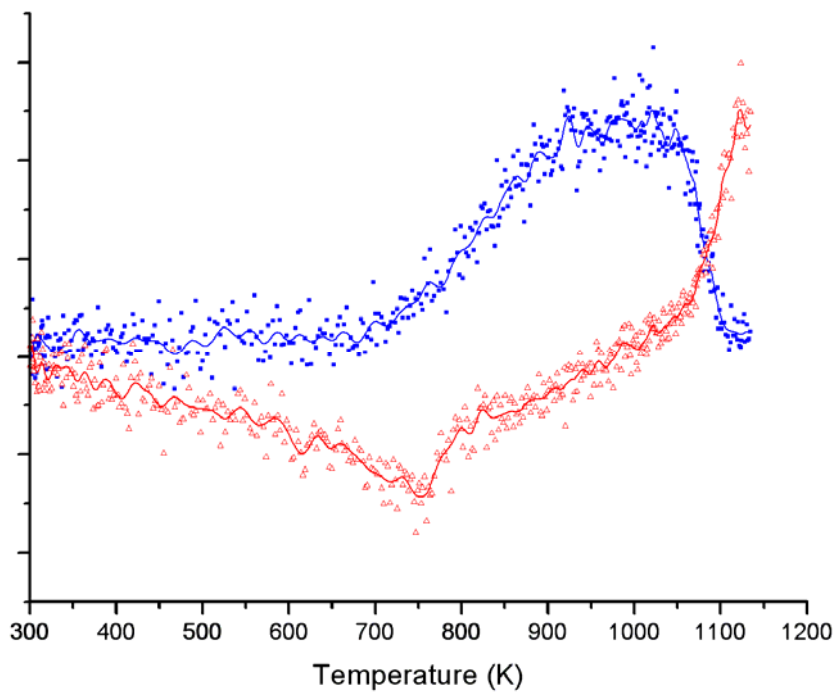
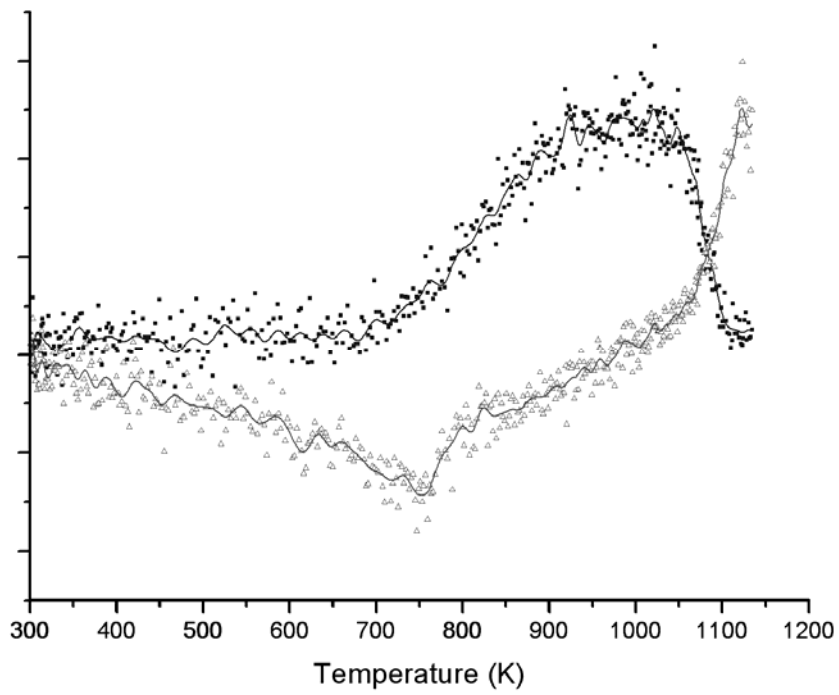


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