First Generation of Deep N-well CMOS MAPS with In-Pixel Sparsification for the ILC Vertex Detector

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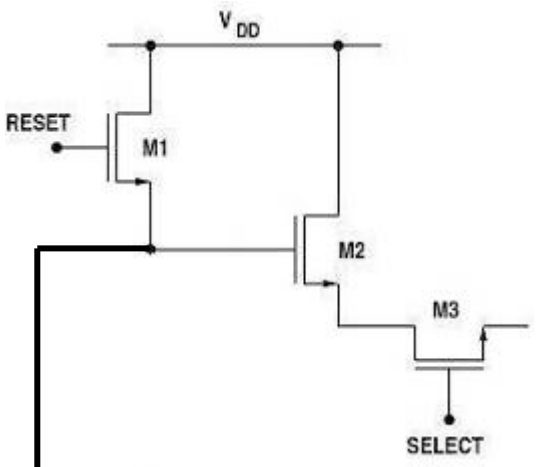
CMOS Monolithic Active Pixel Sensors

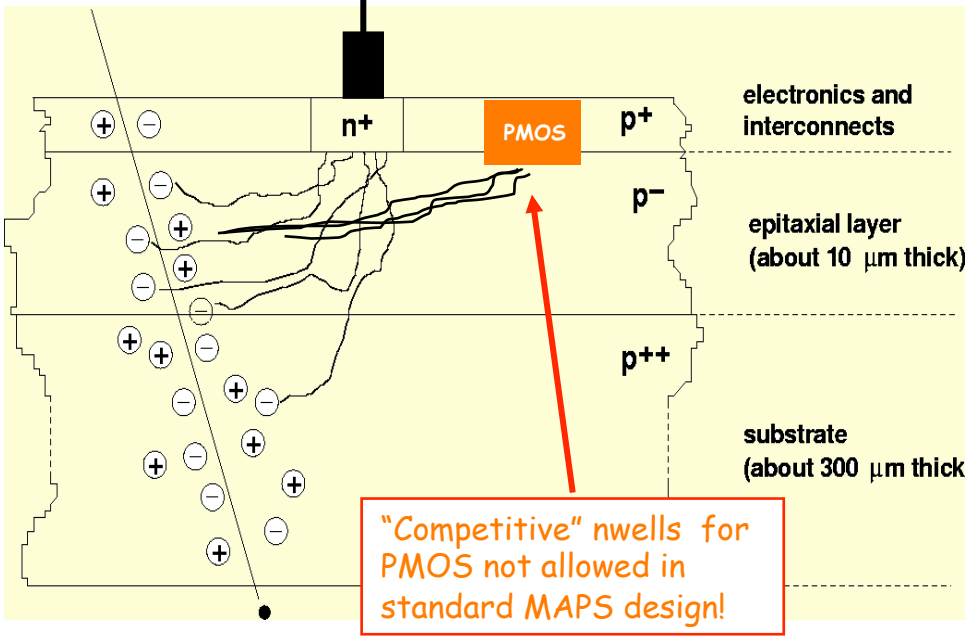
Several reasons make them very appealing as tracking devices :

- detector & readout on the same substrate
- wafer can be thinned down to few tens of μm
- radiation hardness (gate oxide ~nm thick)
- high functional density and versatility
- low power consumption and fabrication costs



Principle of operation

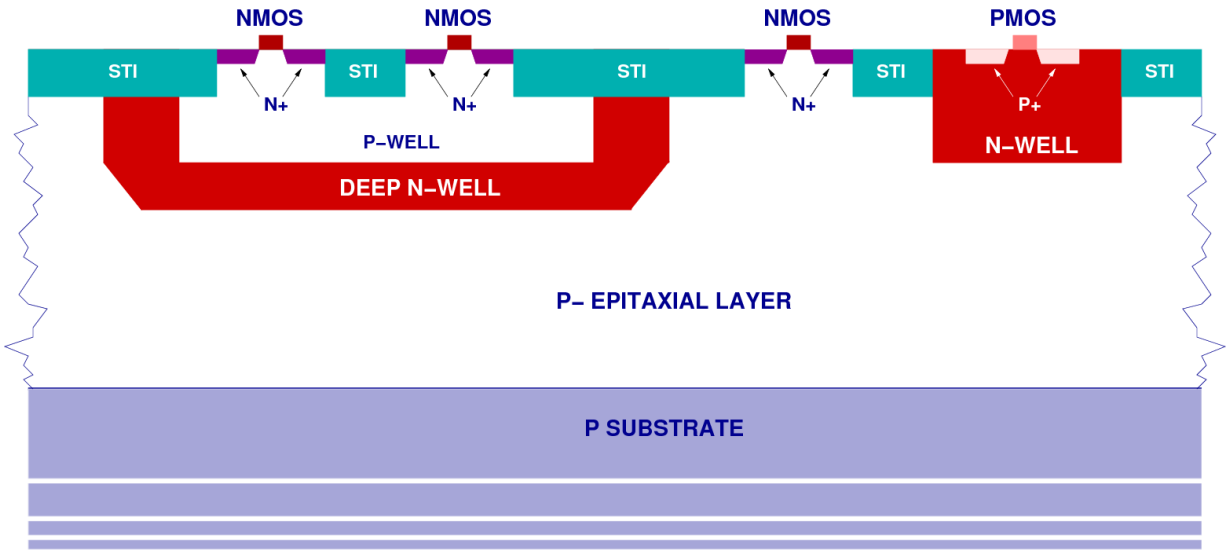
- The undepleted epitaxial layer acts as a potential well for electrons
- Signal (~1000 e-) collected through diffusion by the n-well contact
- Charge-to-voltage conversion provided by the sensor capacitance
  → small collecting electrode
- Simple in-pixel readout (additional nwells for PMOS not allowed in standard MAPS design!)
  → sequential readout



MAPS for vertex detectors in HEP experiments

- Tracking and vertexing systems in future high luminosity colliders (ILC, SLHC, Super B-Factory) will operate at high rate with low material budget to optimize position and momentum resolution
- Data sparsification could be an important asset at future particle physics experiments where detectors will have to manage a large data flow
- Modern VLSI CMOS processes (130 nm and below) could be exploited to increase the functionality in the elementary cell → sparsified readout of the pixel matrix
- The challenge is to implement a MAPS-based, rad-hard detector with similar functionalities as in hybrid pixels (sparsification, time stamping)

Triple-well CMOS processes



- In triple-well CMOS processes a deep N-well is used to shield N-channel devices from substrate noise in mixed-signal circuits
- DNW MAPS is based on the same working principle as standard MAPS

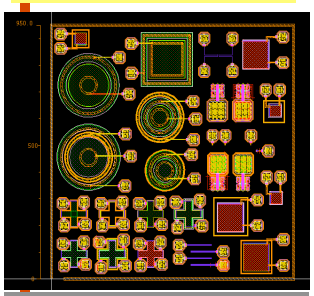
- Classical optimum signal processing chain for capacitive detector can be implemented at pixel level
- The collecting electrode (DNW) can be exploited to obtain higher single pixel collected charge
- A charge preamplifier is used for Q-V conversion → gain decoupled from electrode capacitance
- DNW may house NMOS transistors and using a large detector area, PMOS devices may be included in the front-end design → charge collection efficiency depends on the ratio between the DNW area and the area of all the N-wells (deep and standard)

DNW MAPS 130 nm STM process

SuperB

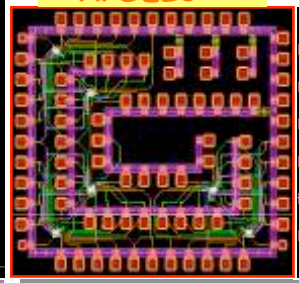
IC group contribution:
- Pavia (PV)-Bergamo (BG) analog front-end
- Pisa (PI)-PV-BG in pixel digital logic
- Bologna-PI digital readout architecture

TEST_STRUCT



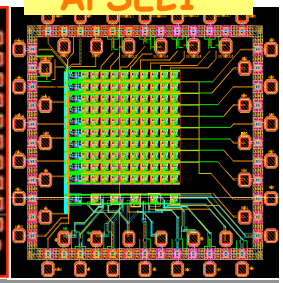
ST 130 Process characterization

APSEL0



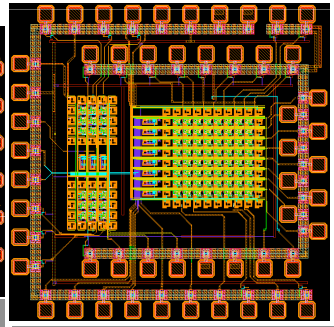
Preamplifier characteriz.

APSEL1



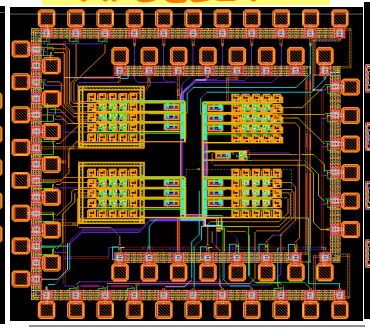
Improved F-E 8x8 Matrix

APSEL2M



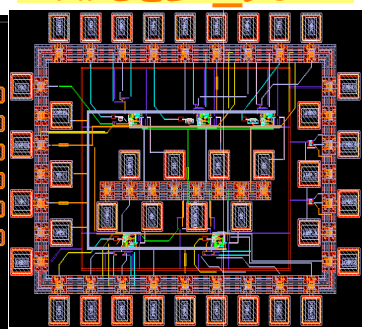
Cure thr disp. and induction

APSEL2T



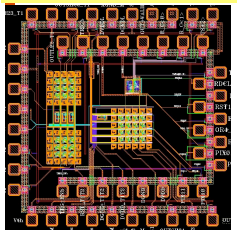
Accessible pixel Study pix resp.

APSEL2_90



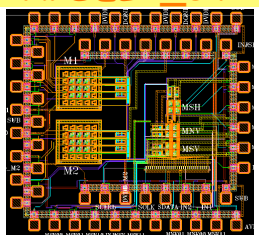
ST 90nm characterization

APSEL2D



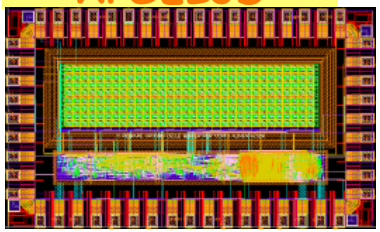
Test digital RO architecture

APSEL2_CT



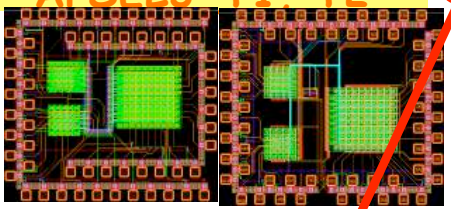
Test chips for shield, xtalk

APSEL3D



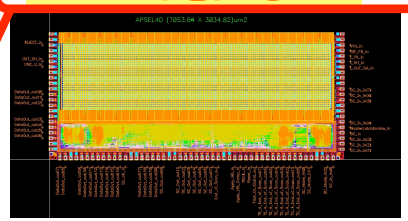
8x32 matrix. Shielded pixel - Data Driven sparsified readout

APSEL3_T1_T2



Test chips to optimize pixel and FE layout

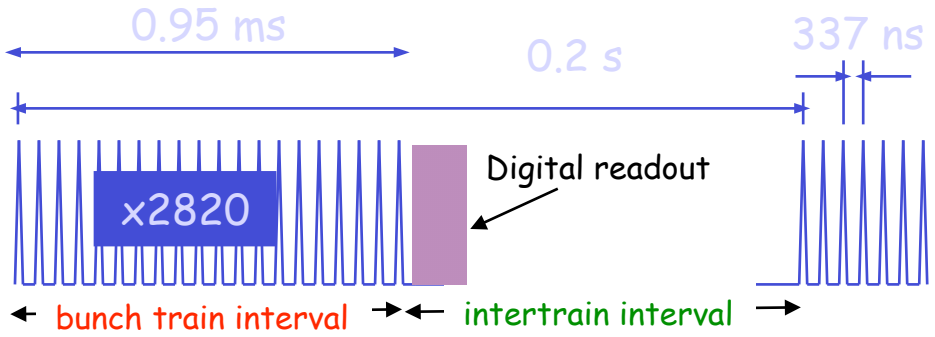
APSEL4D



32x128 matrix. Data Driven sparsified readout - Beam test Sep. 2008

See A. Gabrielli poster: "A 4096-pixel MAPS device with on-chip data sparsification", Poster session 4 - today

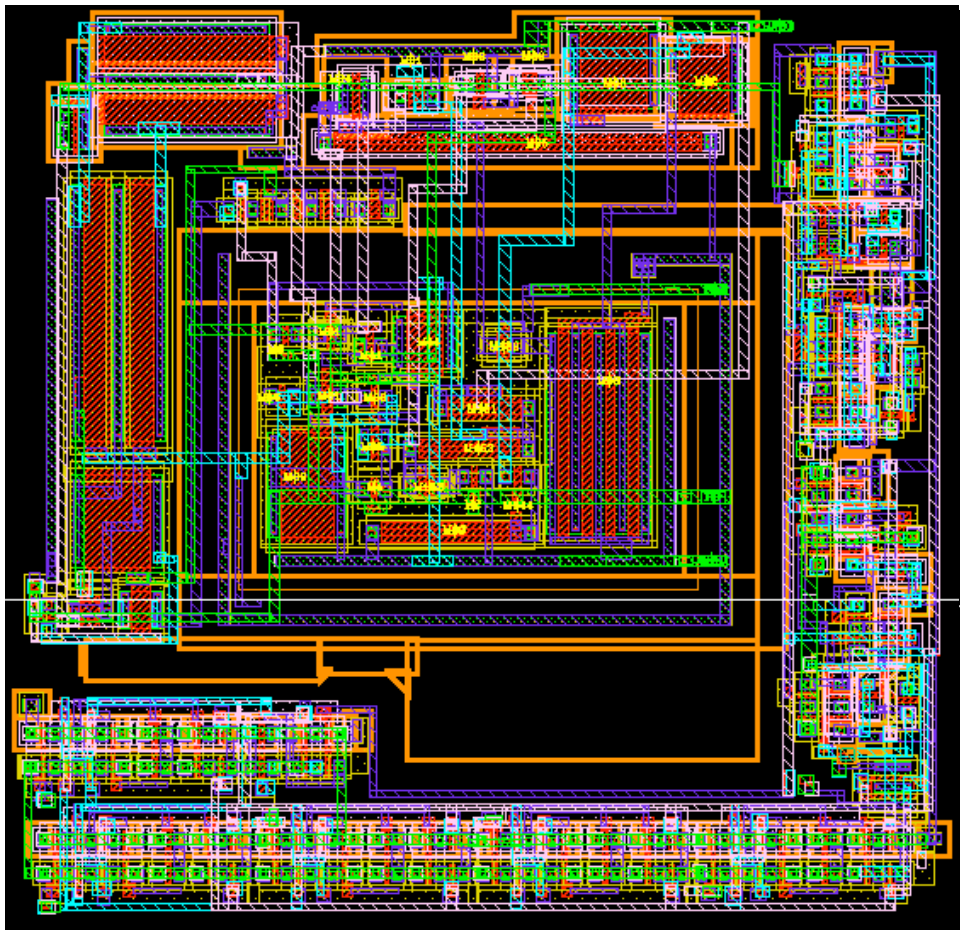
Design specifications for the ILC vertex detector



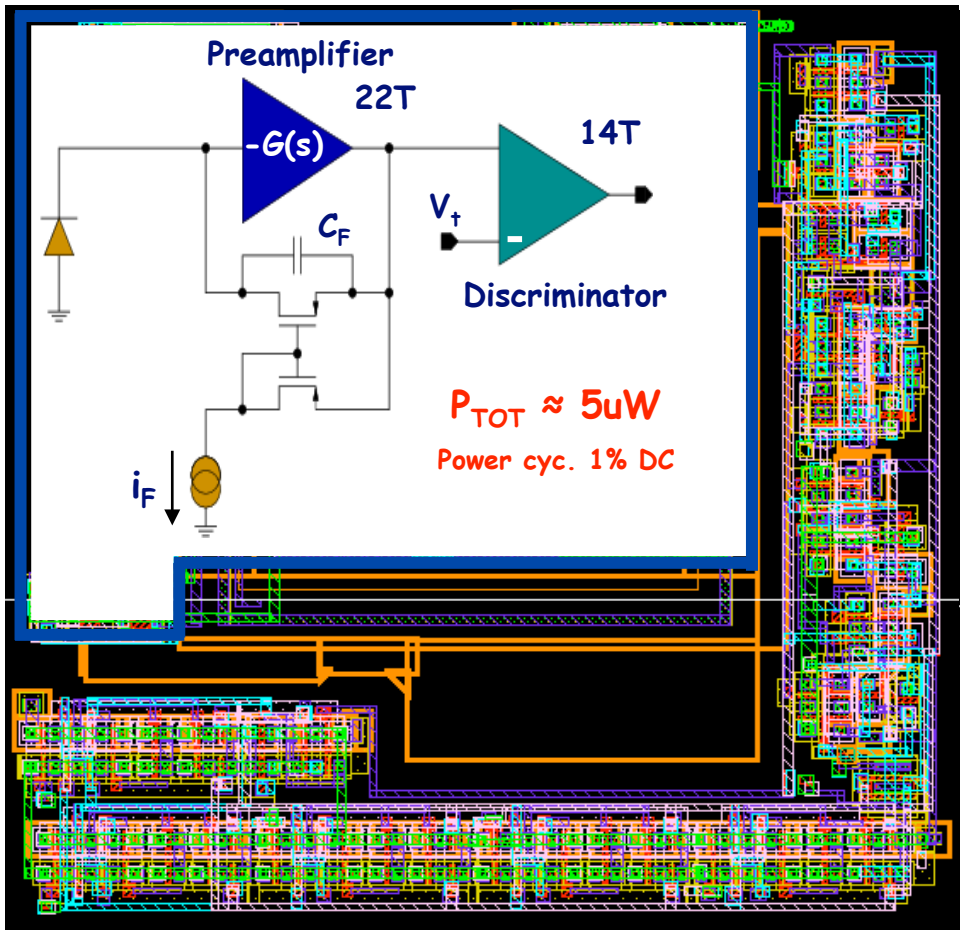
- The beam structure of ILC will feature 2820 crossings in a 1 ms bunch train, with a DC of 0.5%. Assuming:
- maximum hit occupancy 0.03 part./Xing/mm^2
- 3 pixels fire for every particle hitting → hit rate ≈ 250 hits/train/mm^2
- digital readout adopted: 5um resolution requires 17.3 um pixel pitch

- 15 um pixel pitch → $O_c \approx 0.056$ hits/train → the probability of a pixel being hit at least twice in a bunch train period ≈ 0.0016 → there is no need to include a pipeline for storing more than one hit per pixel (more than 99% of events recorded without ambiguity)
- MAPS sensor operation is tailored on the structure of ILC beam
  - Detection phase (corresponding to the bunch train interval)
  - Readout phase (corresponding to the intertrain interval)
- Data readout in the intertrain interval → system EMI insensitive
- Sparsified readout based on the token passing scheme. This architecture was first implemented in the VIP1 chip (3-D MIT LL technology) by the ILC pixel design group at Fermilab

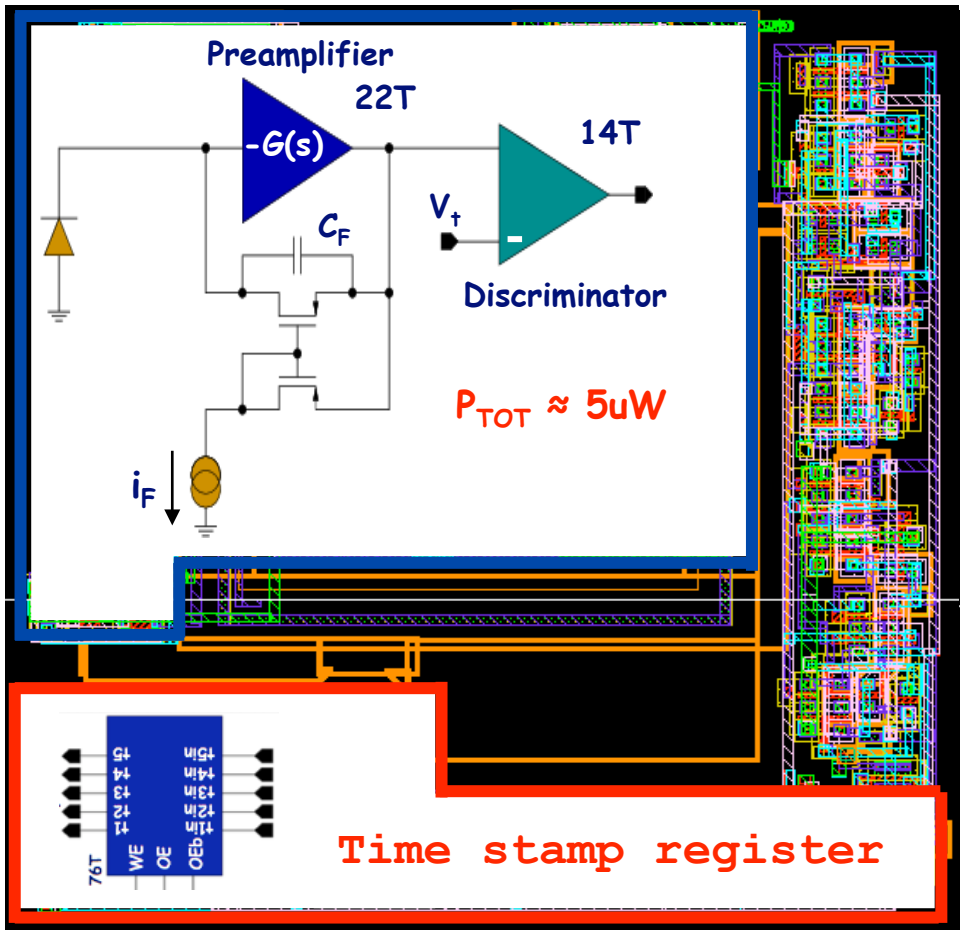
SDRO prototype elementary cell



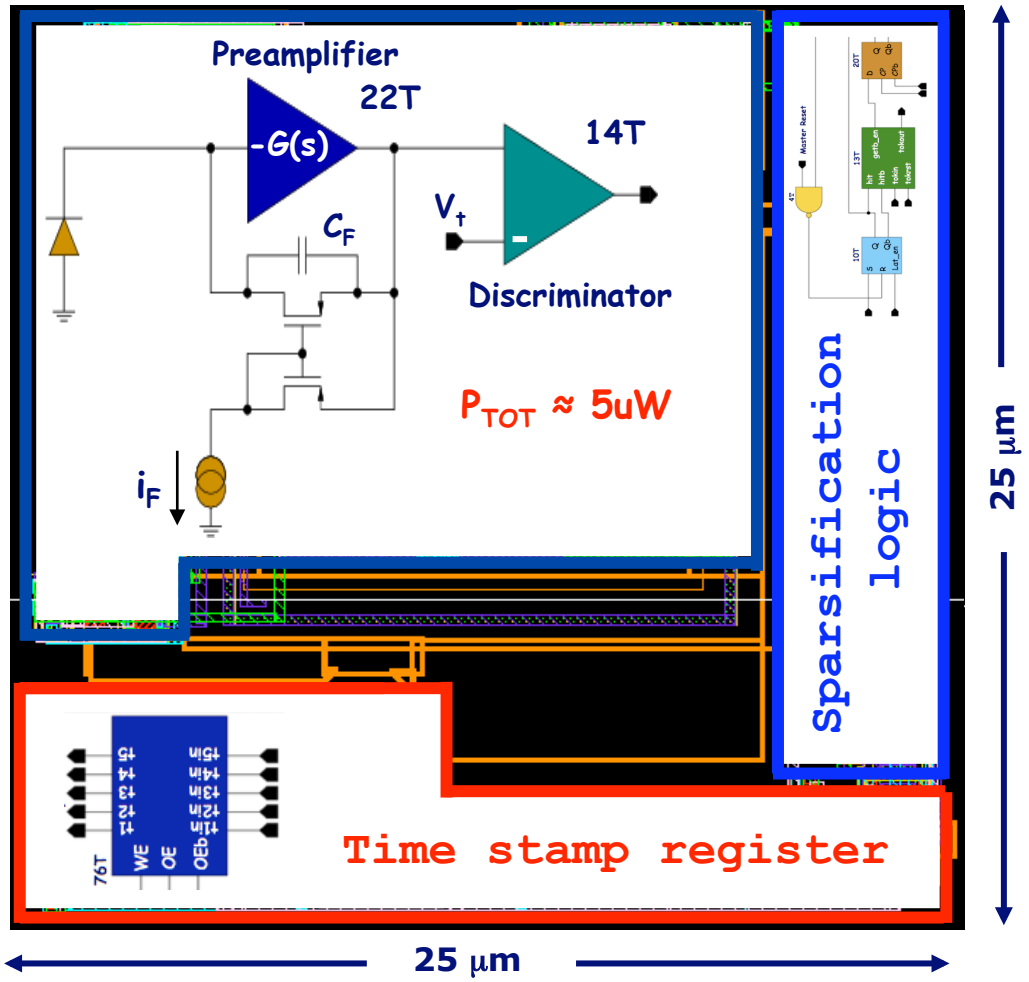
SDRO prototype elementary cell



SDRO prototype elementary cell



SDRO prototype elementary cell



analog front-end

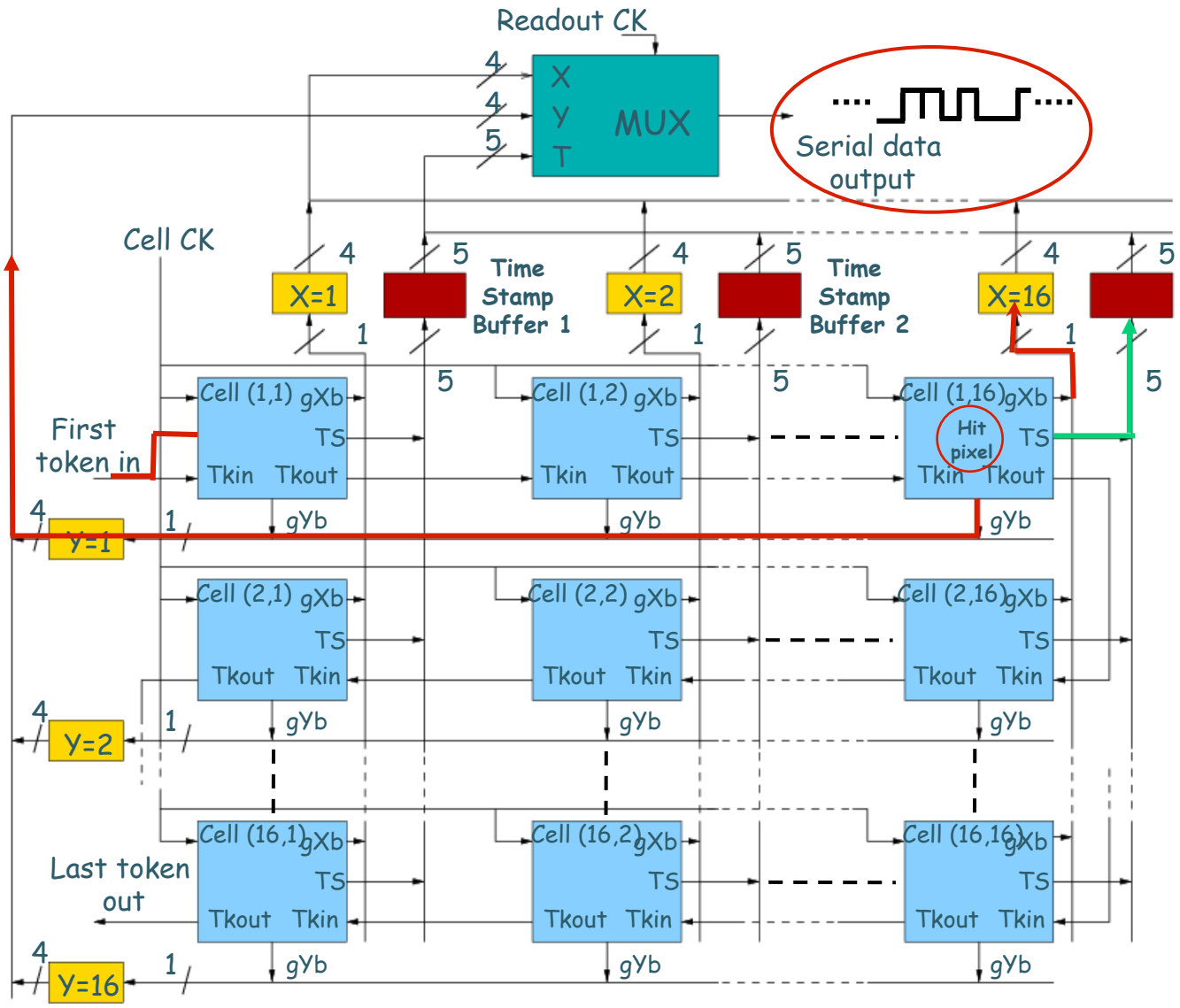
+

digital section

↓

164 transistors

Digital readout scheme



Readout phase:

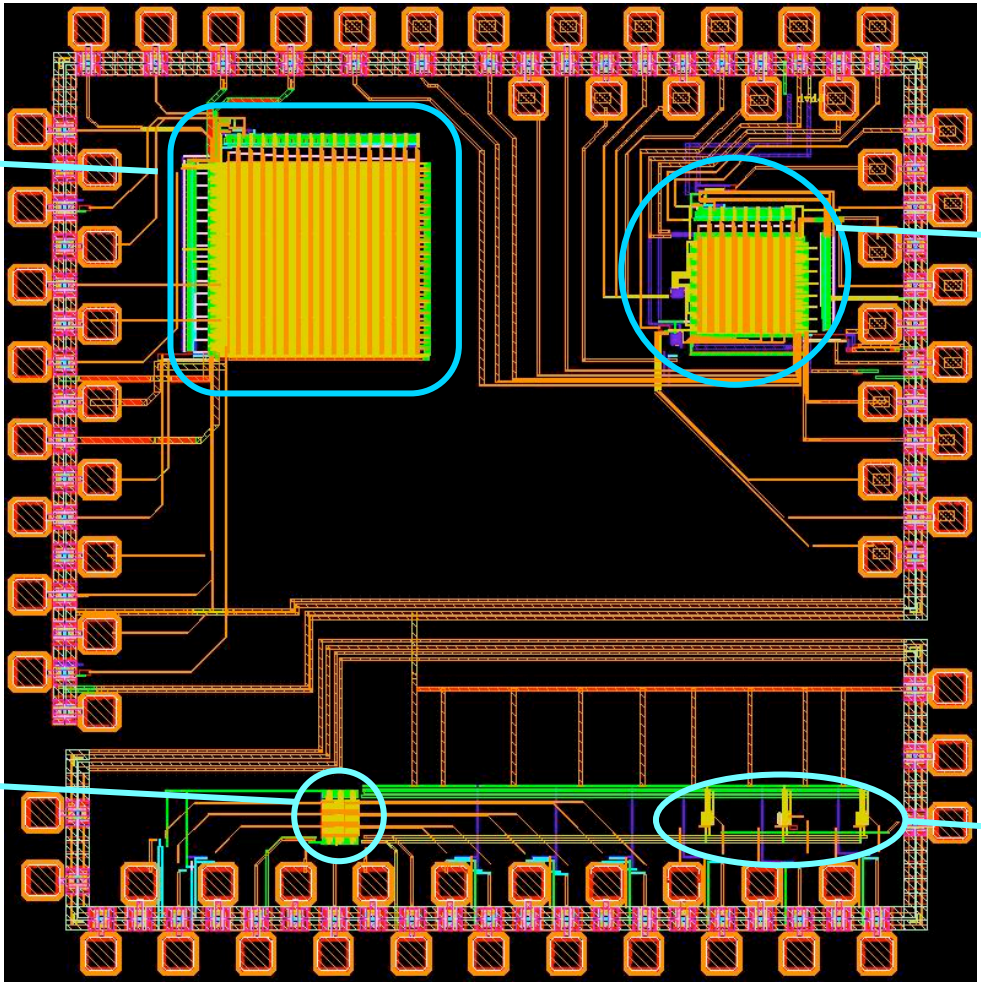
- token is sent
- token scans the matrix and
- gets caught by the first hit pixel
- the pixel points to the X and Y registers at the periphery and
- sends off the time stamp register content
- data are serialized and token scans ahead

The number of elements may be increased without changing the pixel logic (just larger X- and Y-registers and serializer will be required)

Prototype chip layout

- 130 nm CMOS HCMOS9GP by STMicroelectronics: epitaxial, triple-well process (available through CMP, Circuits Multi-Projets)

M1 – a 16x16 matrix chiefly conceived for the test of the digital sparsified readout

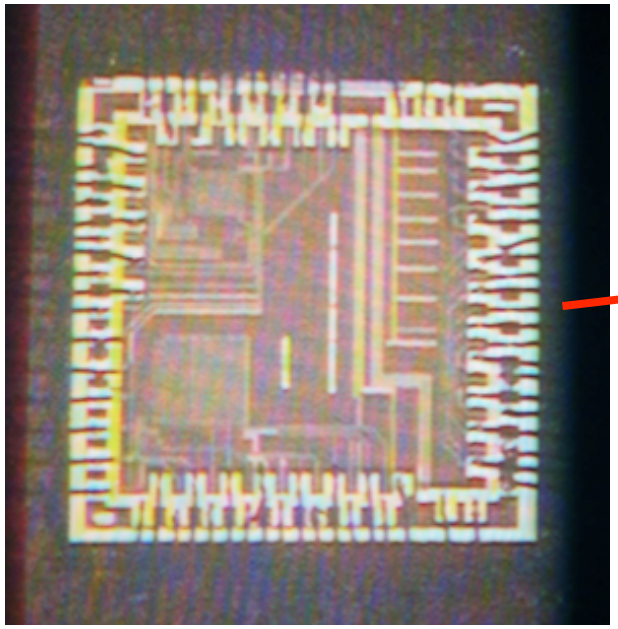


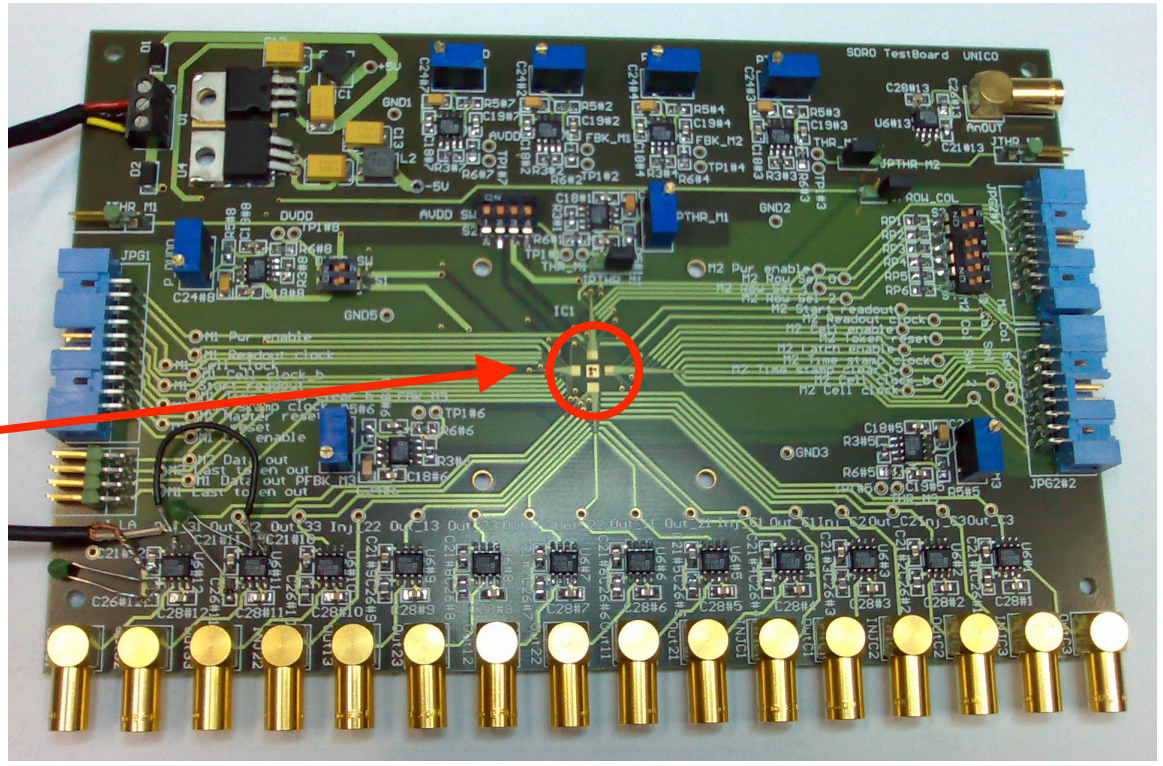
M2 - an 8x8 matrix with digital sparsified readout and selectable analog output

M3 - a 3x3 matrix with all the outputs of the charge preamplifier accessible at the same time

Single pixel test structures - 3 standalone readout channels with different C_D (detector simulating capacitance) with input pads for charge injection

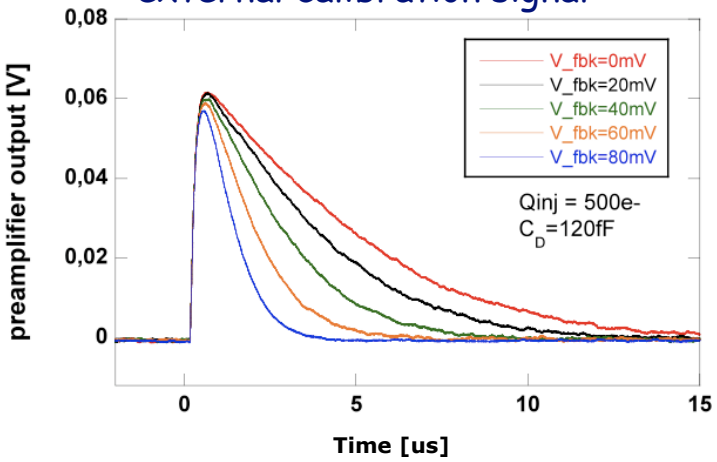
SDR0 chip and test board





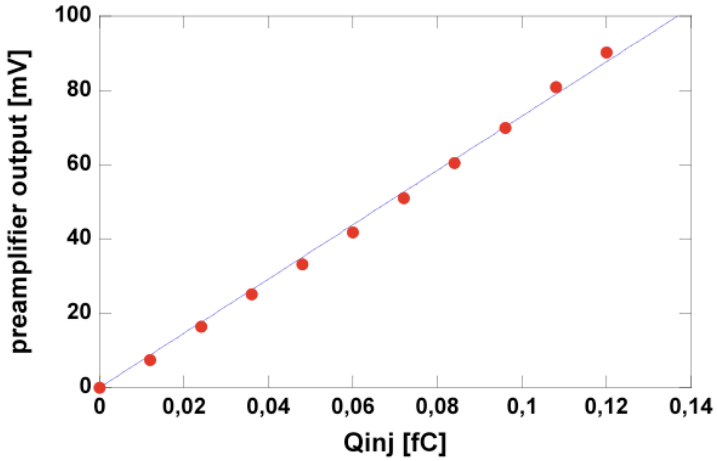
SDR0 experimental results

Preamplifier response to an external calibration signal

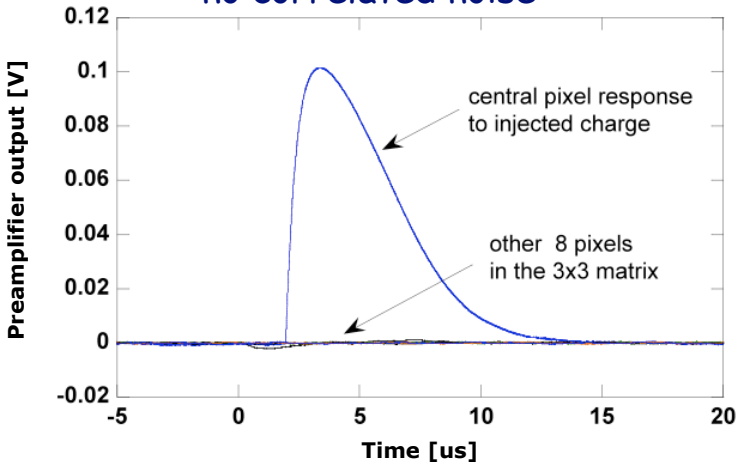


- Tests on the analog section with injection of external calibration signals and with an infrared laser scan (single channels, 3x3 pixel matrix)
- ENC ≈ 60 e- rms
  (PA input device: I_D = 1 uA, W/L= 22/0.25)
- Threshold dispersion ≈ 60 e-

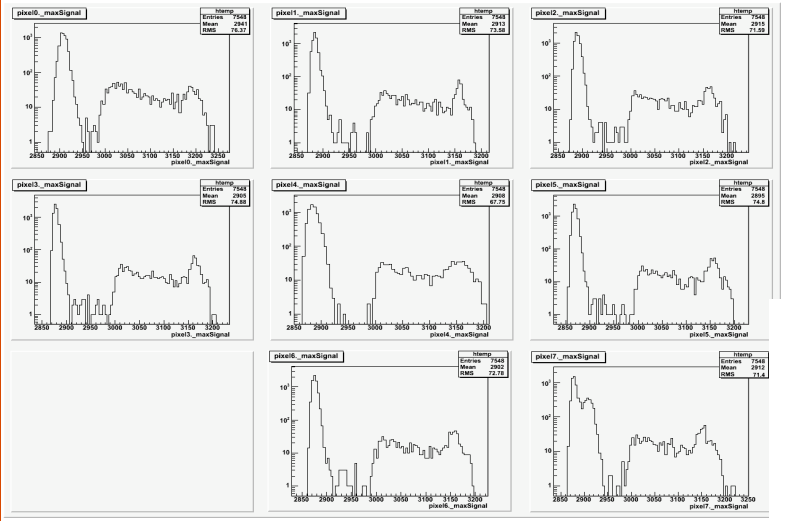
Pixel output signal vs injected charge



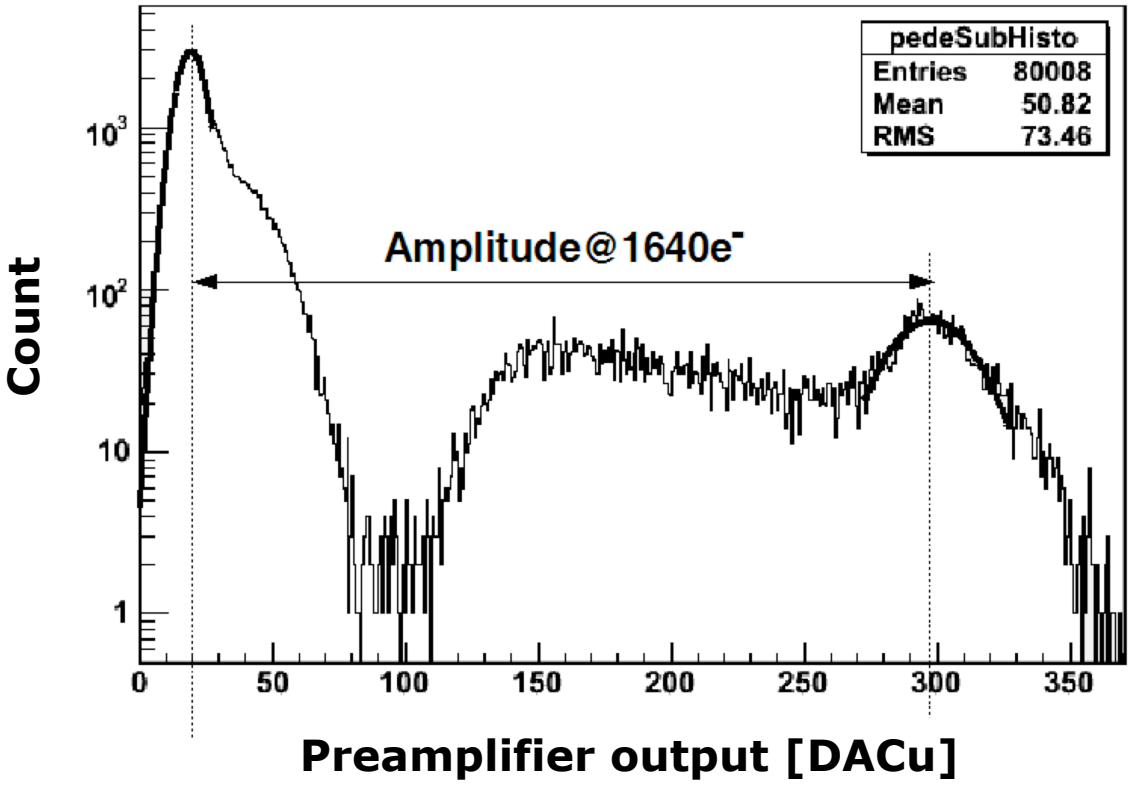
No crosstalk between pixels, no correlated noise



3x3 matrix response to ^{55}Fe source



- ^{55}Fe data confirm pixel gain calibration
- Cumulative spectrum relative to 8 of 9 pixels (M3)
- Charge sensitivity: 650mV/fC (mean value)



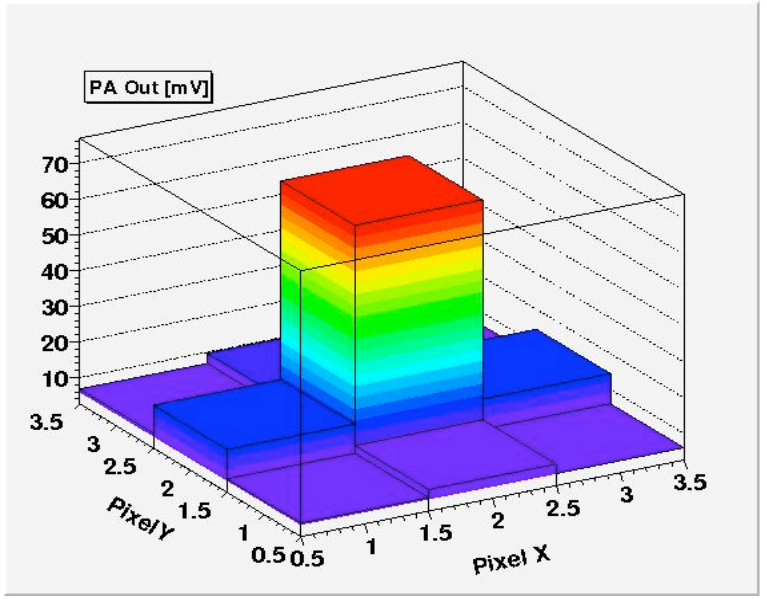
SDRO characterization with laser scan

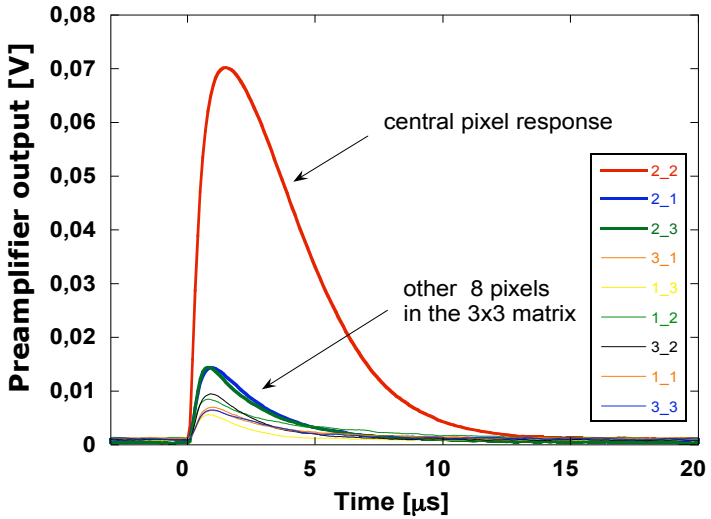
Focussed Laser on rear of sensor

- 1064nm wavelength
- Step by 5um in X and Y

Charge sharing among pixels

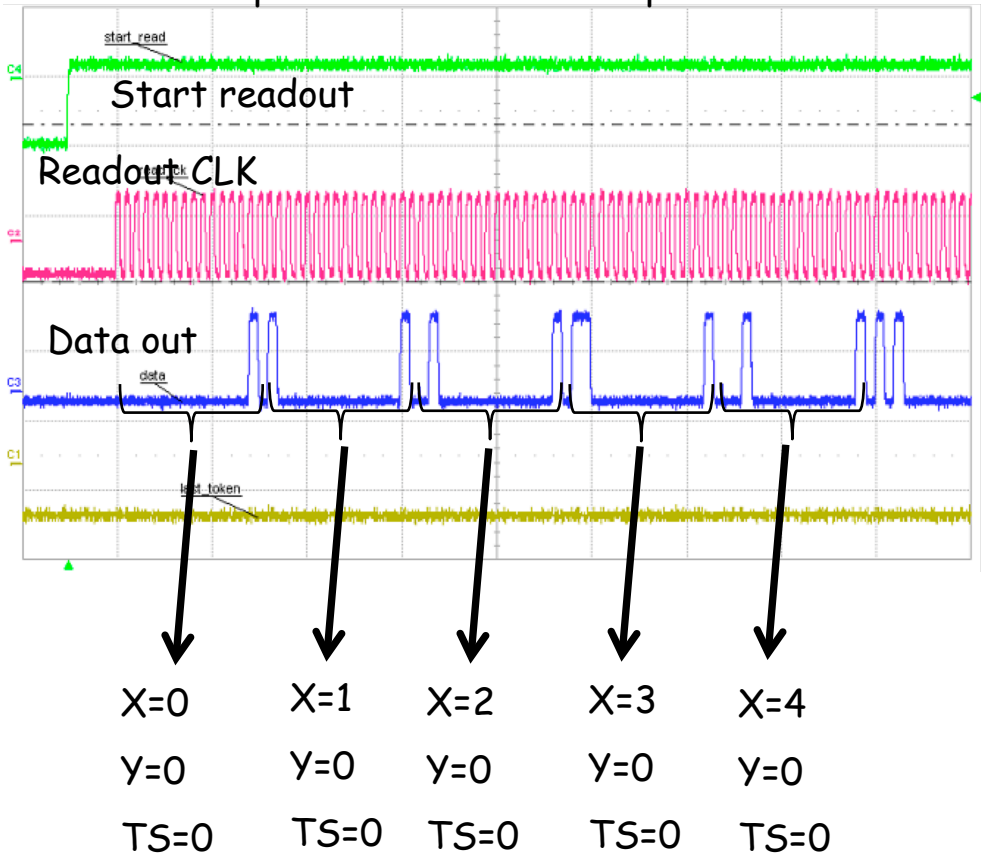
- 3x3 matrix response
- Laser focussed on the central pixel
- Limited charge spreading

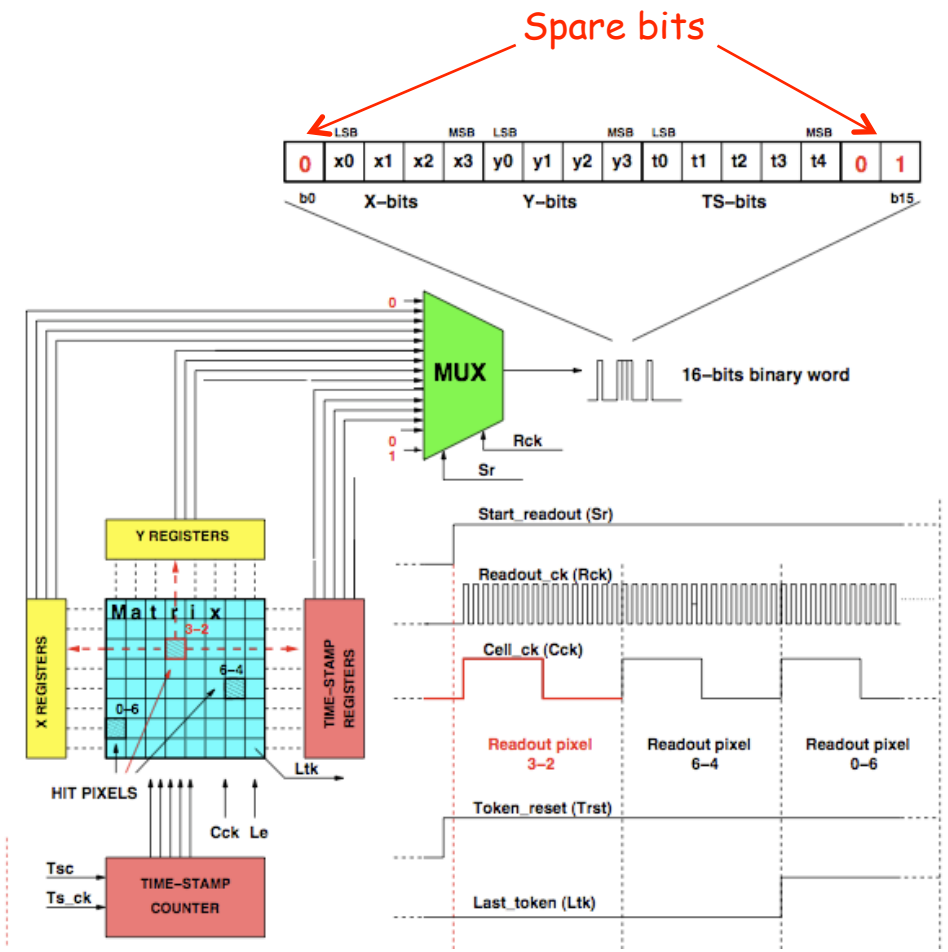




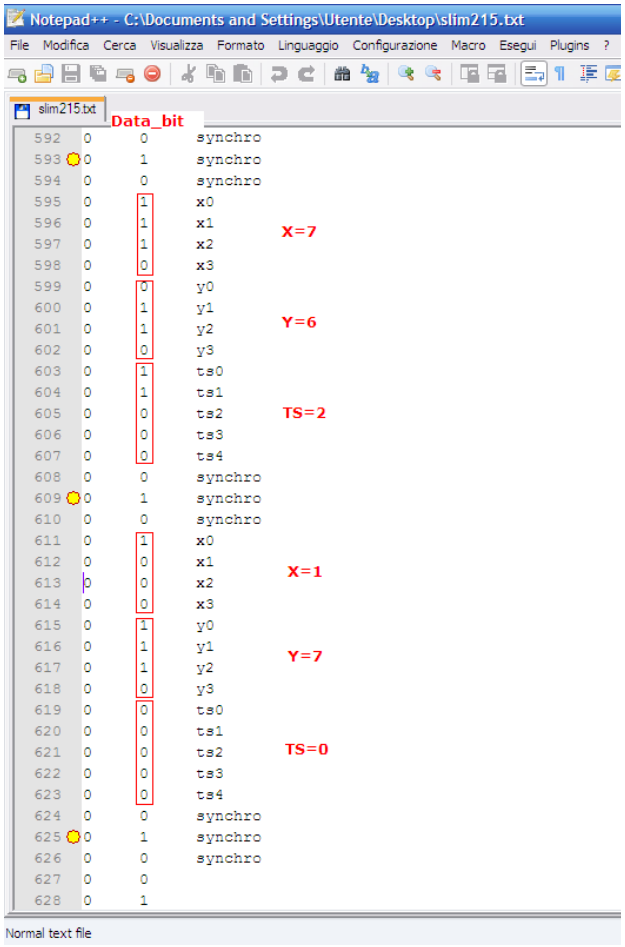
Digital readout test: pixel address

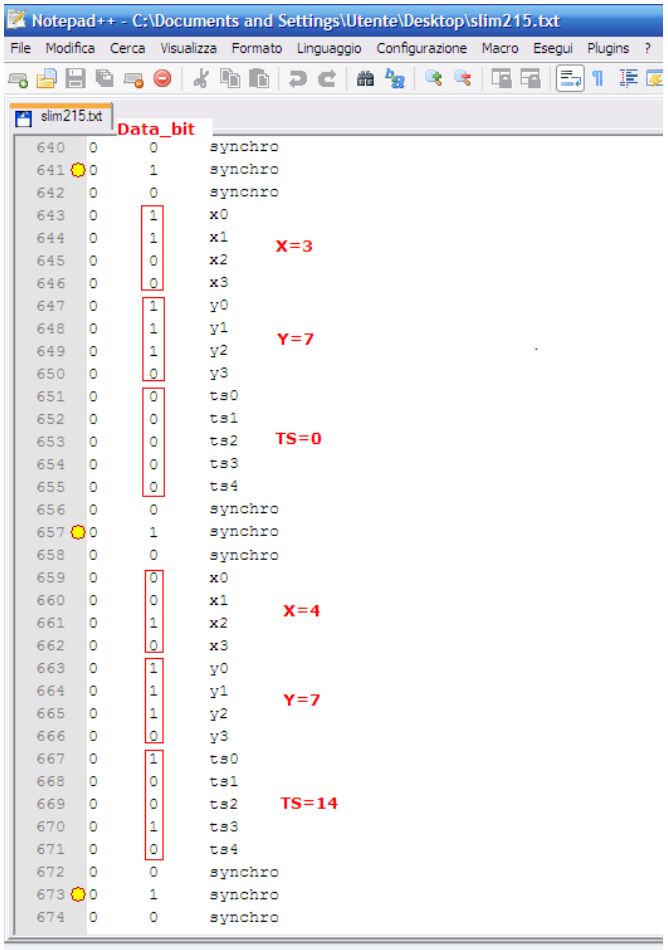
Vth < PA output DC level ➔ all the pixels are readout





Digital readout test: time stamp





Conclusions and future plans

- DNW MAPS structures have been fabricated in a 130 nm, triple well CMOS technology and successfully characterized
  - For the first time we have MAPS with in-pixel data sparsification and time-stamping with 30us precision
- Several issues have to be addressed to meet ILC specifications (pixel pitch, detection efficiency)
  - ILC VTX: if pixel pitch ≈ 15um then binary readout is ok!
  - Smart layout for standard N-wells is needed
- Tests of SDR0 structures with ^{90}Sr
- Explore more advanced technological solutions: Vertical Integration (3D)
- Vertical integration between two layers of 130nm CMOS chips: the first layer may include a MAPS device with analog readout and the second layer the digital readout circuits
- Design of a second prototype in a MPW run using Tezzaron/Chartered process is scheduled