Laser and Beta source characterization of 3D-DDTC detectors fabricated at FBK

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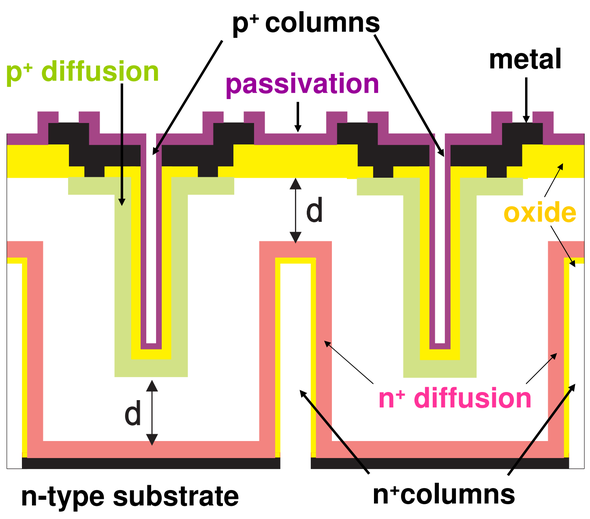
Abstract - We report on the functional characterization of the first batch of 3D Double-Sided Double Type Column (3D-DDTC) detectors fabricated at FBK, Trento. This detector concept represents an evolution of our previous 3D-STC detectors towards full 3D detectors, and is expected to achieve performance comparable to standard 3D detectors, but with a simpler fabrication process. Measurements were performed on detectors in the microstrip configuration coupled to the ATLAS ABCD3T binary readout. Spatially resolved signal efficiency tests made with a pulsed infrared laser setup and charge collection efficiency tests made with a Beta source setup are here reported.

Double-Side Double-Type Column 3D detectors - Process



Technology simplification of DDTC with respect to full 3D:

- Columns etched from both sides and not penetrating the entire substrate ⇨ No need for support wafer and wafer bonding technology
- Columns are not filled with Polysilicon ⇨ Chemical polishing avoided

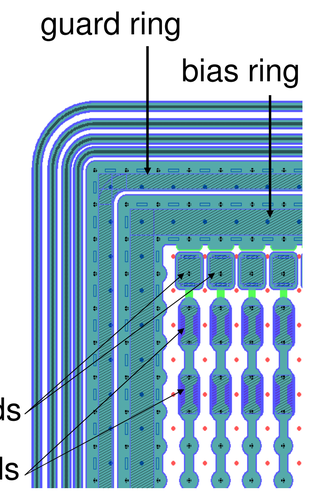
If distance *d* is kept small (tens of microns) performance comparable to standard full 3D are expected with a lower process complexity.

G.-F. Dalla Betta et al., "New development on 3D detectors at IRST ", 2007, IEEE NSS, Conference Record, Paper N44-2"

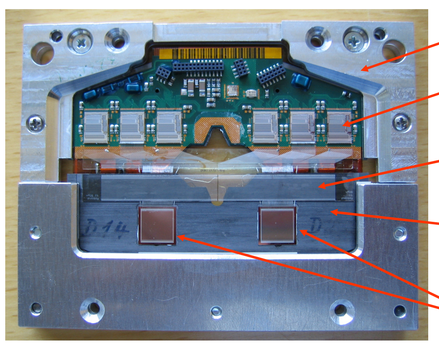
Microstrip detectors features

Substrate thickness	300	µm
Junction column depth	190	µm
Back column depth	170	µm
Lateral depletion	0.5	V
Full depletion	3	V
Back plane capacitance	20	fF/col
Leakage current at FD	0.1	pA/col

102 x 102 columns matrix
80µm inter-intra columns pitch
Area: 1cm²



The module

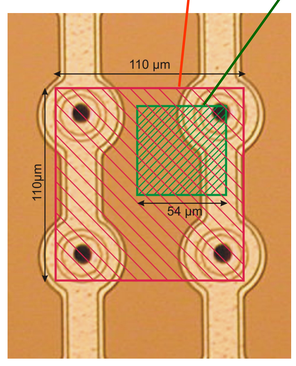


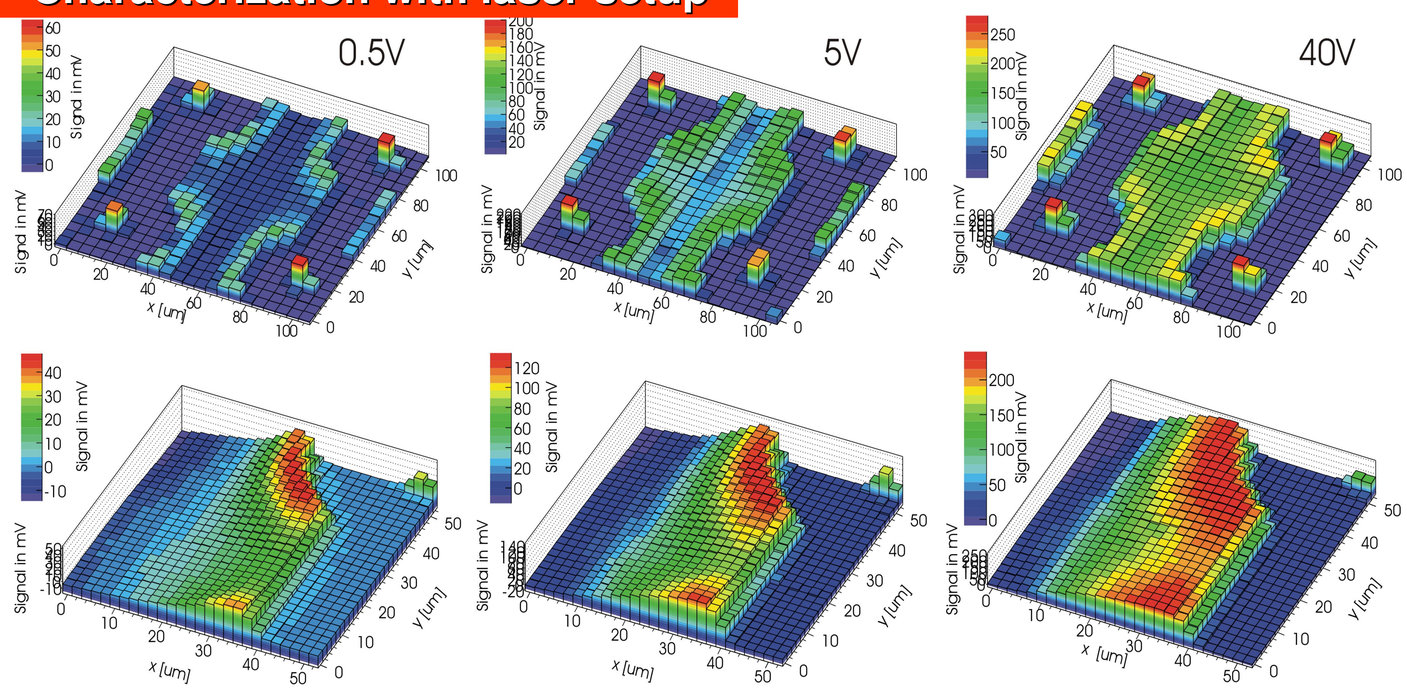
Fast binary readout 20ns shaping time

Characterization with laser setup

Coarse scan 5µm step — Signal from both strips

Fine scan 2µm step — Signal from one strip





Even at very low voltage the sensors collect charge from the region around columns.

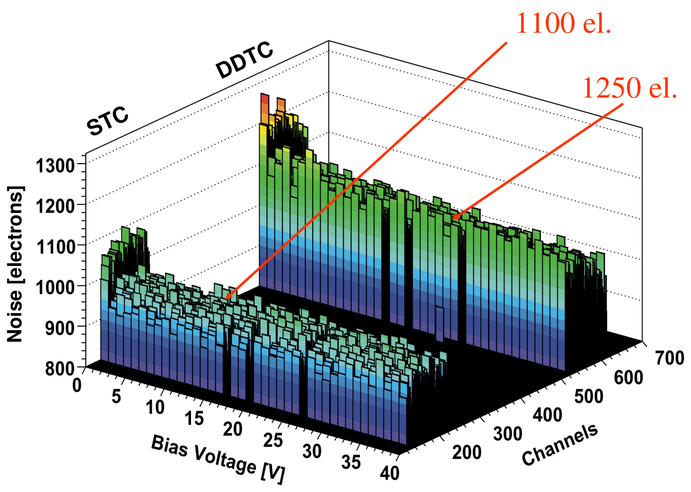
At 5V the collected charge is not uniform among the active area. Ballistic deficit is still an issue due to non-optimal column depth and fast readout.

At 40V the signal is almost uniform among the cell.

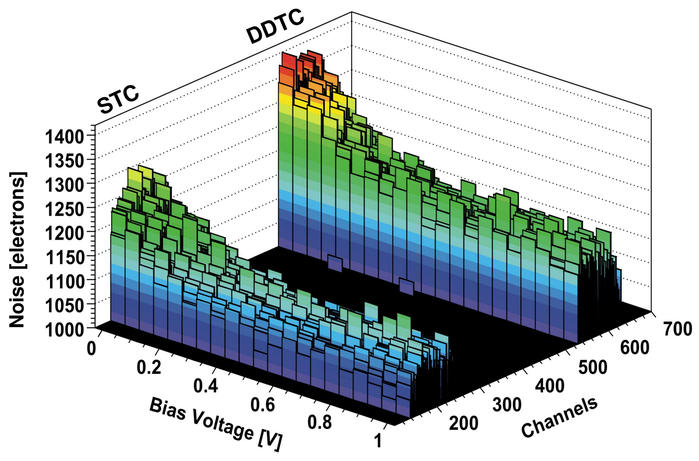
System Setup:
- 980nm infrared laser pulse
- Spot size focused with microscope down to 2µm on detector surface

Noise Scan

DDTC exhibits higher noise respect to STC due to a higher back capacitance. Detectors work properly up to 40V.



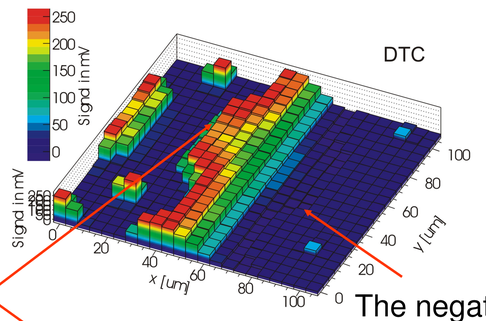
Scan made from 0 to 1V confirms that the lateral depletion value is in agreement with results obtained from CV measurements.



DDTC vs STC: induced signal

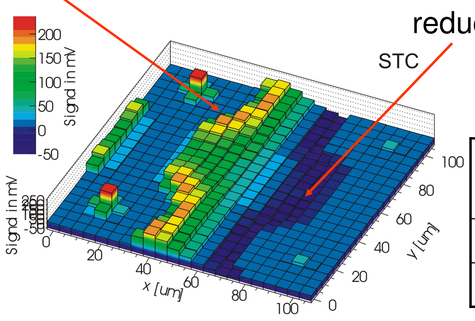
Plots refer to signal induced on left strip at a bias of 10V.

STC and DDTC mounted on the same module



DDTC collects more charge than STC.

The negative signal induced on the left strip is highly reduced on DDTC.

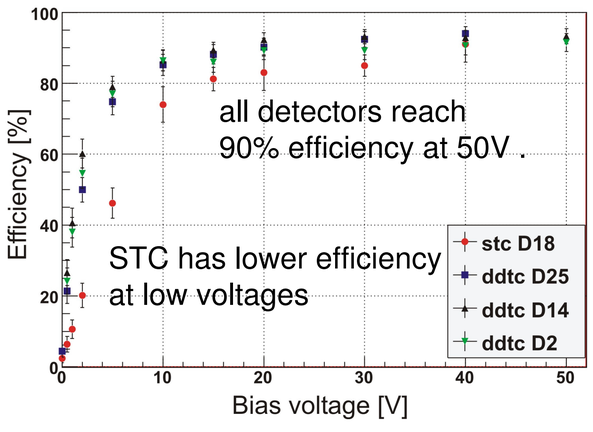


	Maximum signal
DDTC	250 mV
STC	180 mV

	Negative signal
DDTC	-5 mV
STC	-50 mV

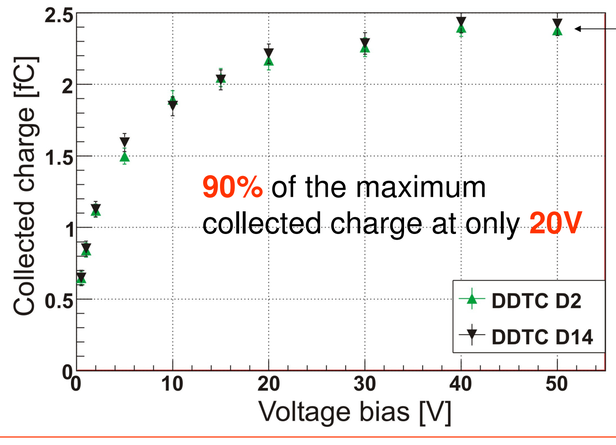
Efficiency at 1 fC

System setup:
2.4MBq Sr^{90} β source.
Events triggered by two scintillators in coincidence.
ATLAS fast binary readout system as for the laser setup.



Charge Collection Efficiency

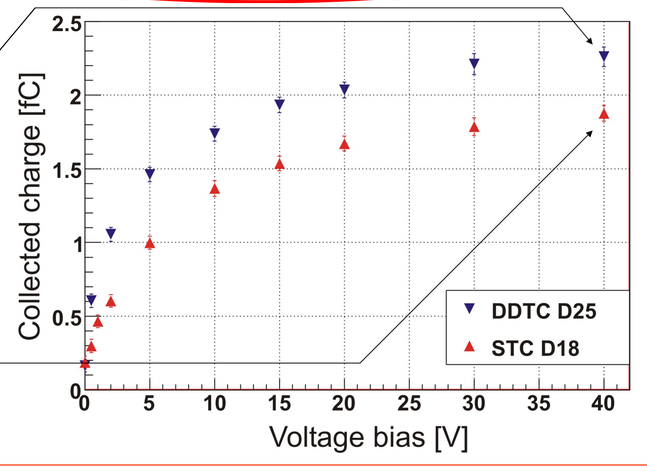
New DDTC technology exhibits a net performance improvement respect to STC



Collected charge at 40V

DDTC: 2.4 fC

STC: 1.8 fC



8th International Conference on Position Sensitive Detectors, 1st - 5th September 2008, Glasgow (Scotland)