HEXITEC
HIGH ENERGY X-RAY IMAGING TECHNOLOGY

PSD8
8TH INTERNATIONAL CONFERENCE ON POSITION SENSITIVE DETECTORS

HEXITEC ASIC – A Pixellated Readout Chip for CZT Detectors

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Science and Technology Facilities Council
Rutherford Appleton Laboratory

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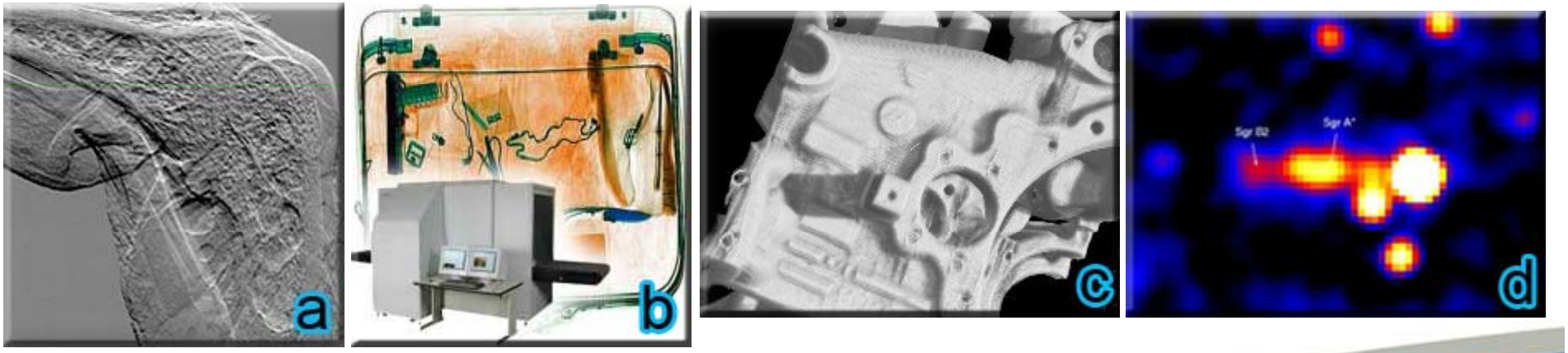
Introduction

- HEXITEC is a collaborative project between the Universities of Manchester, Durham, Surrey, Birkbeck and The Science and Technology Facilities Council (STFC)
- Develop a new range of detectors such as CdZnTe for high energy X-ray imaging for such applications shown below
- The Project has been funded by EPSRC on behalf of RCUK under the Basic Technology Programme

Medical Security Tomography Space



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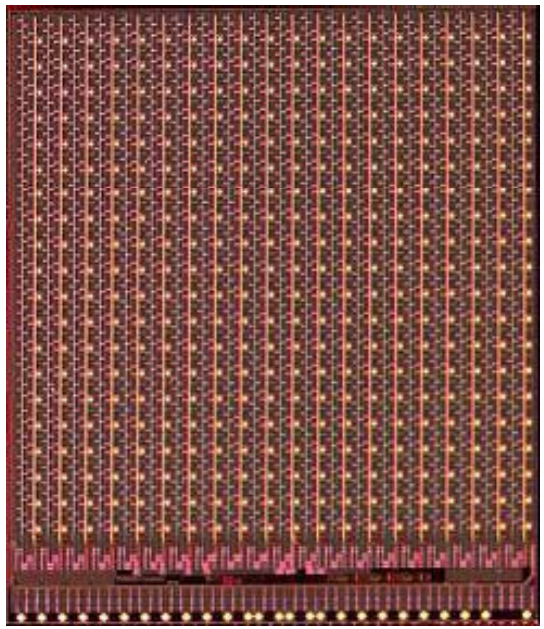
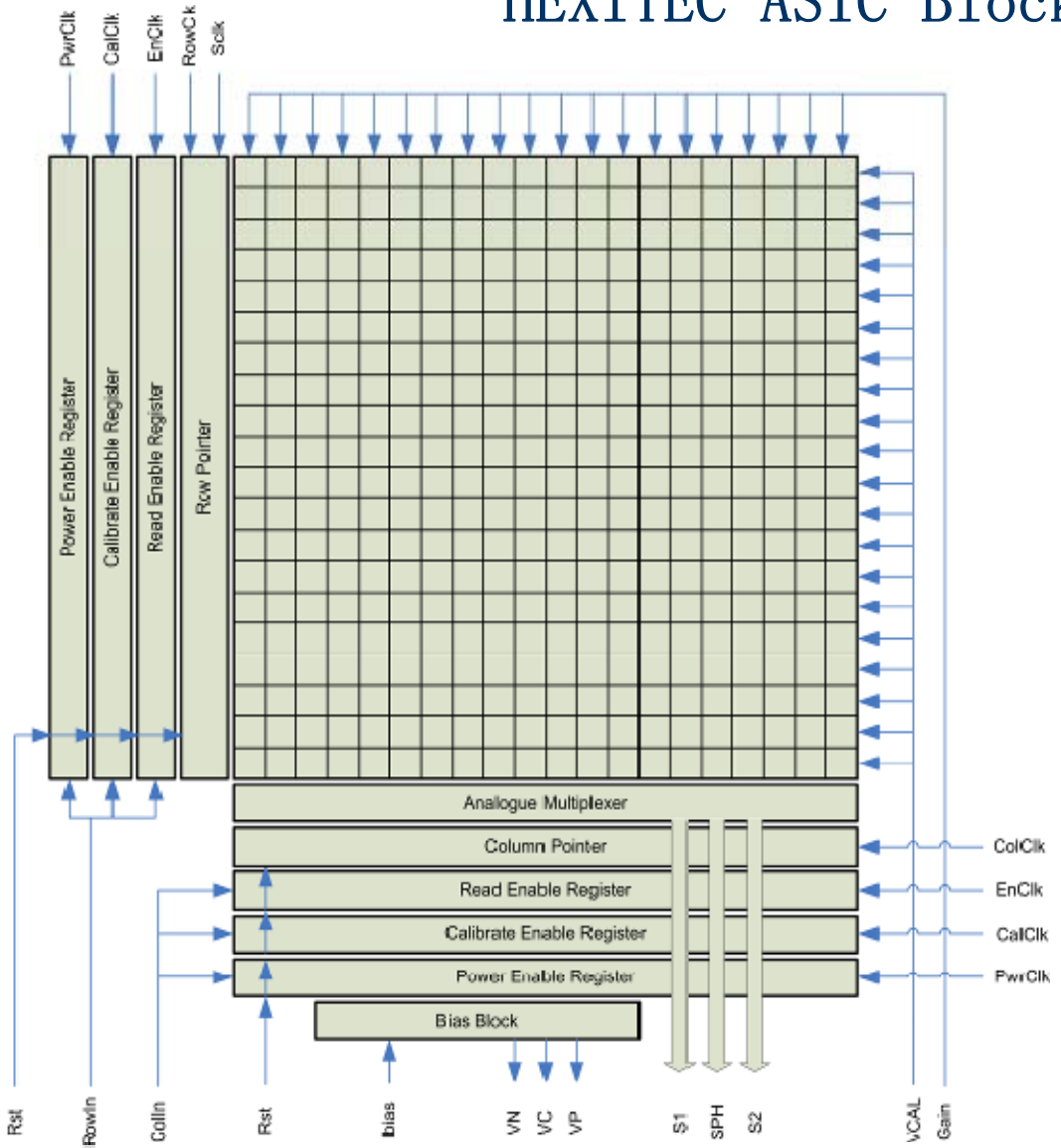
HEXITEC 20x20 ASIC



HEXITEC 20x20 ASIC

- An ASIC has been developed to read out the new pixellated detectors
- Initially a 20x20 pixel readout chip has been designed and manufactured
- Ultimately a 80x80 pixel ASIC is required
- This talk concerns the design of the 20x20 pixel version

HEXITEC ASIC Block Diagram



- 20x20 pixel array
- 250µm x 250µm pixels
- Gold stud bonded to CZT
- Programmable regions of interest
- Rolling shutter type readout
- Analogue output
- Selectable range 150keV / 1500keV (40 000 electrons / 400 000 electrons)
- Noise 200eV FWHM (20 electrons rms)

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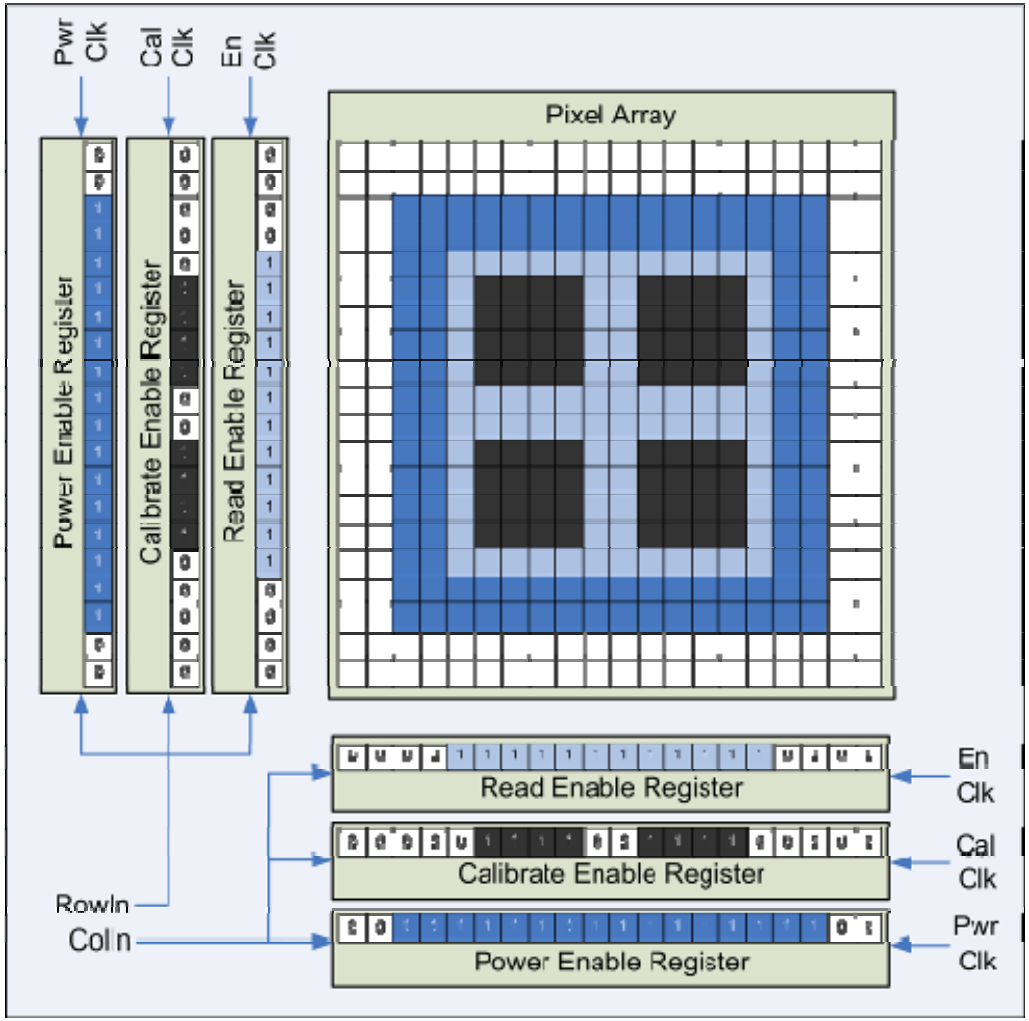
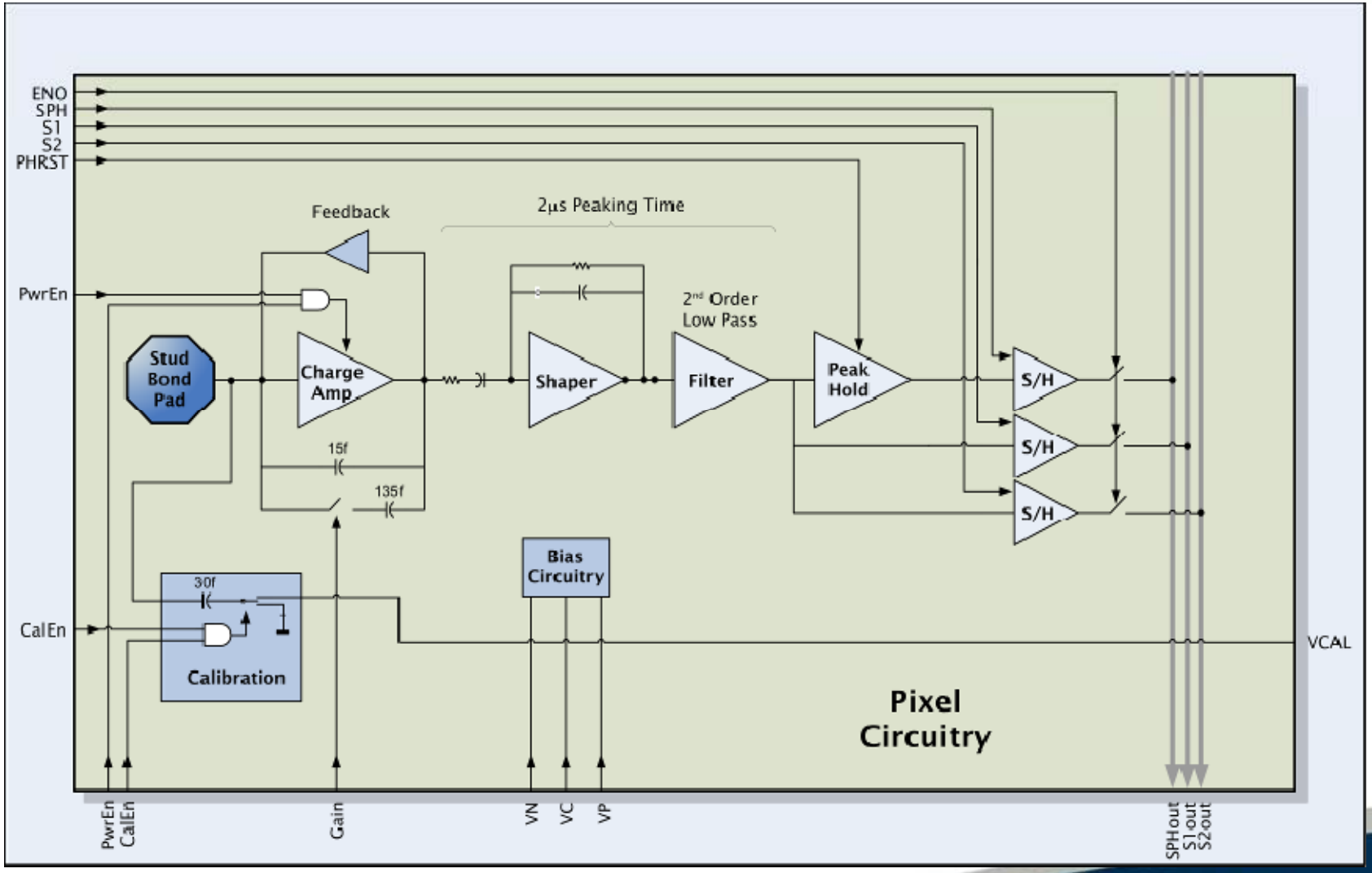
Programmable Regions of Interest



- Three shift registers
- Control regions of interest
- Read enable register
- Calibrate enable register
- Power enable register
- Independently programmable

HEXITEC ASIC Pixel Electronics



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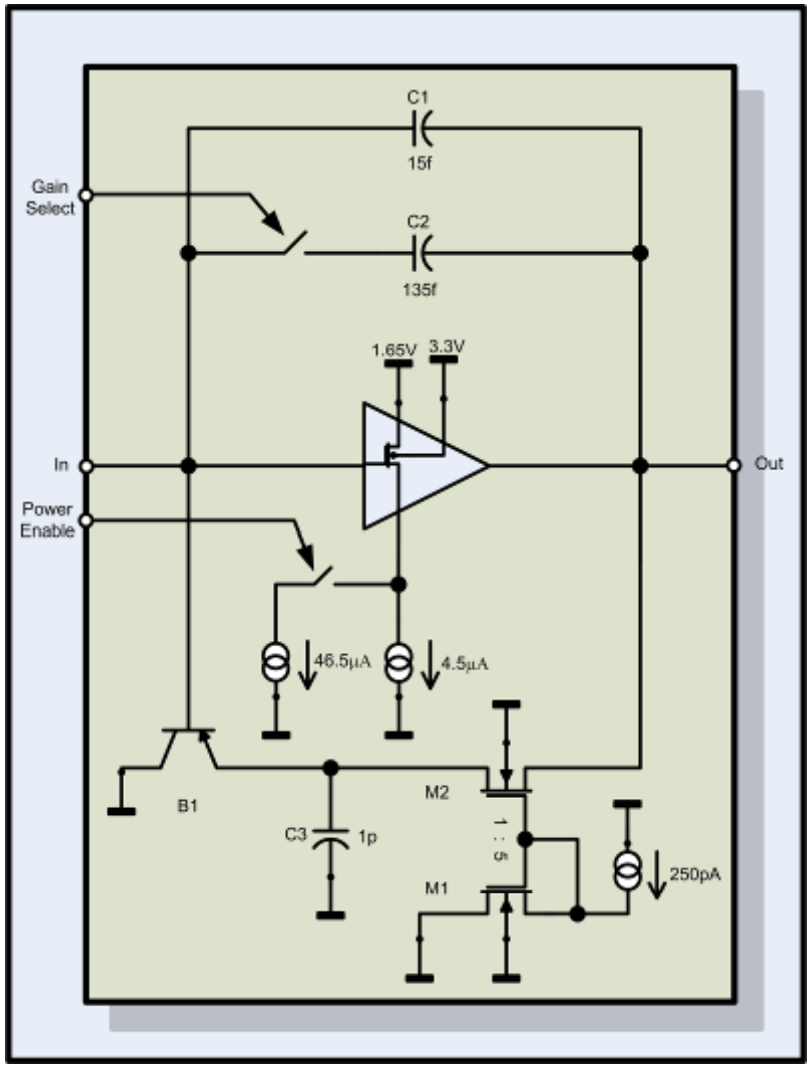
Preamplifier Schematic



- Single-ended, folded cascode
- Selectable gain
- 40 000 or 400 000 electrons
- Power down mode
- Compensates up to 250pA leakage current
- Input FET biased at 1.65V
- Three main noise contributors
- Input FET, Feedback (M2), detector leakage current
- 20 electrons rms noise at 5pA leakage (after filtering)

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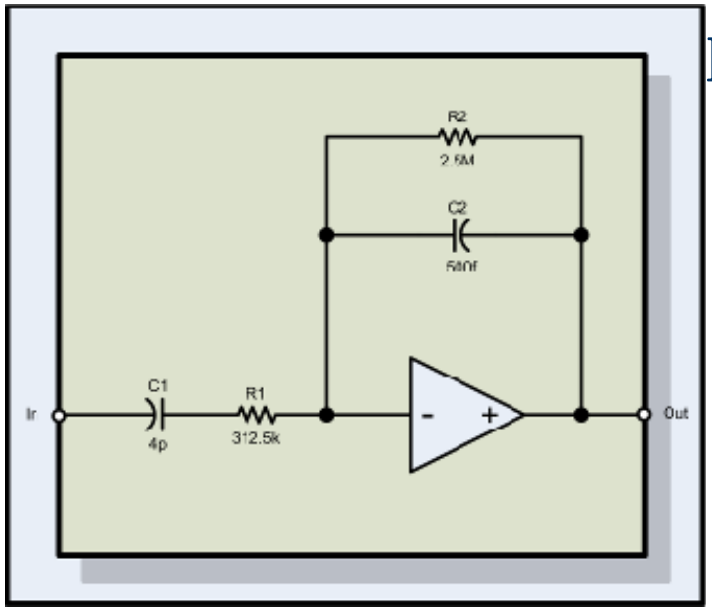
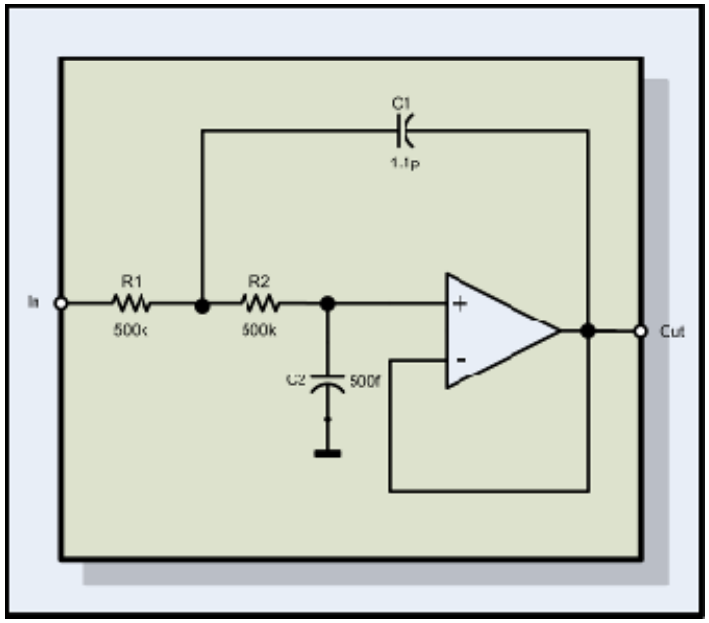
Noise Filtering



- CR-RC band pass filter (1.25µs)
- Single-ended folded cascode
- Not optimum shaping time for noise
- Cannot meet noise specification



- 2nd Order low pass filter
- Filters noise above 1MHz
- Peaking time of signal is 2µs
- Differential amplifier

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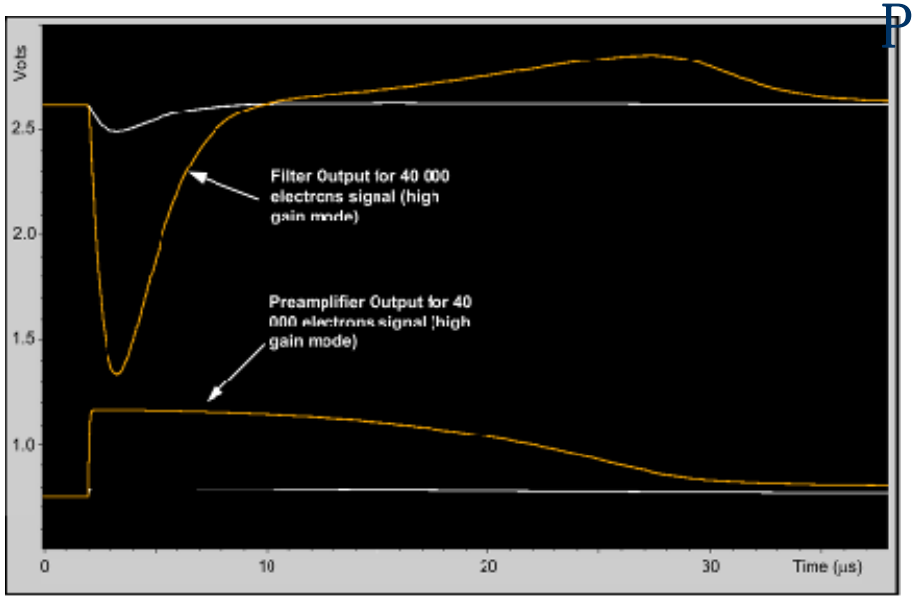
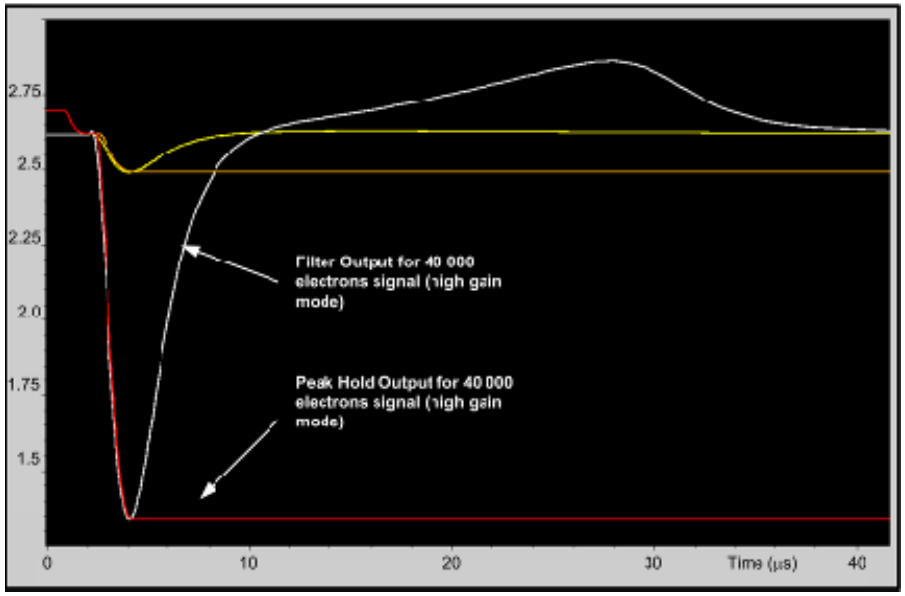
Pixel Simulations 1



Preamplifier / Filter

- Non linear feedback
- Meets noise specification
- Reasonable preamplifier recovery time



Filter/ Peak Hold

- 2µs peaking time
- Must hold for a whole frame readout

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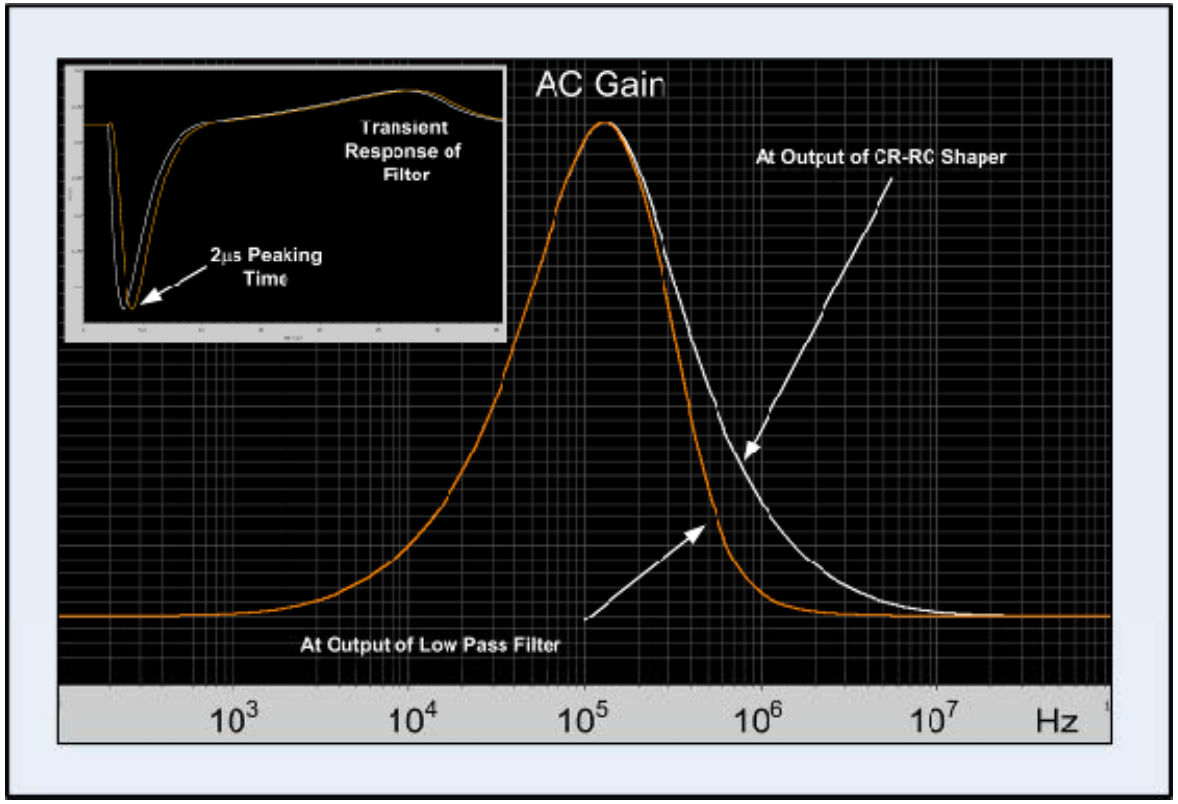
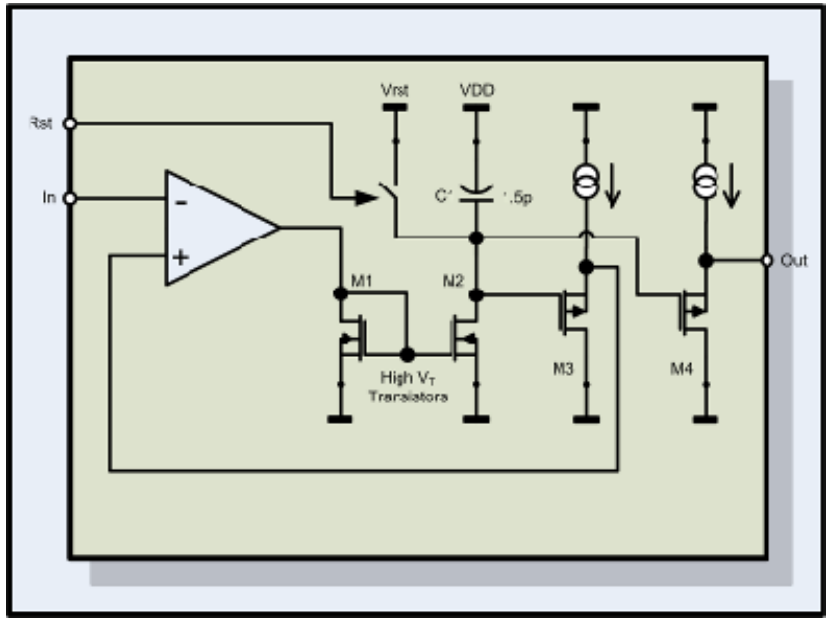
Pixel Simulations 2

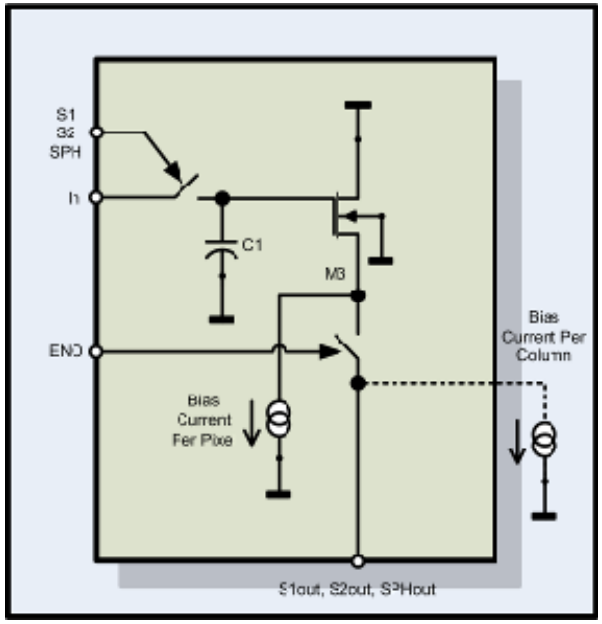


CR-RC Shaper / Filter

- Filter Noise > 1MHz
- 2μs peaking time

Data Sampling





- Peak Hold
- Hold time > 500µs to 12 bits
- 5V transistors give less leakage

- Three Sample and Hold circuits
- S1, S2 and SPH samples
- Internal trickle current

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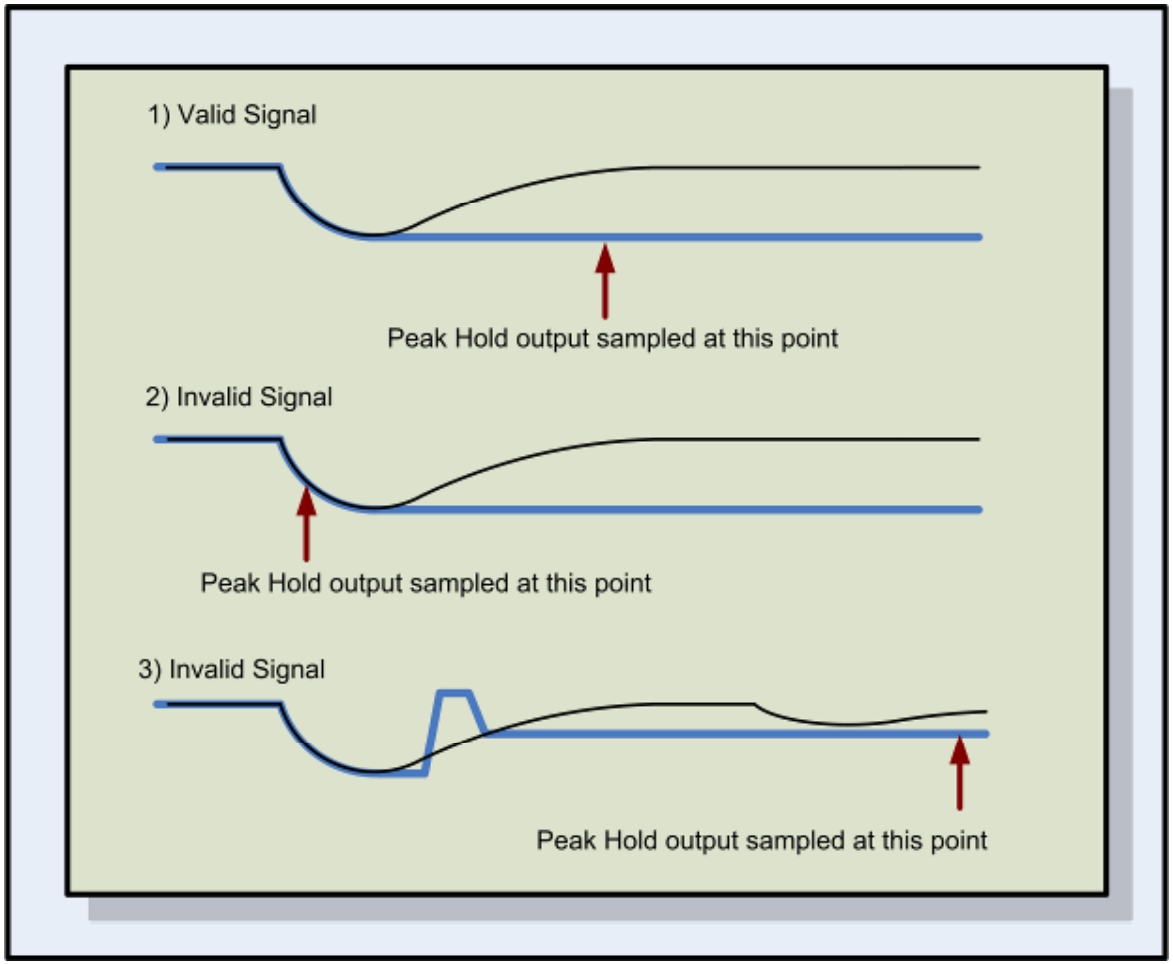
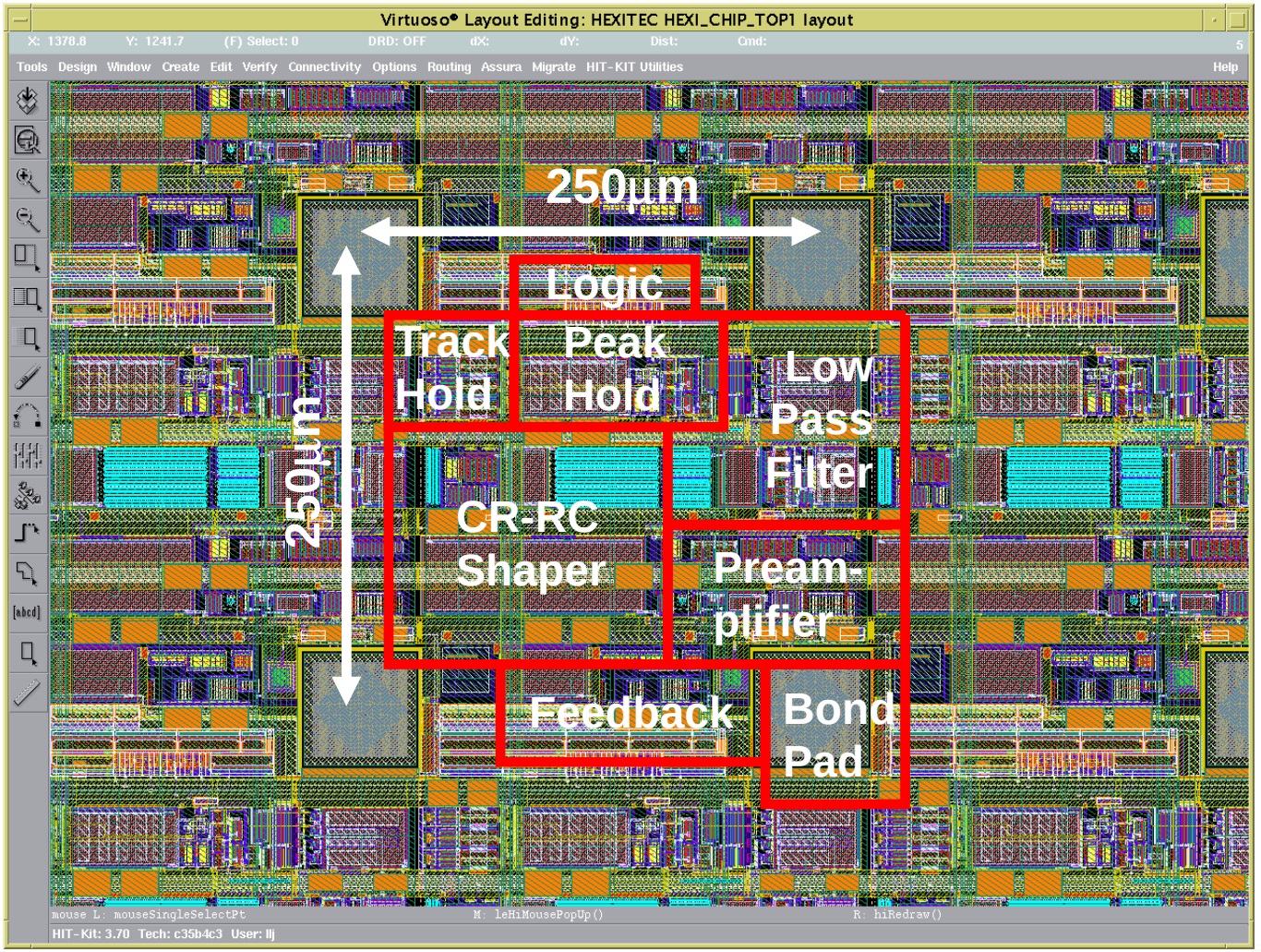
Synchronous Readout Problem



- ✓ Data Sampled after peak value
- ✗ Data Sampled before peak value
- ✗ Peak Hold reset level incorrect

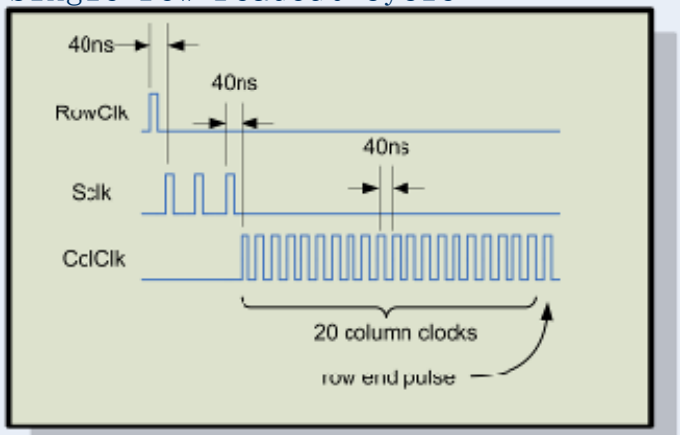
- Sample *filter* output before and after the *peak hold* sample to detect and eliminate erroneous pulses

Pixel Layout



Control Signals and Output Data Format

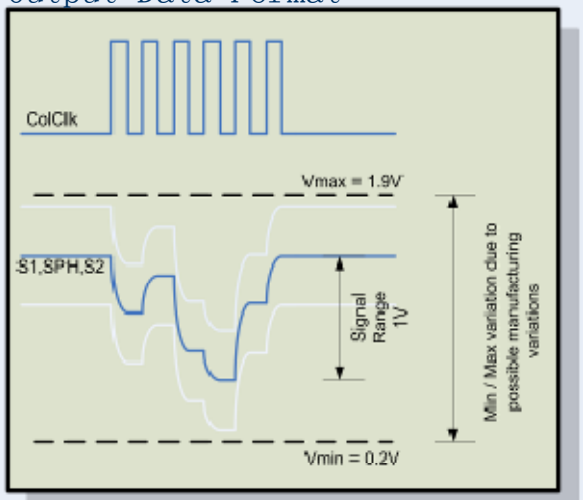
Single row readout cycle



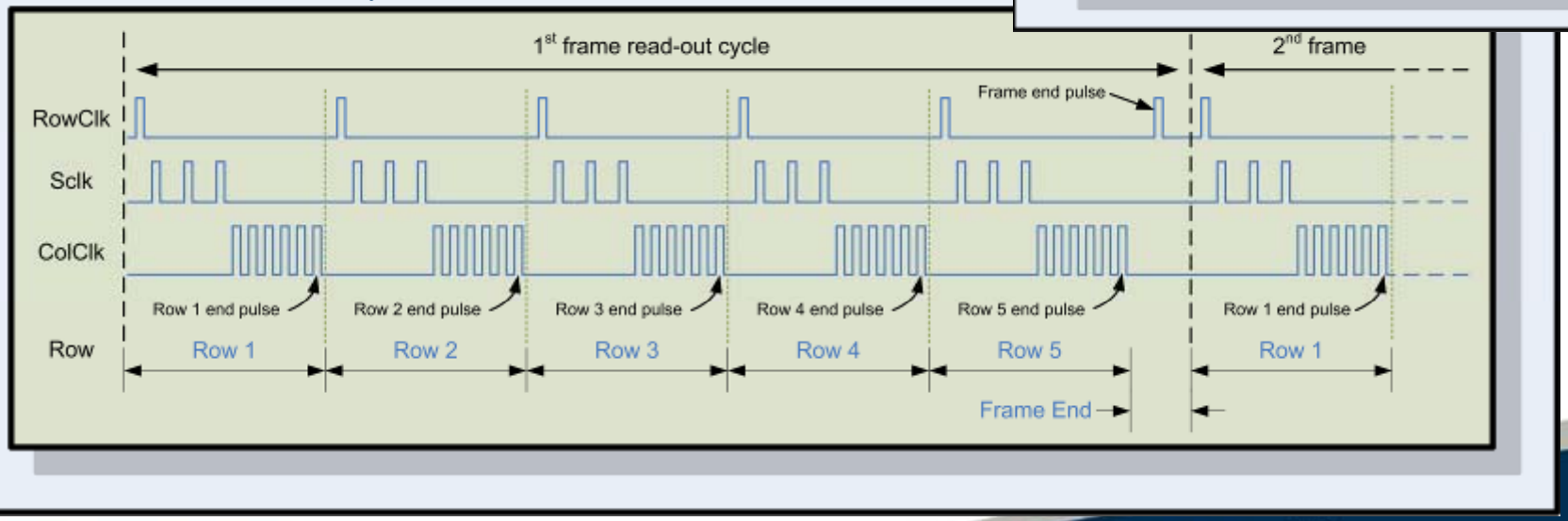
Rolling Shutter

- Row Clock
- Column Clock
- Sample Clock
- ~1µs / row (20)

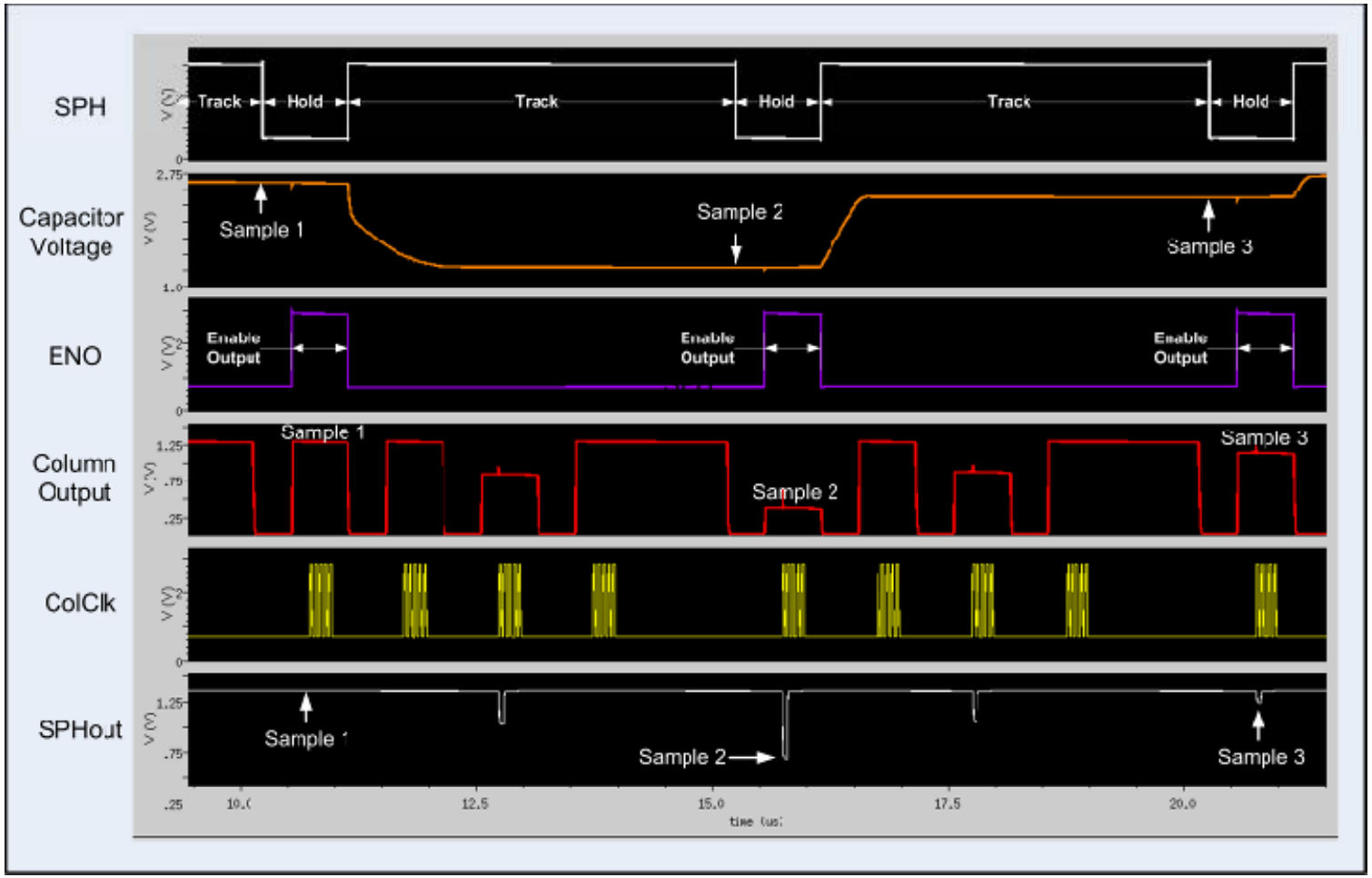
Output Data Format



Full frame readout cycle

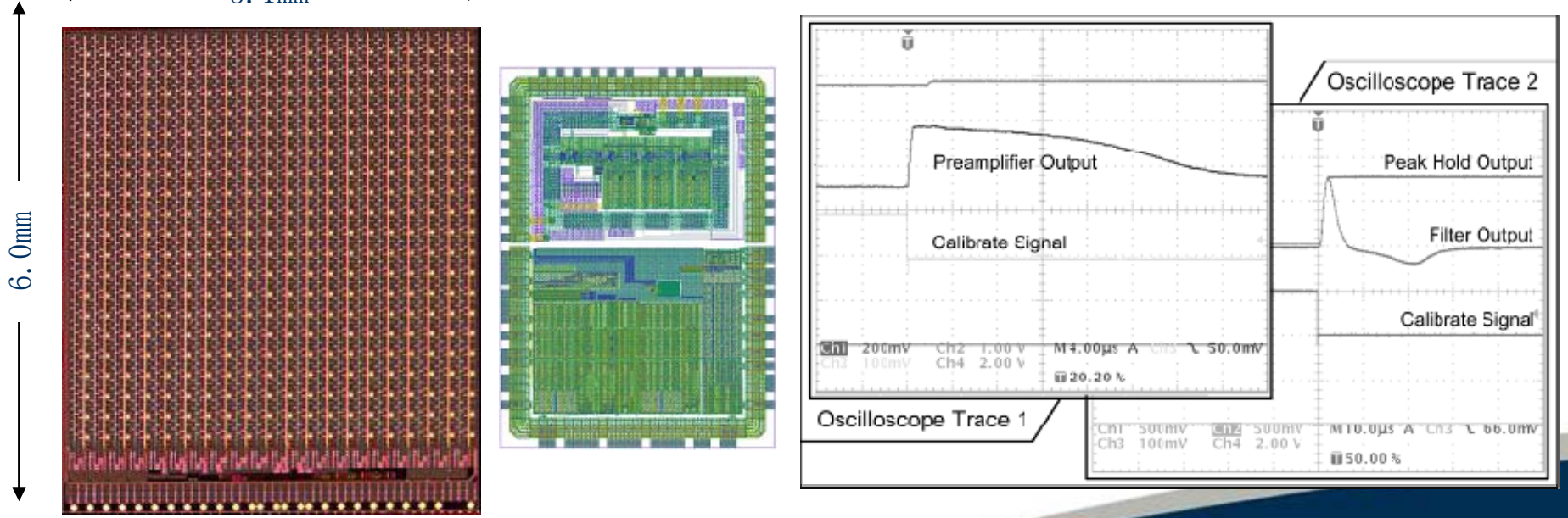


Frame Readout Simulation



Present Status of HEXITEC 20x20 ASIC

- The 20x20 ASIC has been designed and manufactured
- It is untested as data acquisition system not yet ready
- A test structure was manufactured to verify operation of pixel electronics
- Test structure has been tested and the design verified
- g of 20x20 will begin in September



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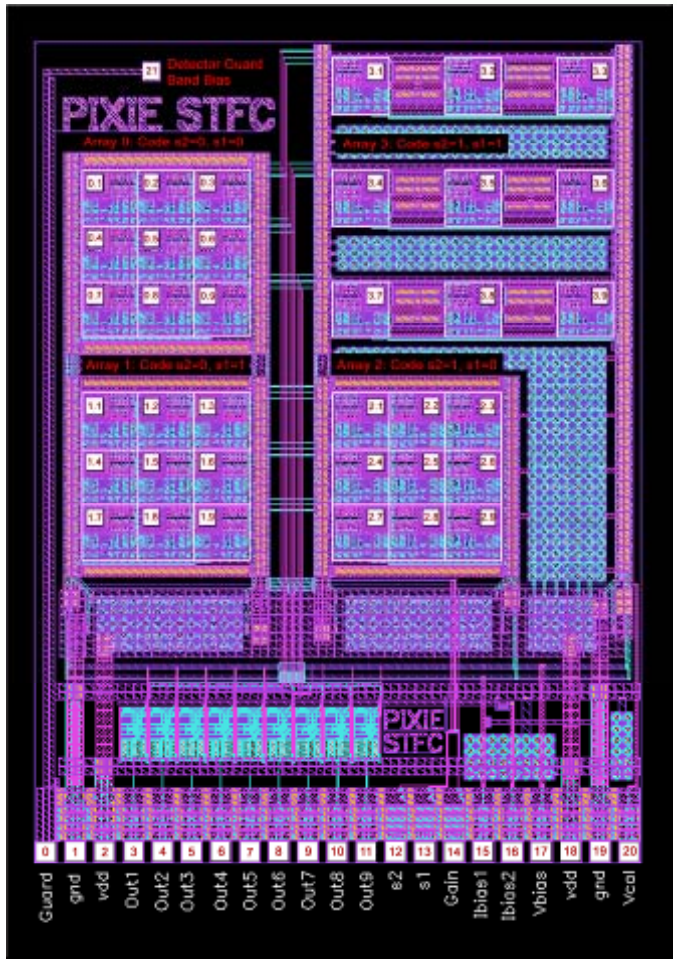
Future Work

- The 20x20 ASIC will be tested
- Design of 80x80 version of the ASIC
- Any problems found with 20x20 will be corrected for the 80x80

Other Work

- PIXIE Chip
- Intended for characterising CZT detector signals
- In fab at moment



Thanks for Listening

Thanks to Paul Seller, Matthew Wilson & Alec Hardie

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