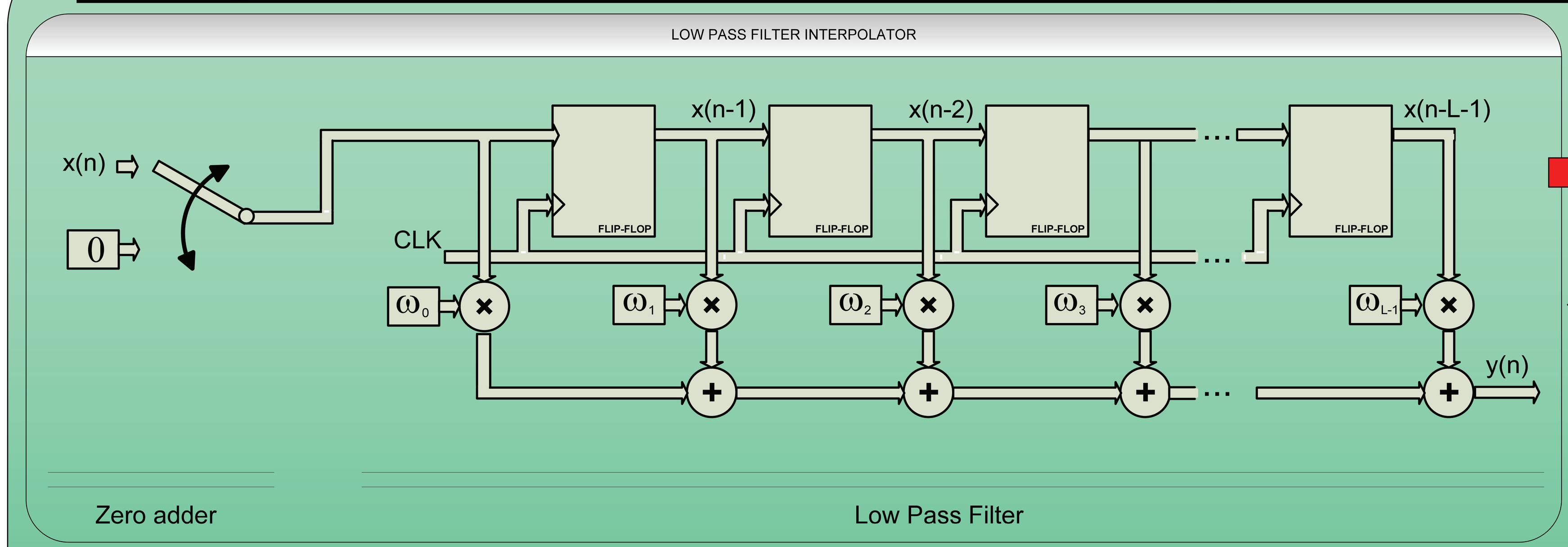
Analysis of Time Resolution in a Dual Head LSO + PSPMT PET System Using Low Pass Filter Interpolation and Digital Constant Fraction Discriminator Techniques

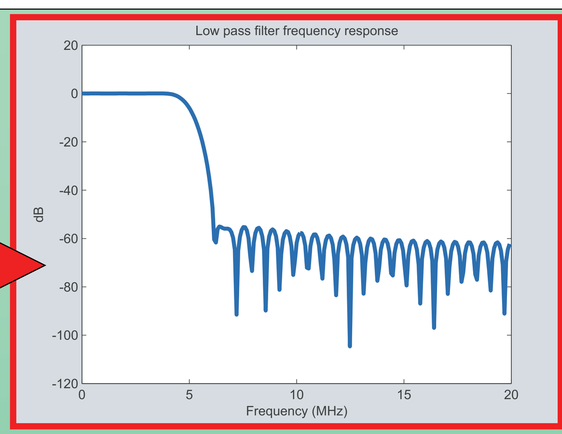
J. M. Monzó[a], C. W. Lerche[a], J. D. Martínez[a], R. Esteve[a], J. Toledo[a], R. Gadea[a], R. J. Colom[a], V. Herrero[a], N. Ferrando[a], R. J. Aliaga[a], F. Mateo[a], F. Sánchez[b], F. J. Mora[b], J. M. Benlloch[b], and A. Sebastiá[a].

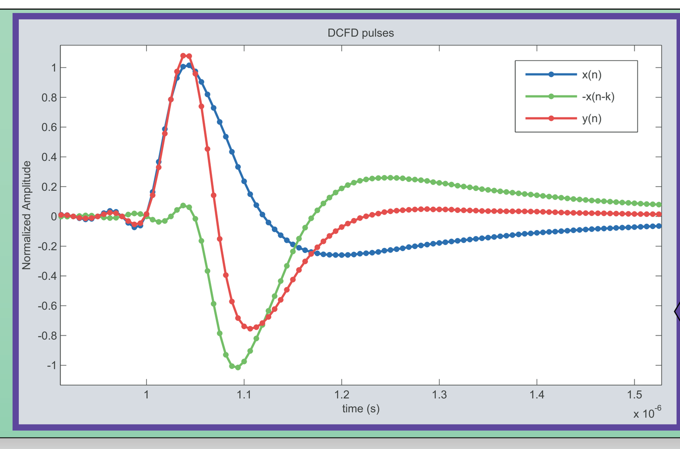
[a]*Digital Systems Design (DSD) group. ITACA institute. Universidad Politécnica de Valencia*

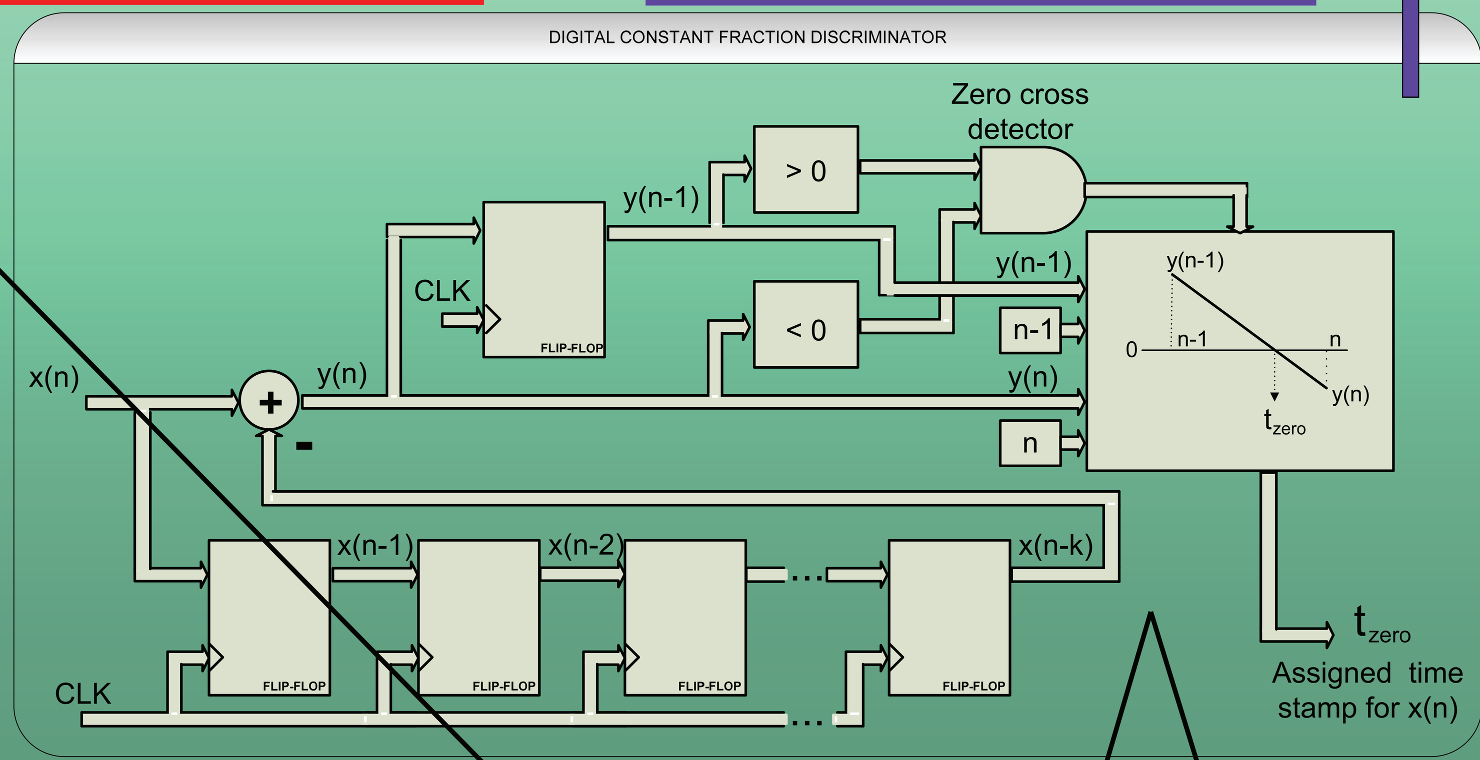
[b]*Nuclear Medical Physics Group. Instituto de Física Corpuscular (IFIC). Consejo Superior de Investigaciones Científicas (CSIC)*

Digital time extraction algorithms









PET systems need a good time resolution to improve true events rate, random events rejection, and pile-ups rejection. In this work, a digital procedure is proposed for this task based in a low-pass filter interpolation plus a Digital Constant Fraction Discriminator (DCFD). It is analyzed the best way to implement this algorithm applied to our dual head PET system [1] and how varying the quality of the acquired signal and electronic noise analytically affects in timestamp resolution. The test bench developed simulates the electronics and digital algorithms using Matlab®.

Low-Pass filter interpolation technique [2],[3]: It is based in Nyquist sampling theorem properties to over-sample the digital signal without loss of information. The interpolation process increases the sampling rate by L. This process is divided into two stages. Firstly, L-1 zeros are introduced between the original samples (1), Secondly, the signal is filtered using a low pass filter with a cut frequency equal to 1/(2L) (2).

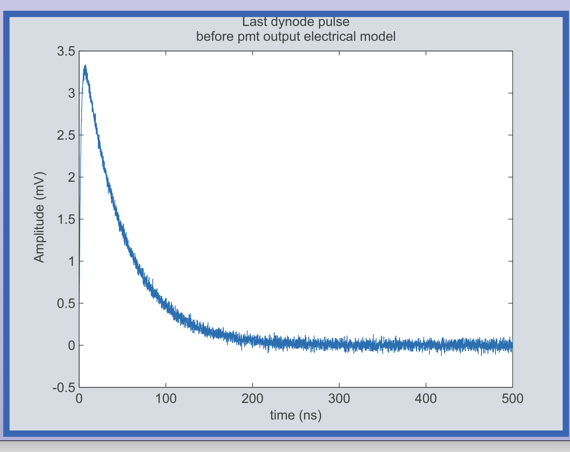
$$w(n)=\begin{cases} x(n/L), & n=0\pm L,\pm 2L,\dots \\ 0, & \text{Other case}\end{cases} \quad (1); \qquad y(n)=\sum_{k=-M}^{M} h(k)\cdot w(n-k) \quad (2)$$

Digital Constant Fraction Discriminator [4]: The received or interpolated signal is copied, inverted, and introduced in a shift register where it can be delayed a fixed number of samples. Choosing the best delay k, the delayed inverted signal is added to the original one (3).

$$y(n)=x(n)-x(n-k) \quad ,(3)$$

The new signal has two samples near the zero value. The two samples define a line that crosses zero in a time that is considered the timestamp for the received pulse.

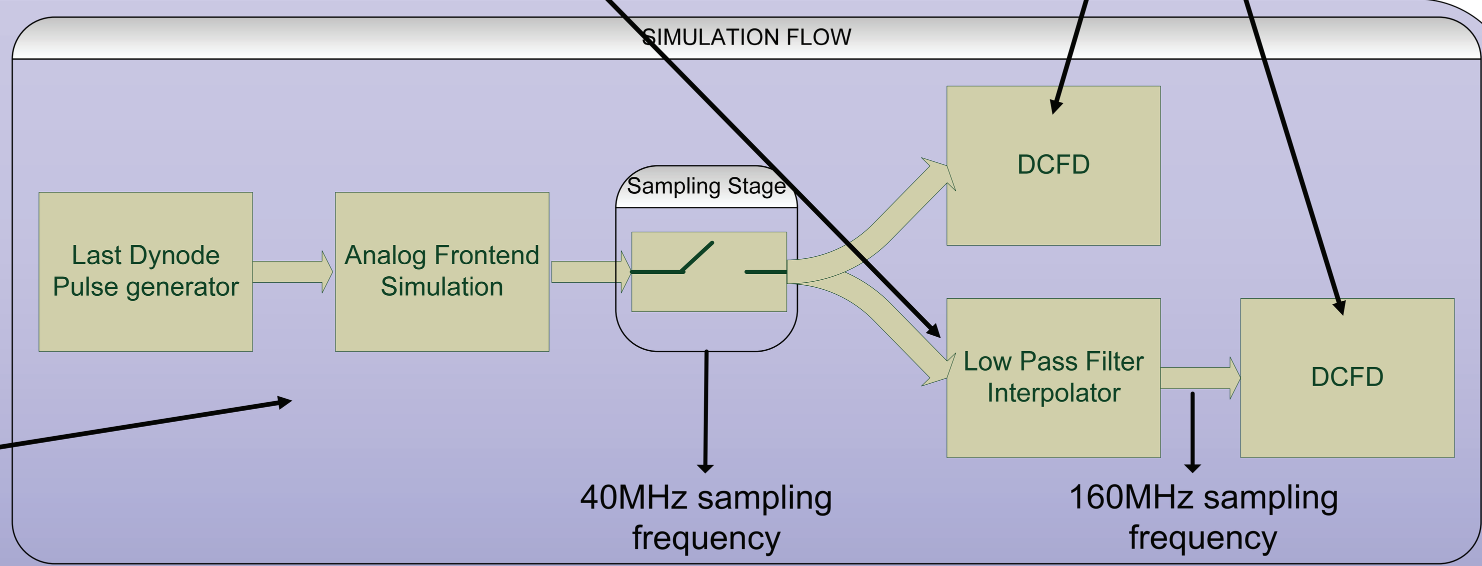
Simulation Testbench

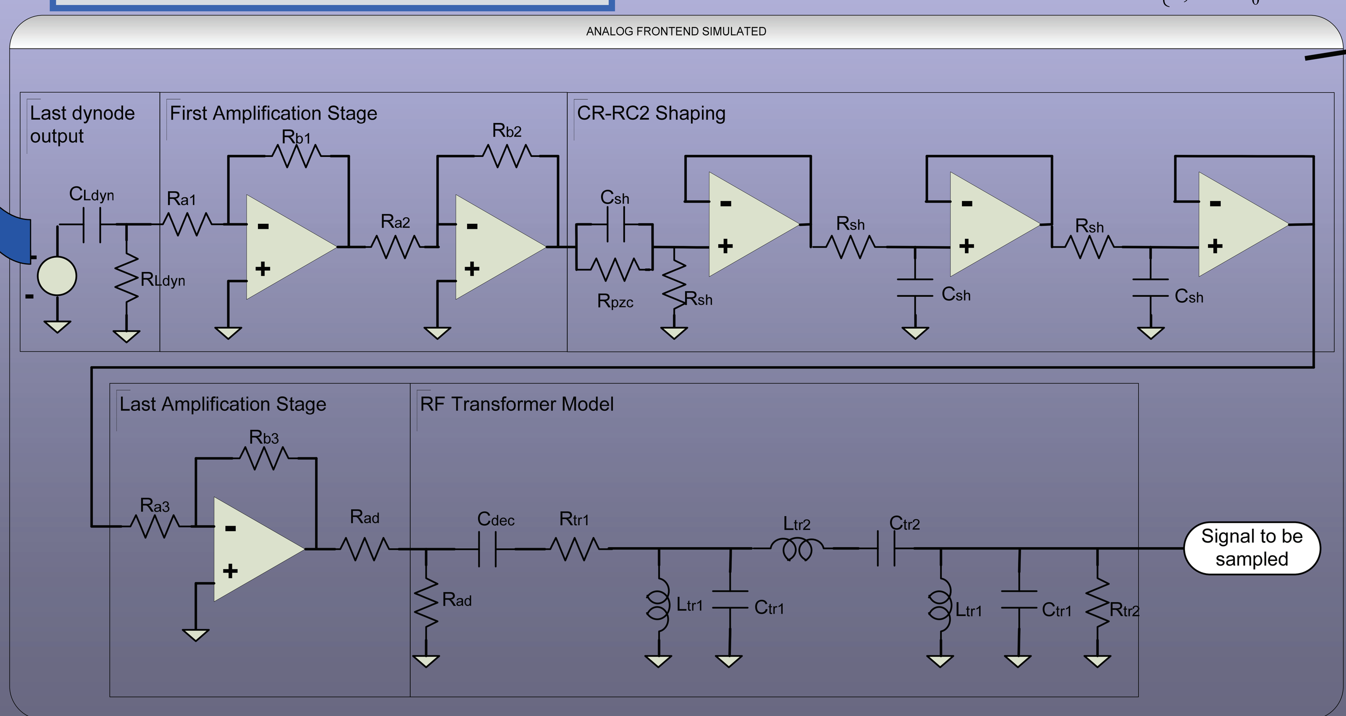


Ideal signals from LSO+PSPMT before last dynode output stage have been generated (4), where A is the amplitude of the pulse, τ_{LSO} is the LSO decaying time, τ_{PMT} is the PMT rise time constant, and t_0 is the event time($\tau_{LSO}=47$ ns and $\tau_{PMT}=2$ns in our test bench).

The main advantage of using ideal pulses is that it accelerates the simulation, without modifying the results, which are very similar to those measured with an oscilloscope at the set-up and those generated with geant-4 simulated through the last dynode stage. A Normally distributed noise has been added to the ideal pulse emulating PMT electron fluctuations.

$$V(t)=\begin{cases} A\left(\exp\left(-\frac{t-t_0}{\tau_{LSO}}\right)-\exp\left(-\frac{t-t_0}{\tau_{PMT}}\right)\right), & t>t_0 \\ 0, & t<t_0\end{cases} \quad (4)$$





Several Noise effects have been considered:

- **The sampling clock phase has been simulated using uniformly distributed values for each sampled pulse.**
- **The sampling clock jitter has been simulated using uniformly distributed values extracted from the electronic specifications jitter values (880ps peak-to-peak). This error affects independently all the sampling times.**
- **Electronic noise (dependent on the signal value) is considered using a normal distribution that affects the pulse before being sampled. Different FWHM are used for this noise: 15% of the instantaneous value of the signal, 10%, 5%, 1% and no noise.**
- **Ambient noise is simulated as a normal distribution, independent of signal value. Different FWHM values are used for this noise: 5mV, 3.3mV, 1.6mV, 0.3mV and no noise.**
- **The pulse amplitude variations that emulate the energy resolution have been simulated using a normal distribution with a FWHM error of 15% fixed in all the simulations.**

Analog Frontend simulation: **The circuit simulation has been done using SCAM[5], a free Matlab® tool for symbolic solution of circuit equations. The simulated circuit includes the last dynode output stage, the signal amplification, the CR-RC2 shaping with pole-zero cancellation, and the RF transformer. The shaping capacitors (Csh) and resistors (Rsh) have been chosen to have a peaking time of 50 ns, having enough samples in the rise time of the signal to process it.**

Results and conclusions

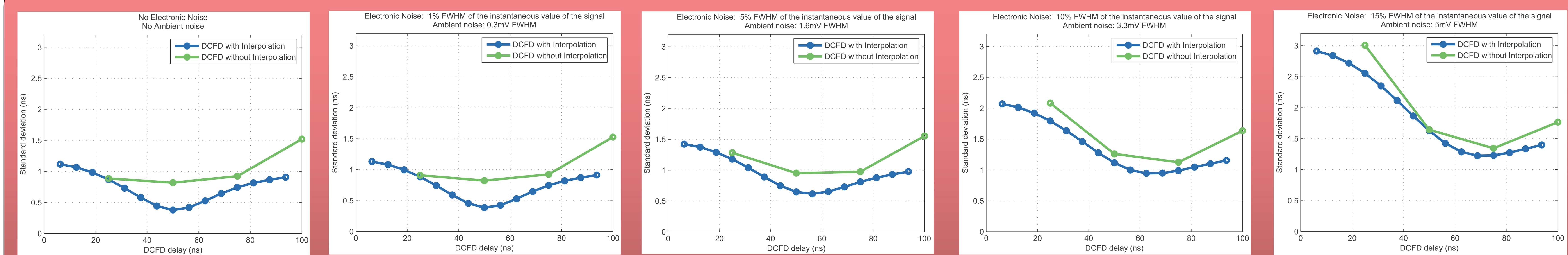


TABLE I
BEST RESULTS FOR DIFFERENT NOISE CONFIGURATIONS

Time extraction algorithm	No Electronic Noise No Ambient noise		Electronic Noise: 1% FWHM Ambient noise: 0.3mV FWHM		Electronic Noise: 5% FWHM Ambient noise: 1.6mV FWHM		Electronic Noise: 10% FWHM Ambient noise: 3.3mV FWHM		Electronic Noise: 15% FWHM Ambient noise: 5mV FWHM	
	Std. deviation	Best Config.	Std. deviation	Best Config.	Std. deviation	Best Config.	Std. deviation	Best Config.	Std. deviation	Best Config.
DCFD with Interpolation	0.3778 ns	50 ns shift	0.3866 ns	50 ns shift	0.6163 ns	56.25ns shift	0.9452 ns	62.5ns shift	1.2239 ns	68.75ns shift
DCFD without Interpolation	0.8194 ns	50 ns shift	0.8221 ns	50 ns shift	0.9521 ns	50 ns shift	1.1245 ns	75 ns shift	1.3438 ns	75 ns shift

This work was supported by the Spanish Ministry of Education and Science (MEC) under Research Projects FPA2007-65013-C02 and by Generalitat Valenciana local government under research project – (GV/2007/008). J. M. Monzó was also supported by a FPI grant from the Spanish MEC BES-2005-10873

Several noise situations have been evaluated using DCFD with and without interpolation. For each simulation, different DCFD delays have also been evaluated, looking for the best solution. An interpolation factor L=4 has been used, which gives us a new sampling frequency of 160MHz, that can be easily tested in a near future in our acquisition board. 20000 events have been generated and simulated at each simulation.

Representing the standard deviation for different electronic noises at the figures above, with and without interpolation, it can be observed how the noise affects severally to the timing resolution of the system. Interpolated DCFD has better results than non-interpolated DCFD. For high noise environments, differences between interpolated DCFD and non interpolated DCFD are reduced.

Besides, it can be seen that an optimum DCFD delay selection improves time resolution. In non-interpolated signals, this delay can be set in 25 ns steps, and in interpolated signals, in 6.25 ns steps. For this reason, interpolated DCFD has more accuracy to optimize the DFCD delay that gives the best timing results.

To select the algorithm to extract the time information of the received events, the noise that affects the system and the available resources of the acquisition board should be taken into account.

[1] J. D. Martínez , *Estudio y diseño de la electrónica de adquisicion de datos para mamografía por emission de positrons con detectors continuos (Study and design of the data adquisition electronics for a positron emission mammography using continuous detectors)*. PhD. Thesis, Universidad Politécnica de Valencia, 2008.

[2] E.C. Ifeachor, B.W. Jervis, *Digital Signal Processing: A Practical Approach.* Addison-Wesley Publishing Company Inc, 1993, ISBN 0-201-54413-X.

[3] R. Fontaine *et al.,* "Timing Improvement by Low-Pass Filtering and Liner Interpolation for the LabPET Scanner", *IEEE Trans. Nucl. Sci.*, vol. 55, n. 1, Feb. 2008.

[4] "Application Note AN42: Principles and Applications of Timing Spectroscopy", ORTEC®

[5] Erik Cheever. "SCAM: Symbolic Circuit Analysis in MatLab", http://www.swarthmore.edu/NatSci/echeeve1/Ref/mna/MNA6.html