CMS tracker UK bump-bonding requirements

Mark Raymond,
UK bump-bonding,
May 2012.

UK CMS community (Bristol, Brunel, Imperial, RAL)

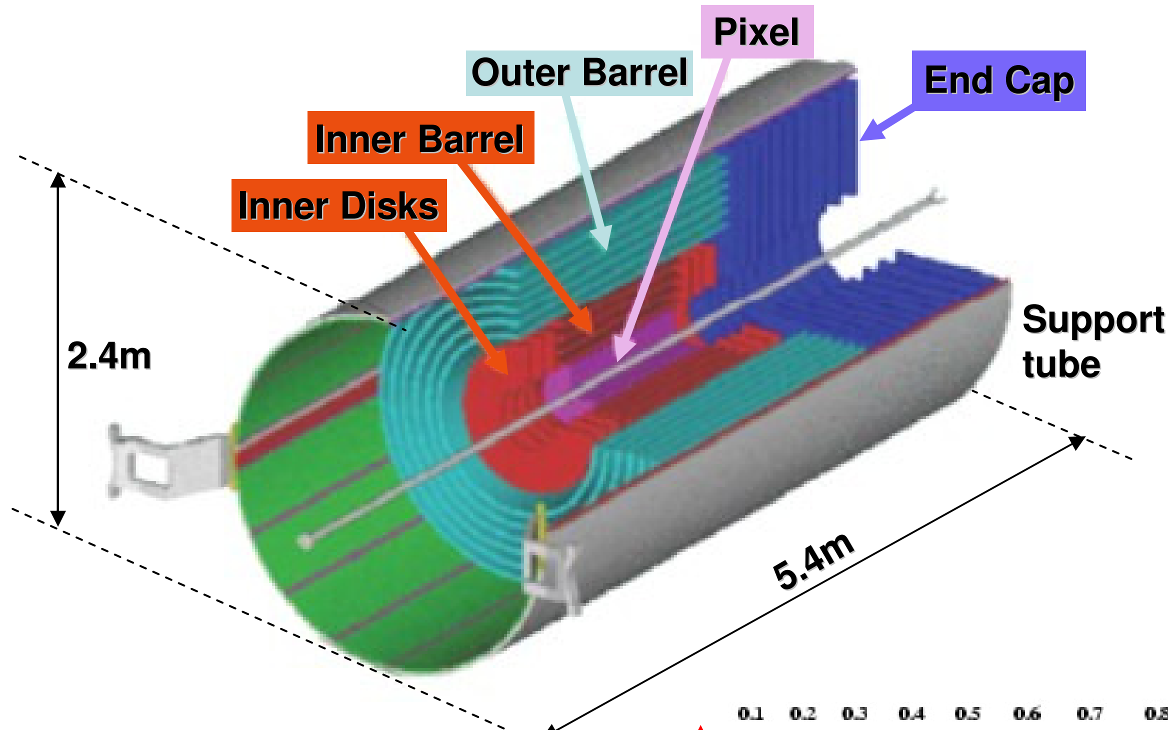
hardware involvement in trigger and tracker

HL-LHC tracker upgrade interests

pixel DAQ (not currently involved with detector module developments)

strip tracker front end electronics - bump-bonding is relevant here

present CMS LHC strip tracker



some numbers

~ 200 m^2 sensor area

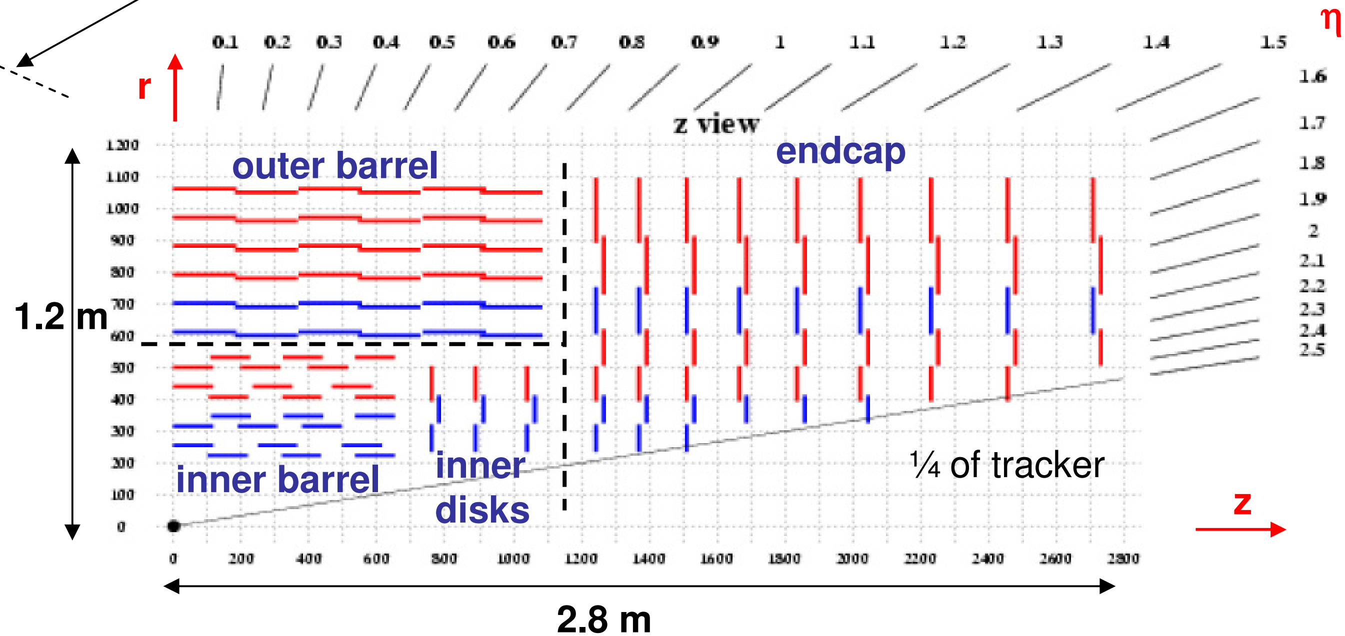
~ 10^7 strips, ~75,000 FE chips (APV25)

~ 15,000 detector modules altogether

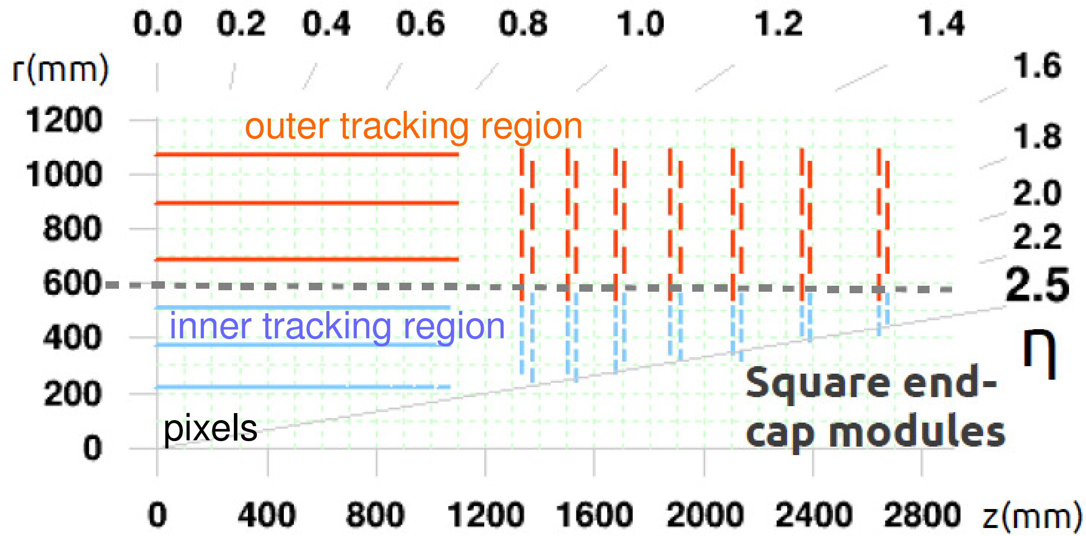
22 different types

all single sided sensors

single layer modules
stereo modules



HL-LHC CMS tracker

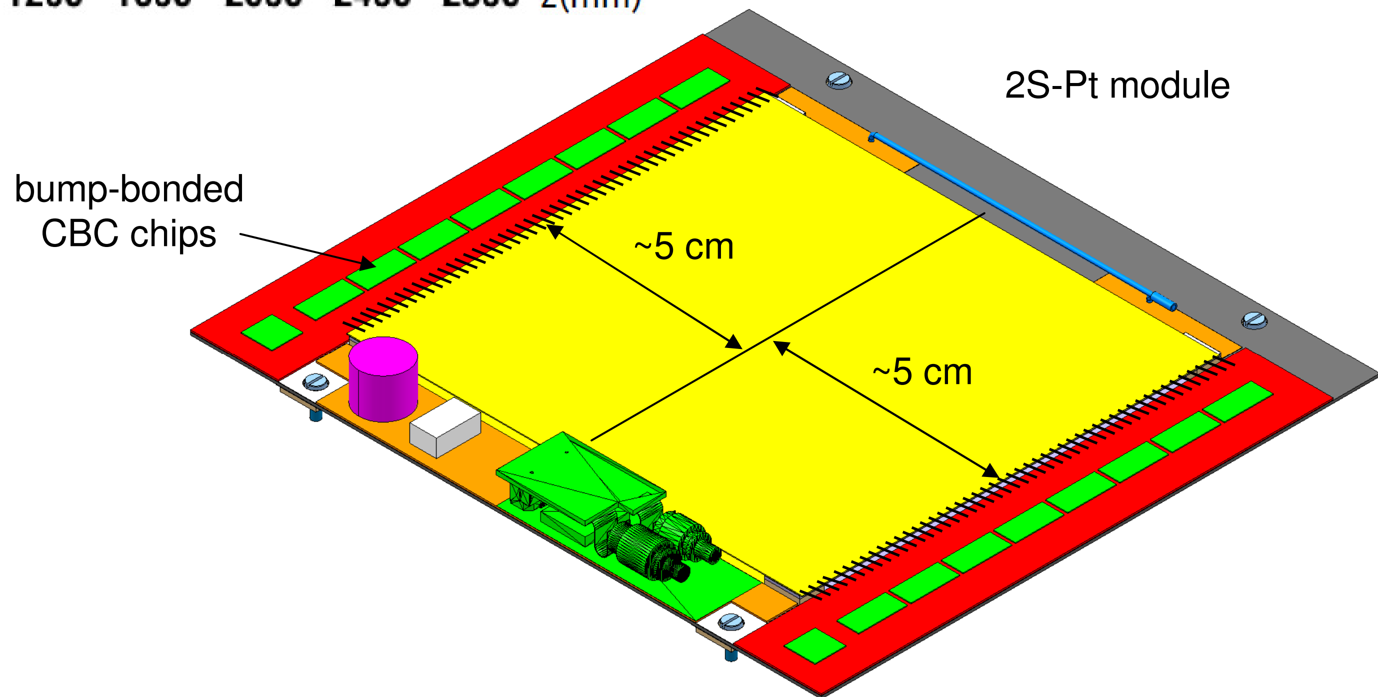


CMS UK developing front end chip for outer tracking region

CBC (CMS Binary Chip)

10x10 cm^2 2S-Pt modules throughout outer tracking region - no variants

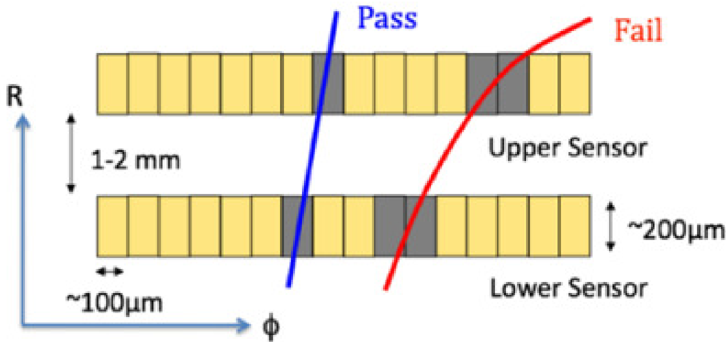
~ 10k modules (rough guess)

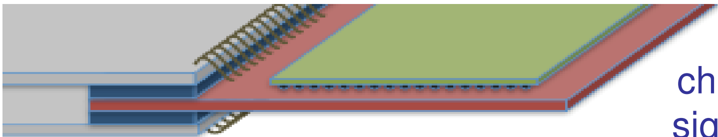


front end module - more detail

2S-Pt module concept proposed for outer tracker layers

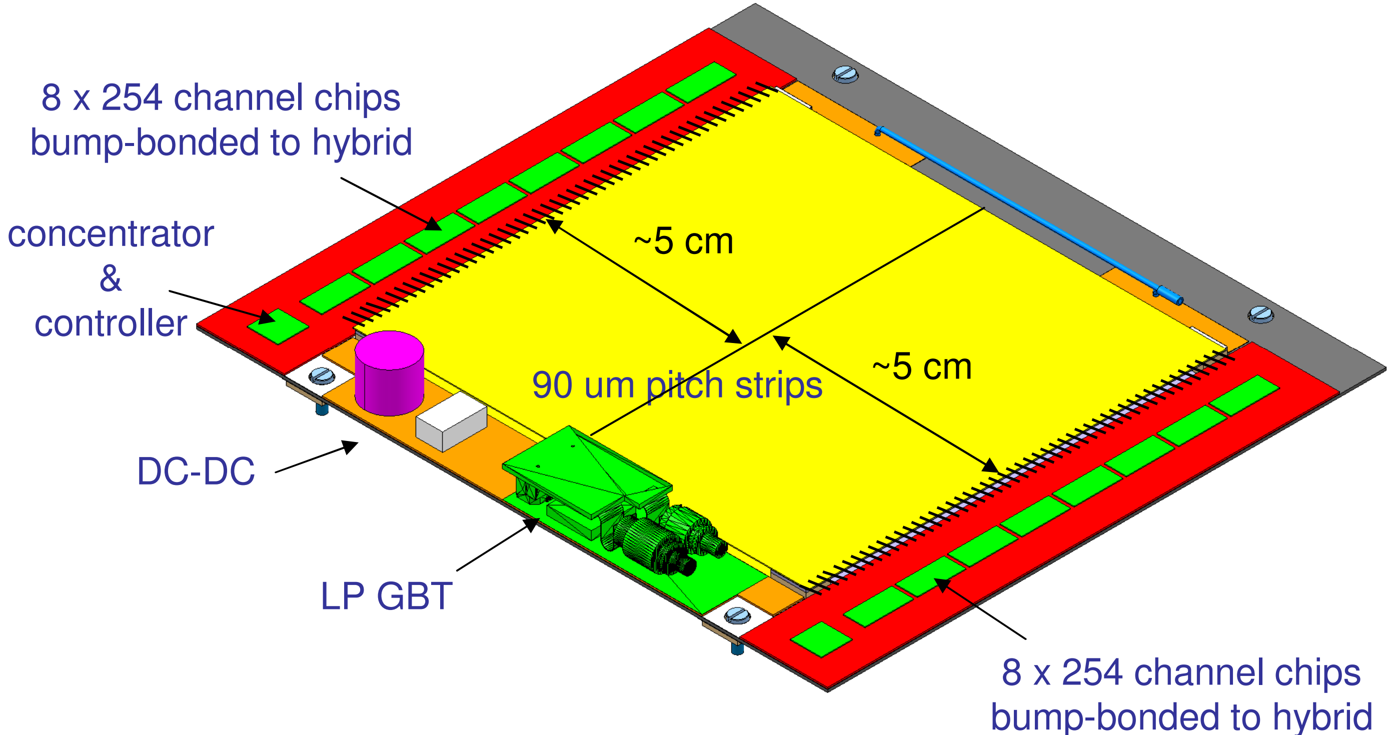
bring signals from 2 strip sensor layers together in one chip
look for cluster correlations to identify high Pt stub





sensors wire-bonded above and below

chips on top surface only
signals from lower sensor
via'd through substrate



CBC(1) -> CBC2

CBC(1) prototype (2011)

130nm CMOS

128 channel wirebond

L1 triggered readout only

works very well

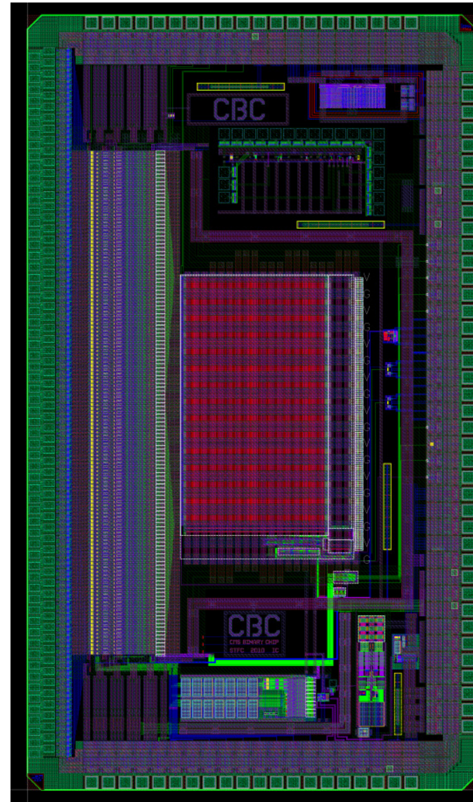
CBC2 - in production soon

L1 triggered readout and Pt stub information

254 channels: allows correlation between 127 strips on top and bottom sensors

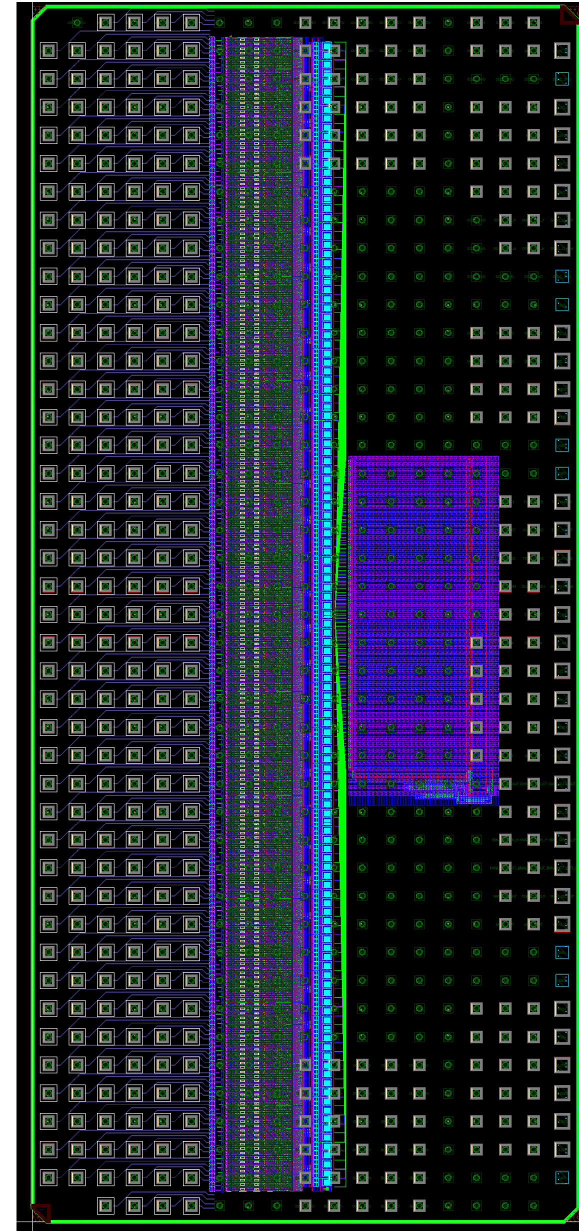
250µm C4 bump-bonding

~ 800 pads



CBC(1)
128 channels
wirebond: 50 um pitch
7mm x 4mm

CBC2
254 channels
C4 bump-bond: 250 um pitch
10.75mm x 4.75mm



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CBC2

why bump-bonding?

no wire-bonding at chip periphery
reduced space requirements

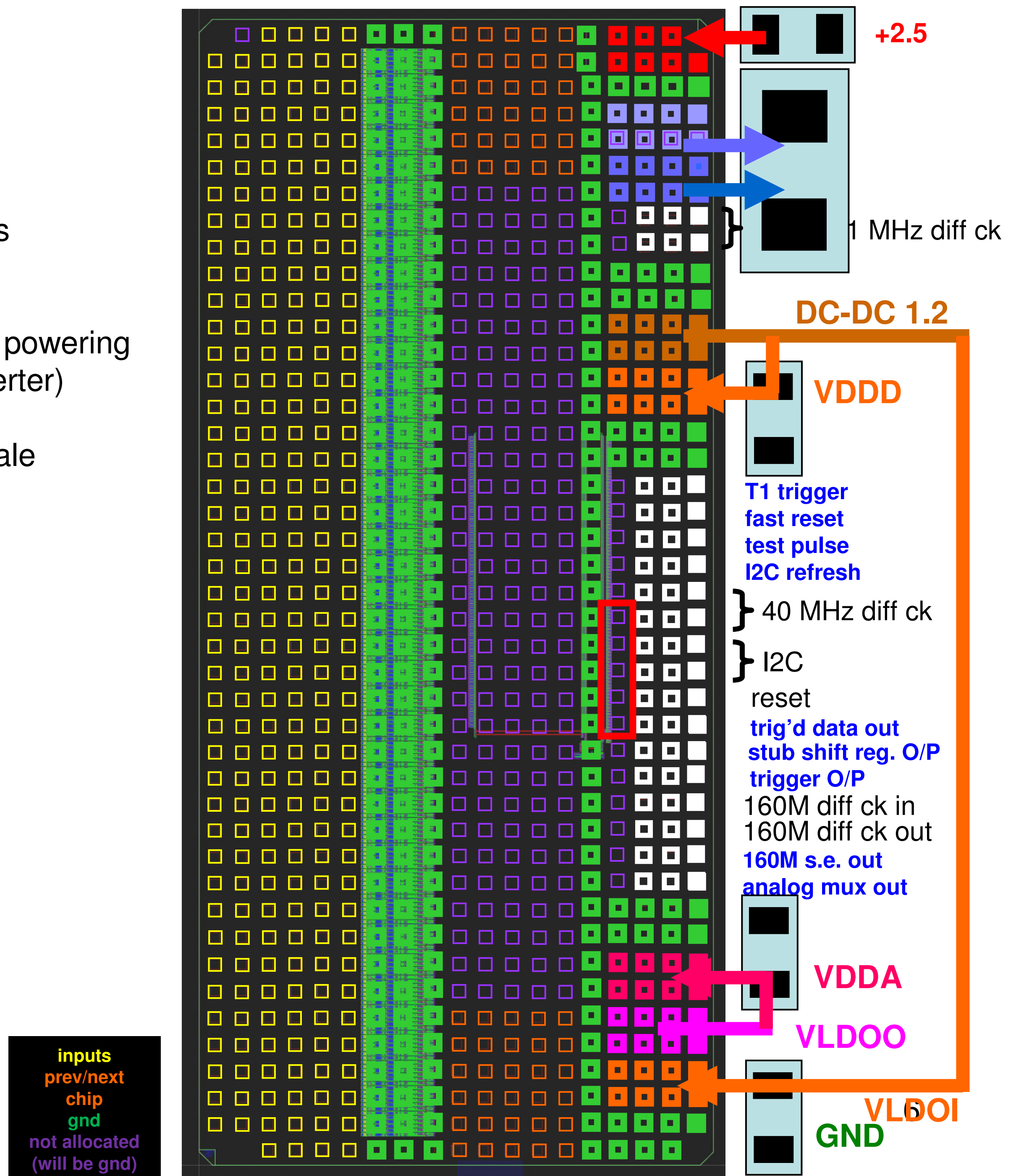
low inductance and resistance
particularly useful for CBC2 powering
(switched cap DC-DC converter)

want to use industry for large - scale production assembly

why 250 - not 200?

as conservative as possible

need high yield over large area



UK bump-bond facility relevance to CBC

for large scale production - probably not

a big task - C4 chosen to facilitate commercial production of module sub-assemblies

(still plenty of assembly, wire-bonding, testing,… to do in the institutes)

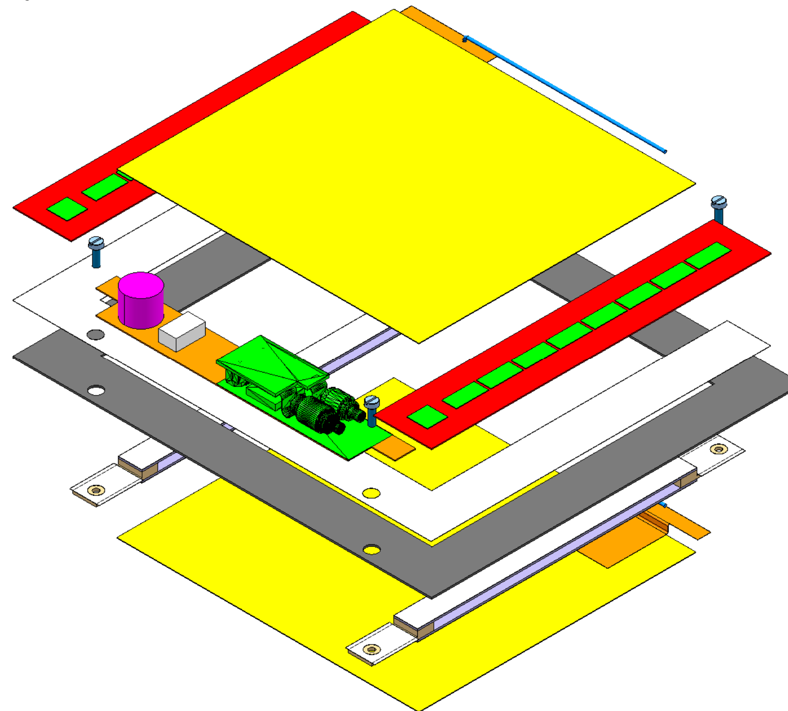
for prototyping and testing – maybe

some commercial prototyping necessary to prove feasibility

but once that achieved it might be more economic to bond further test pieces in-house

in any case we can probably provide C4 chips to try out if that is useful

chips available ~ late 2012



EXTRA

a few slides borrowed from Georges Blanchot's WIT presentation

Hybrid circuits and substrate technologies for the CMS tracker upgrade

G. Blanchot

Rigid substrates

- **Build-up substrates are commonly used for chip packaging.**

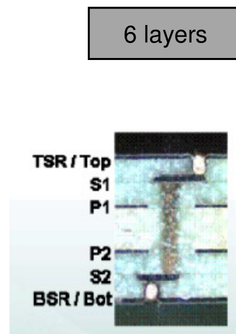
•Core layer provides:

- Power/Ground planes
- Rigid core material.
- Mid density routing and through hole vias.

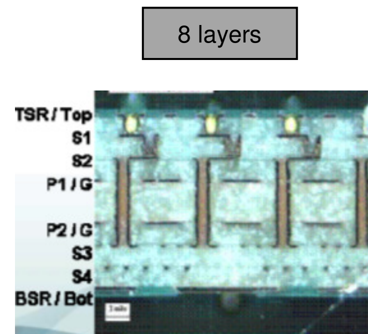
•Build-up layers are laminated on top and bottom of core:

- Very high density interconnections on constrained areas.
- Microvias to connect build up layers to core external layers.
- No through hole vias..

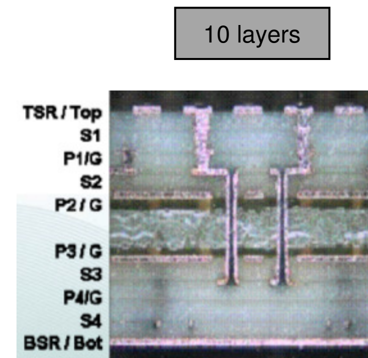
6 layers



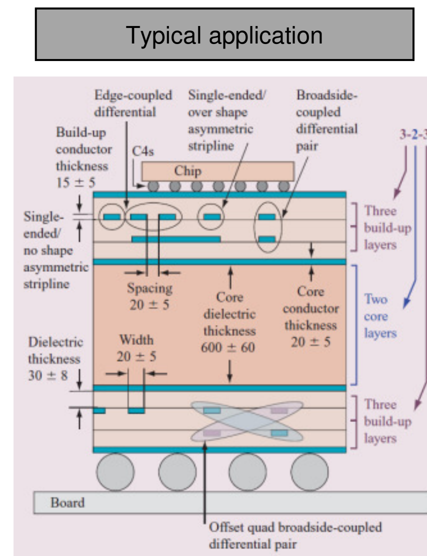
8 layers



10 layers



Typical application



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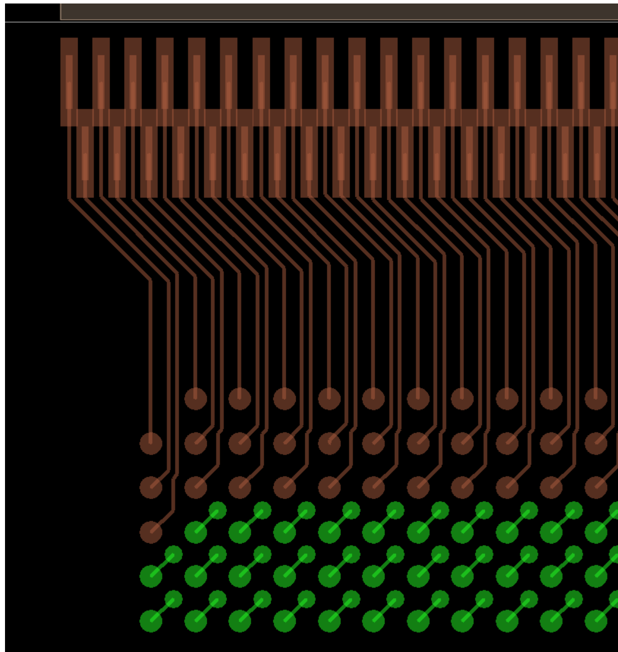
The high density flip chip array imposes the need for high density interconnection substrates.
For example, sensor wirebonding: 25um traces required for straight connection to bond fingers.



- Top sensor bond fingers can be in-line or staggered

•In both cases, the wirebond pads are very close of the sensor edge.

•Traces escape all in same direction without need of vias.

•Traces can still go through 2 adjacent vias without turn arounds.

- Sensor bond fingers are present at same locations on the bottom side:

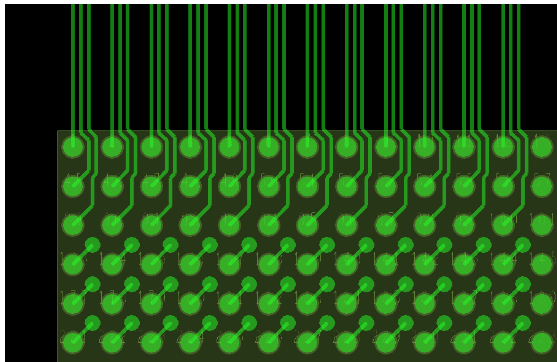
•The connection is possible through the CBC pin escapes via array from the 3 last rows.

•The 3 top rows are associated to the top side sensor.

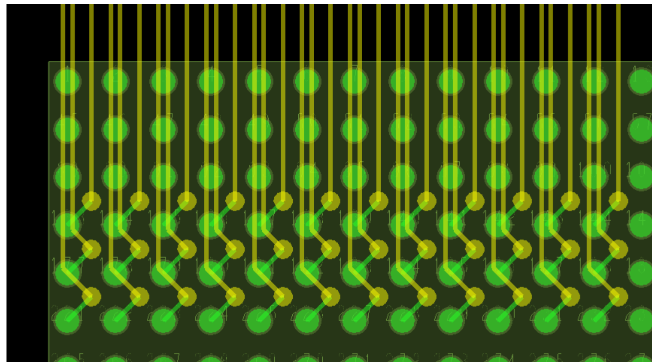
•Microvias, 50 μm drill, 100 μm capture pad are required.

Rigid and flexible substrate technologies are today available with these degree of interconnection densities.

Rows 1, 2, 3: top sensor, straight connection.



Rows 4, 5, 6: bottom sensor, straight connection through pin escapes.

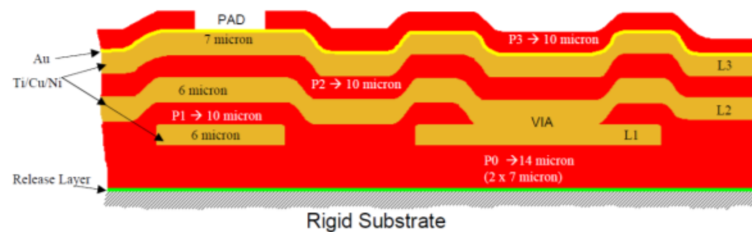


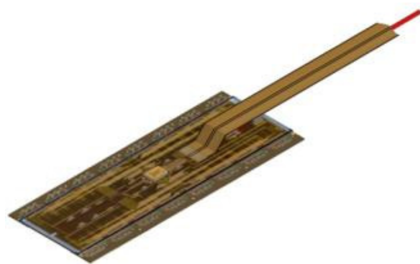
Flexible substrates

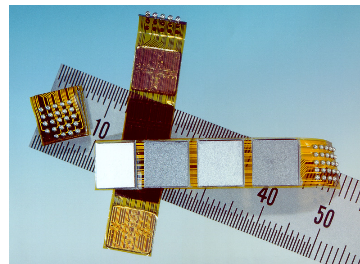
▪ **<u>Flexible polyimide is a quickly emerging technology.</u>**

•Thin film flex technology made of spinned liquid polyimide on square panels.

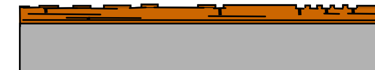
- Very high density layouts: Tracks w/s = 20 µm, microvias = 30 µm.
- Silicon matching CTE = 3 ppm/K.
- Very low mass: Cu thickness < 7 µm, film thickness ≈ 10 µm.
- However: 4 layers maximum, no copper on base layer, limited power delivery capabilities.



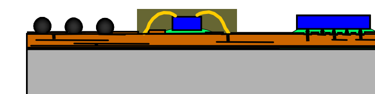




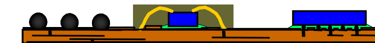
Fabrication of Multilayer Structure on Rigid Carrier Substrate

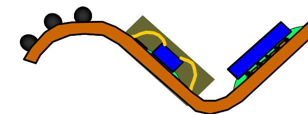


Assembling, Bonding, Protection , Test

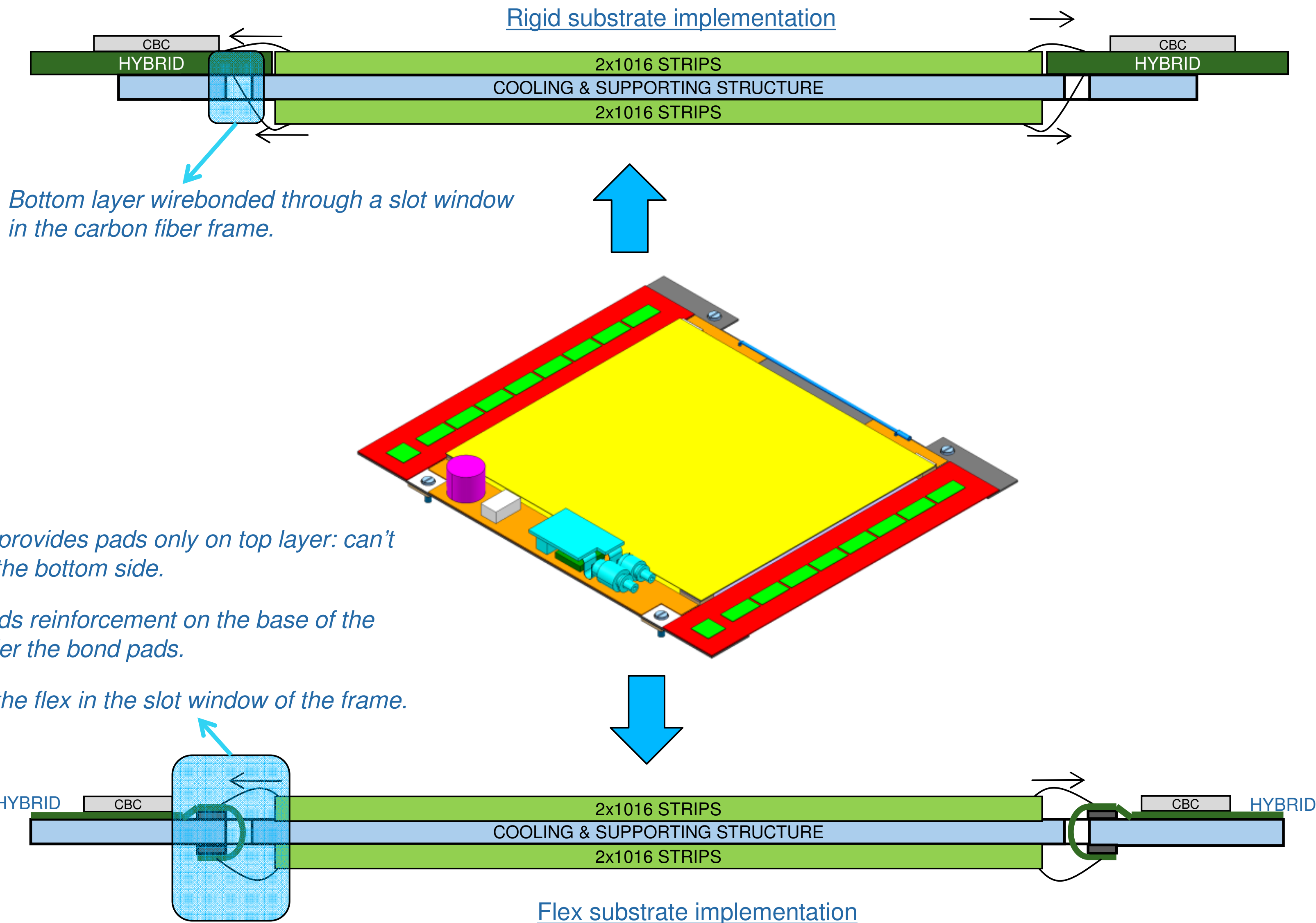


Separation of Multilayer from Rigid Substrate Reuse of Carrier





Flexible substrates for the CMS tracker modules



CBC prototype summary

features

- designed for short strips, ~2.5–5cm, < ~ 10 pF
- full size prototype - 128 channels
  50 µm pitch wirebond
- binary un-sparsified readout
- powering test features
  2.5 -> 1.2 DC-DC converter
  LDO regulator (1.2 -> 1.1) feeds analog FE

main functional blocks

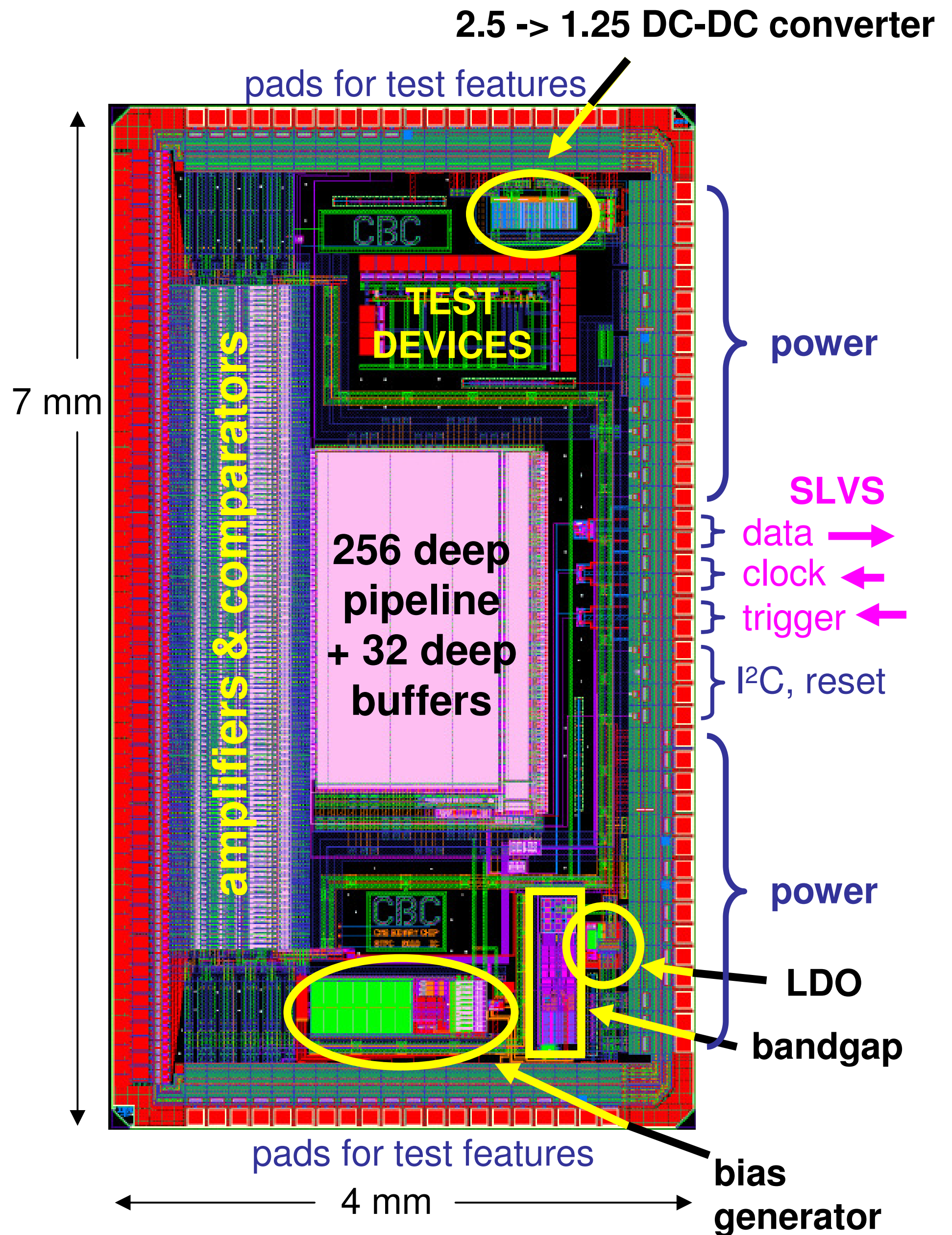
- fast front end amplifier – 20 nsec peaking
- comparator with programmable threshold trim
- 256 deep pipeline (6.4 us)
- 32 deep buffer for triggered events
- fast (SLVS) and slow (I2C) control interfaces

front end

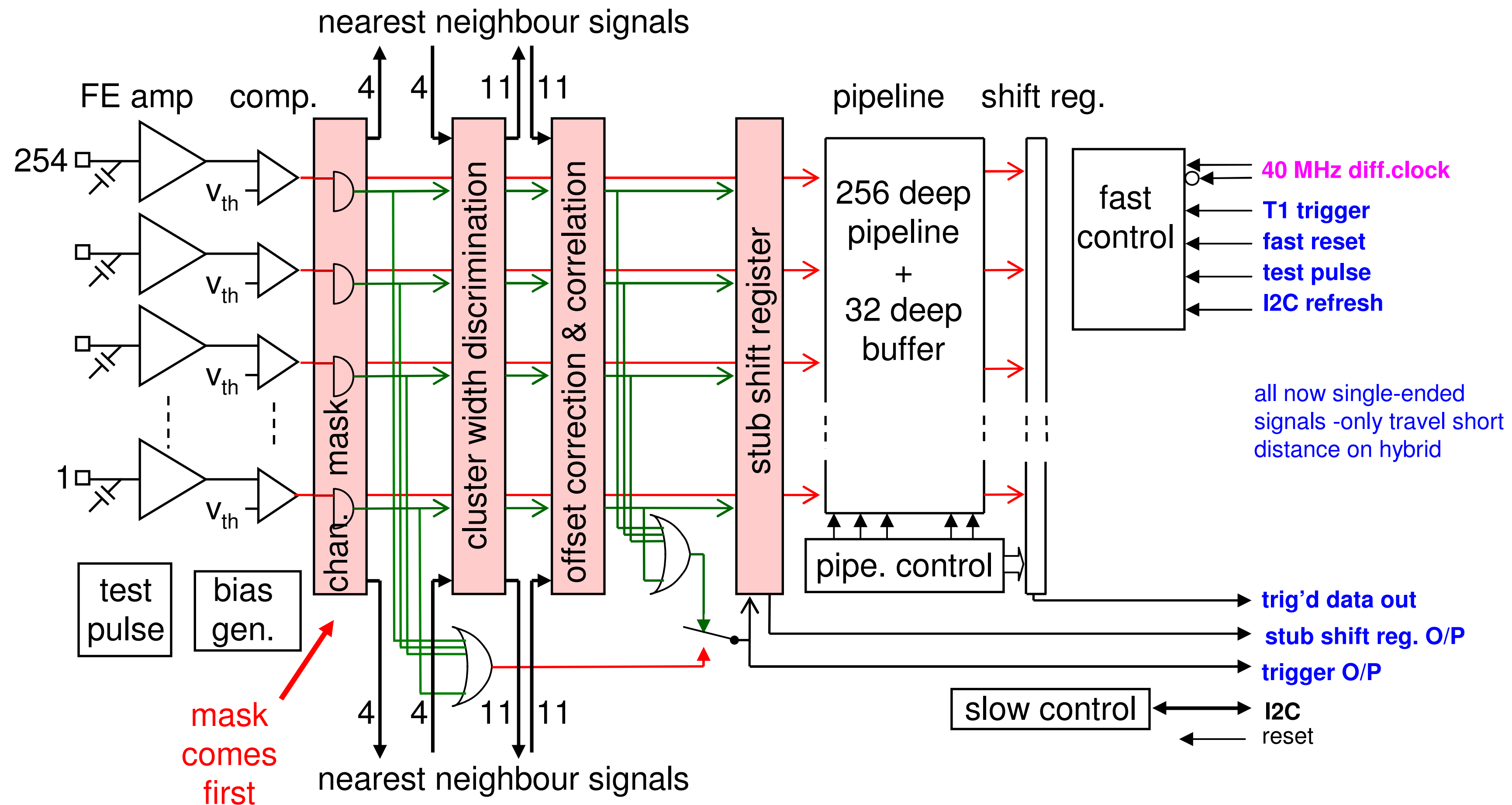
- DC coupling to sensor – up to 1 uA leakage
- can be used for both sensor polarities

for 5 pF input capacitance

noise ~800e
power ~300 µW / chan.



CBC2 architecture



blocks associated with Pt stub generation

channel mask: block noisy channels (but not from pipeline)
cluster width discrimination: exclude wide clusters
offset correction and correlation: correct for phi offset across module and correlate between layers
stub shift register: test feature - shift out result of correlation operation at 40 MHz
fast OR at comp. O/P and correlation O/P: - can select either to transmit off-chip
for normal operation choose correlation O/P

neighbour chip signals - CWD O/Ps

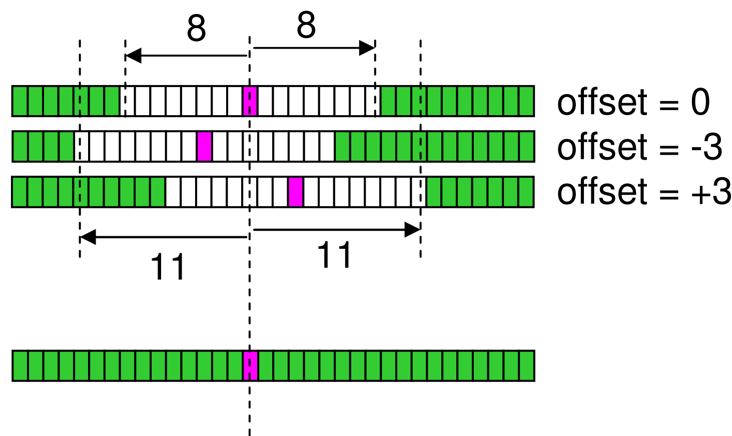
need programmability of **offset** and **window** width for upper layer channels to correlate with hit in inner layer

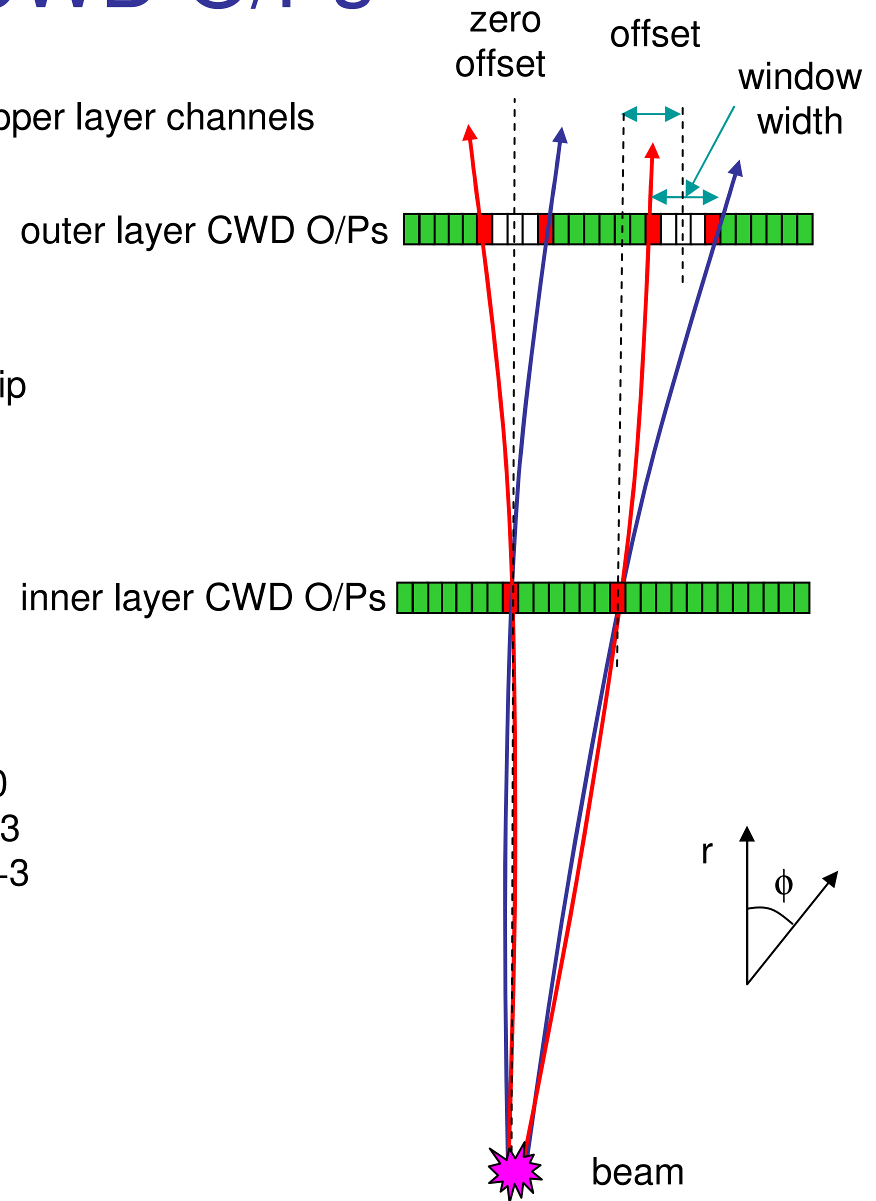
window defines Pt cut
width programmable up to **+/- 8** channels

offset defines lateral displacement of window across chip
programmable up to **+/- 3** channels

=> 11 signals to transmit to neighbouring chip
11 to receive from neighbouring chip

= 22 signals





adding comp O/Ps -> 30 signals altogether, top and bottom of chip