WORKSHOP ON ROC ASIC DESIGN FOR CMS PIXEL EVOLUTION

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Introduction

- Most of the workshop will take place at ‘Sala Castagnoli’ room at University/INFN Torino, v.P.Giuria 1 Torino

- Start Monday morning (10:30-11:00)
- Dinner downtime Monday (and Tuesday?) evening
- Close work on Wednesday afternoon 4-6pm

GOAL of the workshop

- Discuss guide lines / ideas for the new chip
- Discussion / decision on technology
- Define a working model for ASIC design
- Define a 6 months work plan
- Define a brush plan for the full project
- Text for the Pixel upgrade TDR
- To Do list

Agenda Day one

We go through few presentations, in a workshop spirit (lot of questions / interruptions / flexible schedule):

- Future Pixel for CMS - Lino
- 65nm technology and CERN results - Jorgen
- CERN activities and interest on a new Pixel chip - Jorgen
- FNAL activities and interest on new Pixel chip - Gregory
- Torino activities and interest on new Pixel chip - Angelo
- Discussion

Dinner downtime

Agenda Day two

- We need to focus our discussion on points raise on day one or important to start real work
  - Important to make a list of points we want to go through (see later slides)

Dinner downtime (or freetime!)

Agenda day three

- Discuss a collaborative model for a chip design
- Define a Pixel Development Work plan
- Make a To Do List for the next 6 months
- Discuss ideas for first submission
- Attracting new groups ?

- Workshop closes at ~5pm

List of topics for discussion

Topic for discussion: 65 nm

- How many other 65nm chip in next 5-10y will be used in a running HEP experiment ?
- Radiation tollerance for digital / analog
- Analog performance / scaling ?
- T3 isolation available as for 130nm IBM ?
- Costs of 65nm
- When can we start to work with this technology outside CERN ?
- What limitations we have before a design kit distributed by CERN is available ?
- How more difficult than 130nm ?
- Building blocks for a first submission / sharing with on-going work at CERN ?
- Radiation hardness for 10^{16}n(1MeV) /cm^2 ?

Topic for discussion: 130/110 nm

- How small a pixel could be if we choose this technology ?
- What do we gain / what do we loose ?

Topic for discussion: Architectural studies

- What architectures ?
  - Pixel matrix
  - Chip perifery
- How do we diversify from FEI4 evolution in 65nm ?
- How can we share the work ?
- Inside pixel
  - Clock distribution
- Trigger stamp inside pixel: obligatory ?
- Regional approach
- Compatibility with Trigger Selective Readout
- Compatibility with Self triggering
- How much ‘flexibility’ we want on this chip ?

Topic for discussion: implication of trigger support

- Implication of Self triggering
- Implication of Selective readout
- Macro region for self trigger
  - Like local region in pixel matrix or different ?
  - Column ?

Topic for discussion: Analog part

- Inside pixel: ADC / ToT / binary / analog ?
- How to cope with different sensor technologies: pixel 3D, planar, diamonds ? (different capacitance / leakage current)
- Calibration circuit ?
- Limitation to the pixel size: dominant factor ?
- Pixel self-calibration ?
- Achievable a ~1000e- threshold ?
- Can threshold be estimated from simulation

Topic for discussion: Tools needed

- List of needed Common tools for sharing the work
- VERILOG / VHDL
- Simulation tools
- Collaboration platform: SOS design repository as adopted by FEI4 ?

Topic for discussion: chip perifery

Topic for discussion: Planning

- Thoughts for a first prototype
- Possible a 5-year plan ?
- Engineering run: how many ?
- Strategy to reduce probability of needing a further engineering run
- Reducing costs of a development line (shared reticule?)
- Lab tests / with sensors
- Revise planning presented at pixel CDR

Topic for discussion: System aspects

- Back-end compatibility
  - (LP-)GBT like – for HL-LHC
  - TBM like – for Phase 1
- Power distribution

Topic for discussion: technical Specs

- Pixel size: initial Straw man (i.e. 30x100 micron2)
- Radiation tollerance
- Input capacitance range
- In-time Threshold
- Average hit rate
- Max number of continuous triggers
- Trigger latency
- Single chip data output rate
- DC leakage current tolerance
- Power consumption
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- .
- ….