CMS PIXEL UPGRADE

21/05/12 Torino

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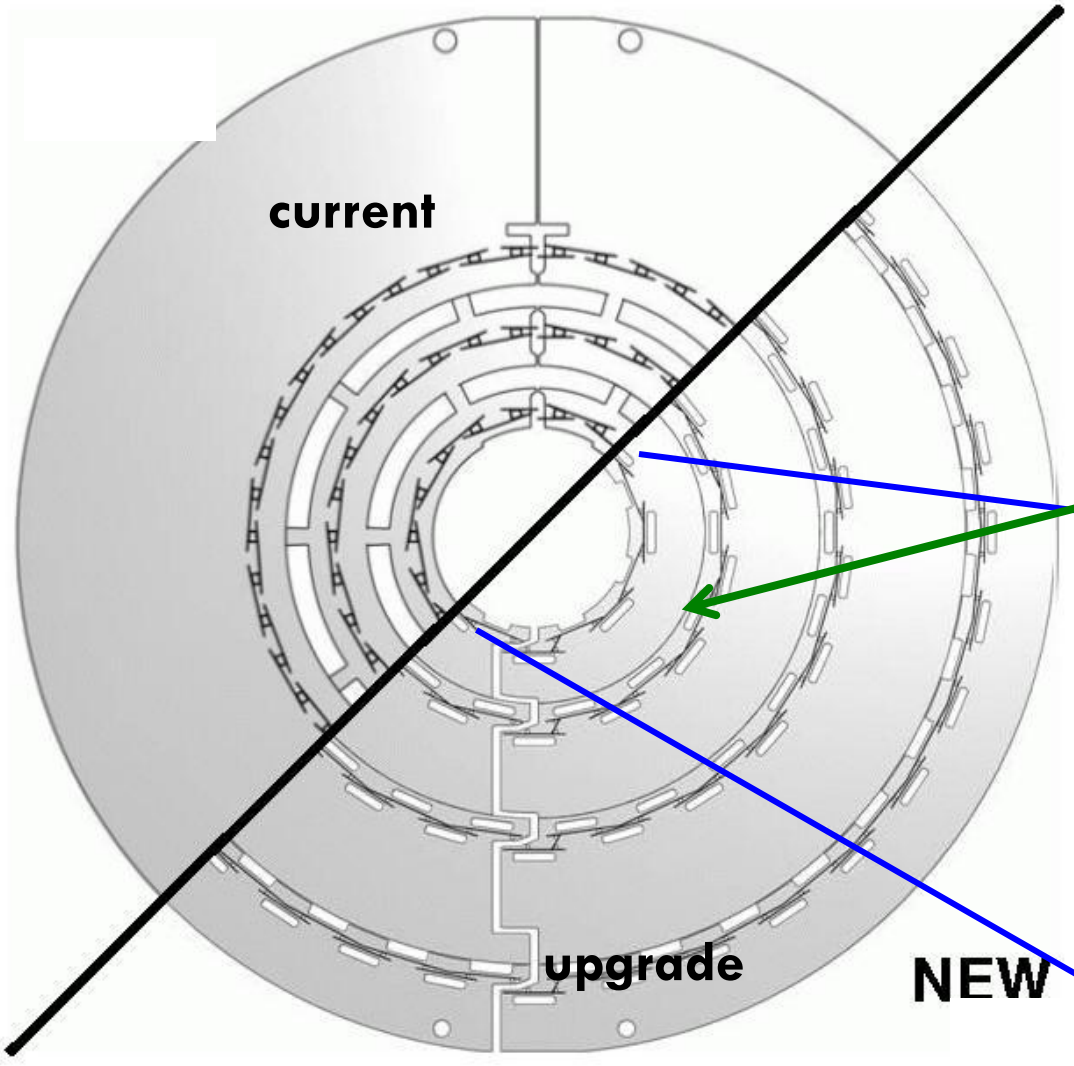
Introduction

- LHC is constantly improving the luminosity and they will always do that as much a possible. Two major upgrades are identified as Phase 1 and Phase 2.

- While Strip Tracker replacement can only be done once in the life of the experiment, Pixel detector replacement will be done more times
  - Building a **new detector** covering **Phase 1** (2016/17) pixel detector
  - Replacing inner layer(s) during Phase 1 (2019)
  - Building a further **new detector for Phase 2** (>2021)

BPIX upgrade for Phase 1

→ **81M pixel** (1.6 x present BPIX)



- **Full module type only**

Layer 1: r = 30mm; 12 faces

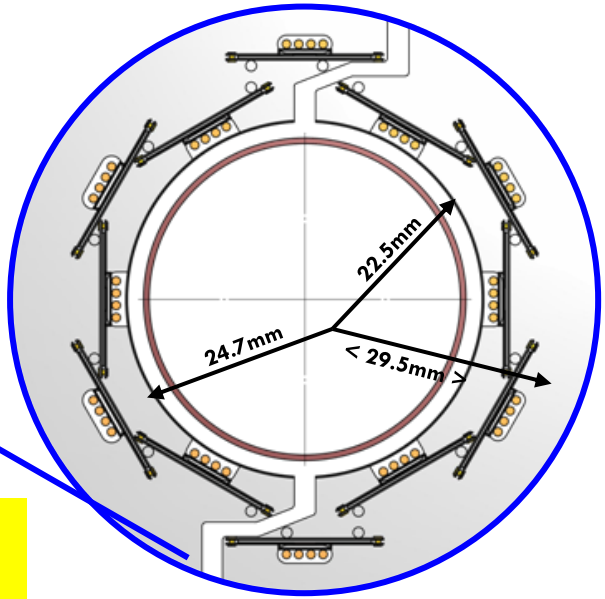
Layer 2: r = 68mm; 28 faces

Layer 3: r = 109mm; 44 faces

Layer 4: r =160mm; 64 faces

fall back with old beam pipe

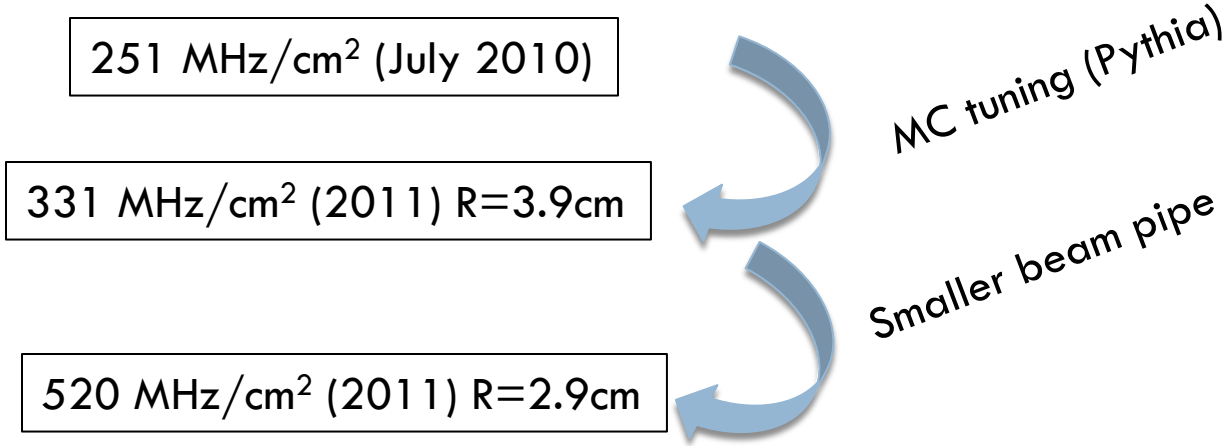
Layer 1: r = 39mm ; 16 faces



INNER LAYER NEED replacement after 250 fb^{-1}

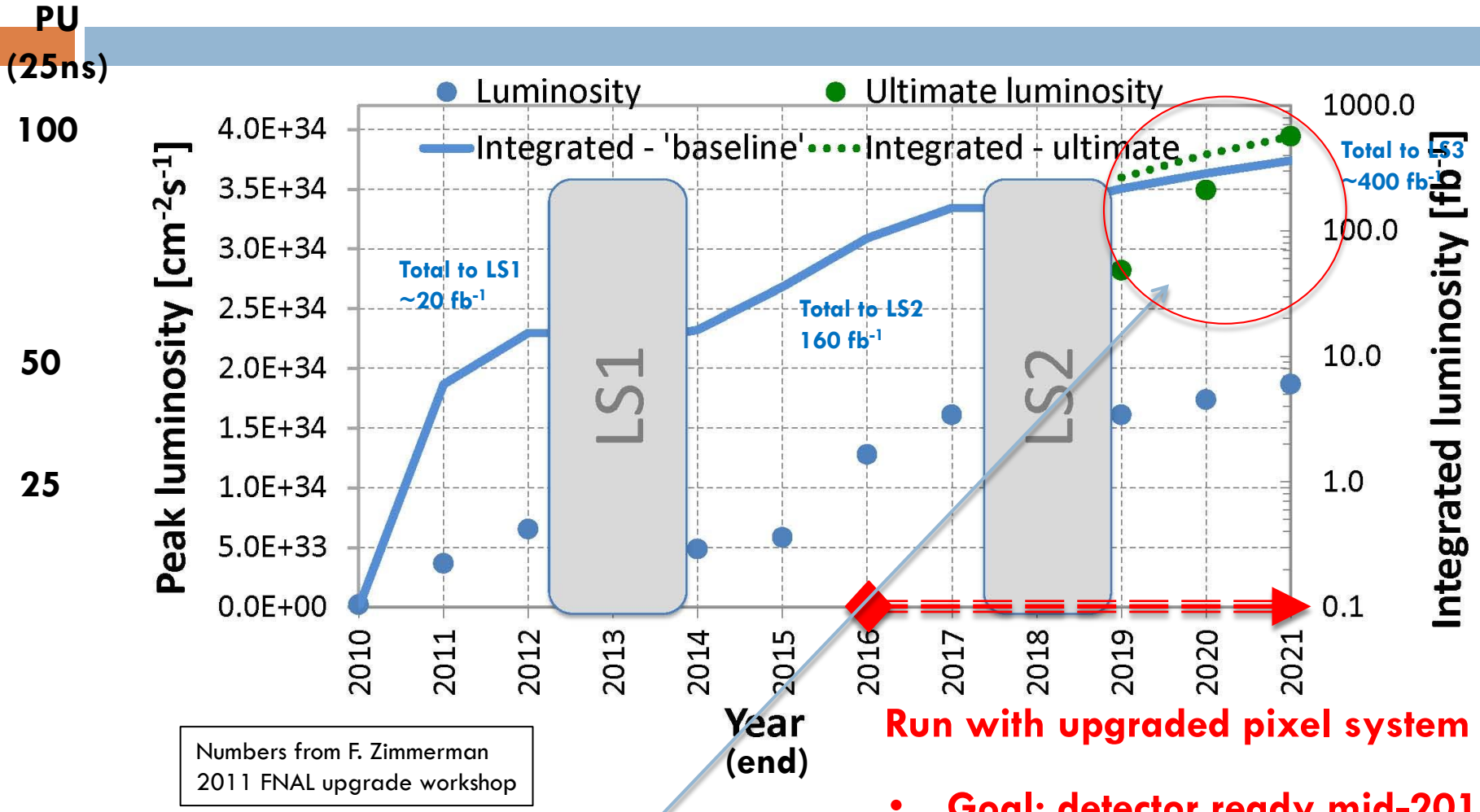
CAN STAND instant Lumi up to 2-2.5 10^{34} $cm^{-2}s^{-1}$

Pixel rates in L1



- PSI46dig_V1 cannot work on L1: too high losses
- PSI46dig_V2 will implement changes in the double column. Not yet clear what are all the interventions needed
  - according to simulation studies can provide 2.5% inefficiency inside the column
  - NOT clear what are the inefficiency in the readout both for 25ns and 50ns scenario for 100 kHz trigger rate (up to 10%?)
  - Losses are increasing exp with instant Luminosity (wall like) and also depends on Trigger Latency

- keep basic functionality for integrated luminosity **>500fb^{-1}** → *operate up to LS3*
- allow a simple Layer 1 replacement after ~200fb^{-1} in extended winter shutdown



Numbers from F. Zimmerman
2011 FNAL upgrade workshop

Run with upgraded pixel system

- **Goal: detector ready mid-2016**
- **5 months to install and commission**

BASELINE LUMI COULD BE EXCEEDED

New generation pixel detector

- Phase 1 pixel is made of present pixel sensors and a modification of present PSI46 chip in VLSI 250nm
- Proposal is to launch the development of a new generation pixel detector
  - New sensors with a much higher radiation tolerance
    - Present sensor needs replacement after 100-200 fb^{-1}; lifetime much dependent on the threshold itself
  - New ROC chip
    - High efficiency at very high Instant luminosity of 5 10^{34} $cm^{-2}s^{-1}$
    - Efficient for L1 trigger @100 kHz and max 6.4 μsec (this define pixel buffering)
    - High radiation tolerance (~10^{16} particles/cm2)
    - Lower threshold <1500 e-
    - Higher granularity (factor at least ~3) ➔ smaller pixels
    - Support for intermediate level trigger (more on line of Phase 2)

Upgrade appointment

- TDR of Phase 1 upgrade under preparation
  - April Conceptual Design Report – done
  - May/June: second draft
  - July: Final Draft
  - August: CMS TRK Ph1 Manag Board
  - Sept: final signoff and presentation to LHCC
- Appendix: Evolution of Phase 1 pixel detector
  - Under work (~40% written)
    - sensor part almost ready
    - New chip part to be written (only my skeleton there)
    - System aspects

From CDR (1)

- The Phase 1 upgrades should operate under these conditions until LS3, which is the long shutdown in which Phase 2 upgrade are installed, including a new tracking system. The date of LS3 is uncertain. It is possible that a total of 500-700 fb-1 will be accumulated by LS3, and the Phase 1 upgrades must survive or be extendable through this period.
- There is a risk that CMS will see high luminosity running before LS3 for an extended period of a few years. It is proposed that an R&D program be described in an appendix of the TDR that targets the critical technology needed for very high luminosity pixel operation. This development will be directed to the Phase 2 upgrade (for which a Technical Proposal is planned in ~2014), and/or to an extension of the Phase 1 upgrade with replacement of inner layer(s) should this be necessary.
- The reviewers endorse this strategy for a baseline replacement of the inner layer, and the description of a ~5 year R&D program targeting sensor and chip technology. The emphasis on 65 nm technology proposed in the review should be justified, and the program should describe R&D for sensors and chip.

From CDR (2)

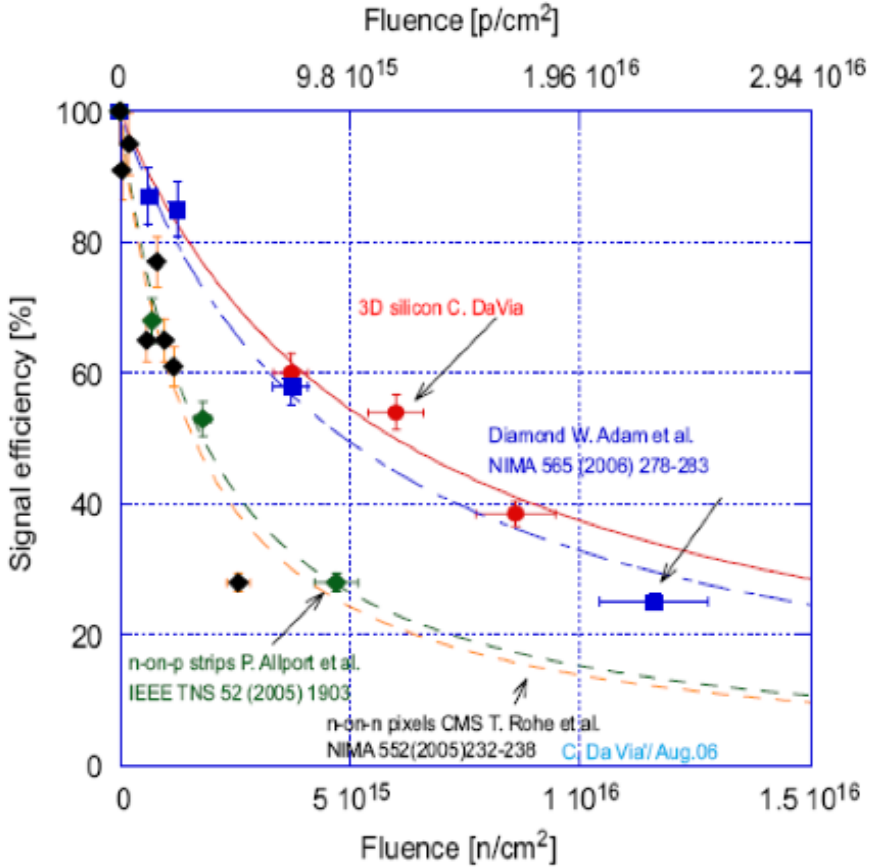
- The requirements for operation at luminosities well above 2E34 likely include smaller pixel size, and a more radiation tolerant sensor technology (thin planar silicon, 3d sensors, diamond detectors). The readout chip will need more processing capability for high bandwidth and to provide selective readout at high frequency for track triggering in Phase 2. Future chips are likely to be submitted in ~130 nm or ~65nm processes. Other projects (Medipix and Atlas) are currently working with 130 nm and looking at 65.
- A set of benchmark criteria should be established and an R&D program described to target these. The criteria should target Phase 2 conditions.
- The program should allow a branch point for replacing the inner layer(s) to extend the life of the Phase 1 detector should this be required.

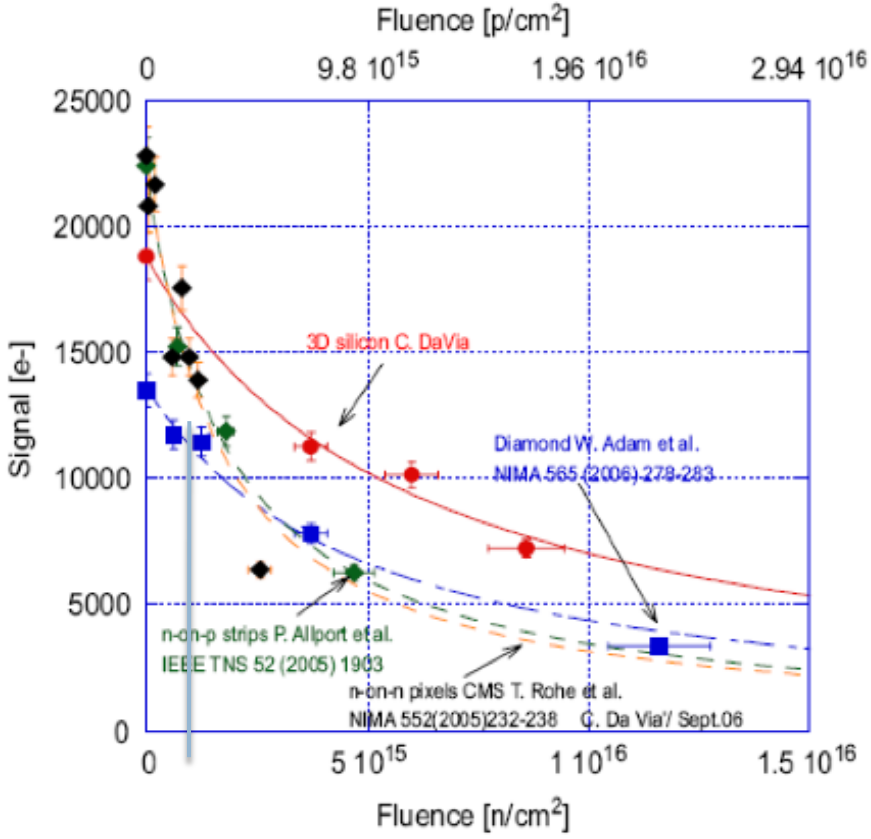
Radiation fluence at 3000 fb^{-1}

- L1 (@2.9cm): ~ 14E15
- L2 (@6.86cm) ~ 7E15
- L3 (@10.9cm) ~ 4E15
- L4 (@16.0cm) ~ 2E15

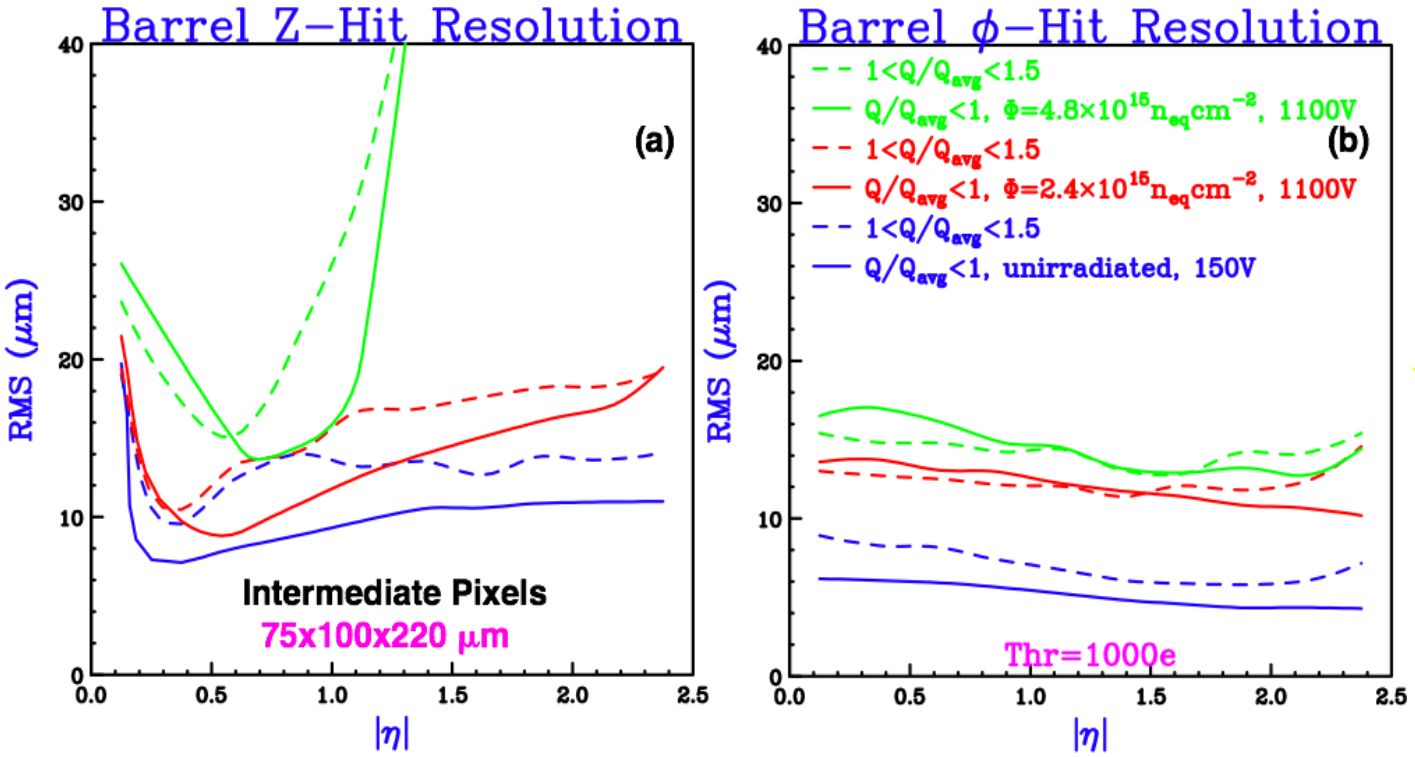
Estimates from leakage current measurements (G.Bolla)

Sensor technologies: radiation hardness





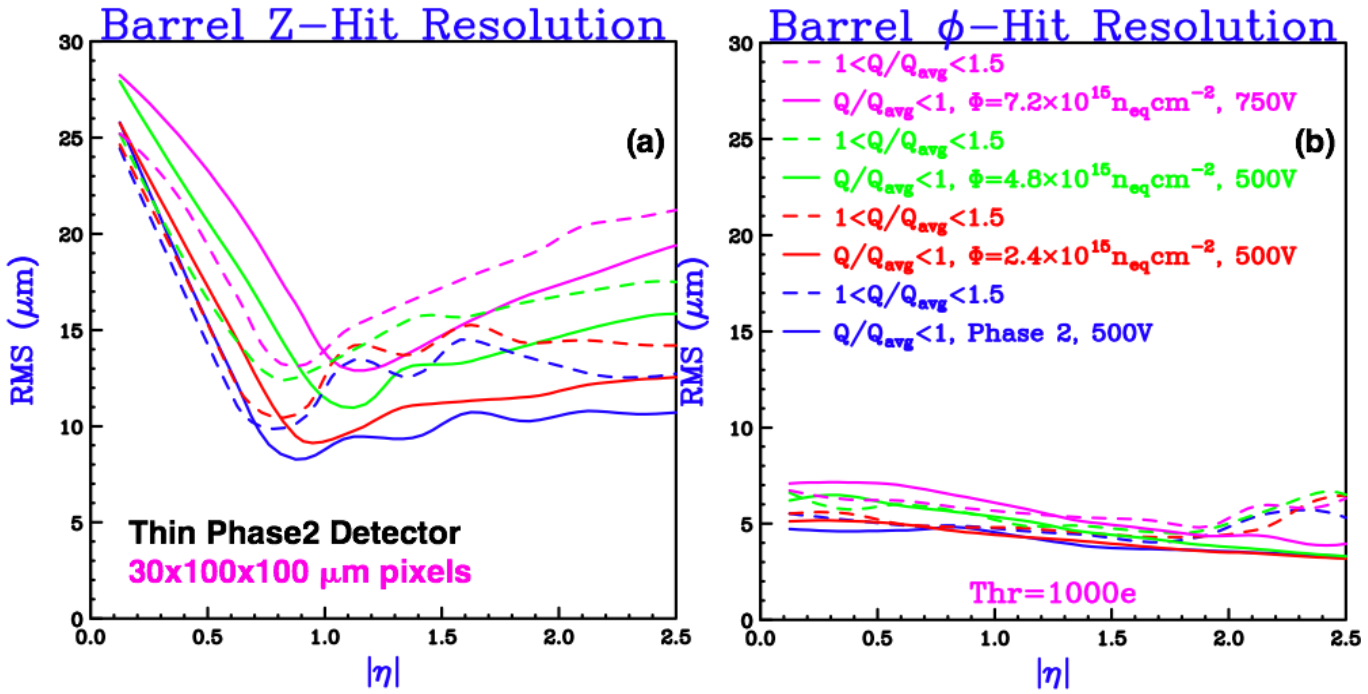
Planar Silicon (study 1)



geometry (75x100x220μm cell) with the 1000e threshold detector would still function at 2.4×10^{15} n_{eq}/cm^2 with a loss of about 50% in resolution. The very poor high-eta global-z resolution seen at 4.8×10^{15} n_{eq}/cm^2 is evidence of cluster breakage.

Swartz Morris

Planar Silicon (study 2)



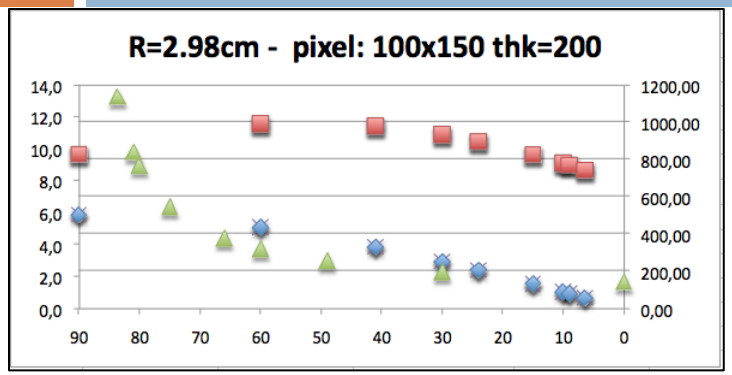
PRELIMINAR?Y

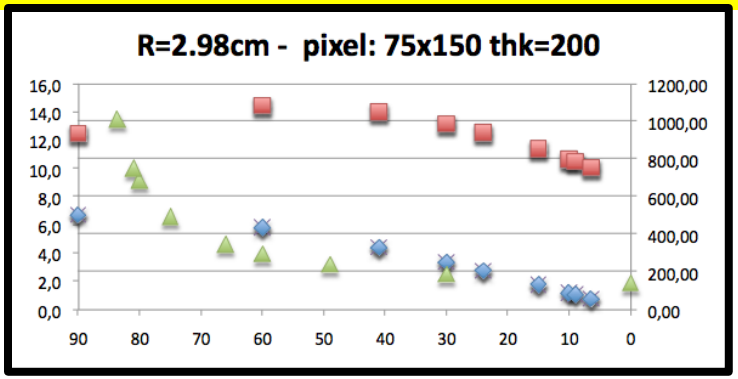
geometry (30x100x100μm cell) with the 1000e threshold The global-z resolution remains "well-behaved" and gradually worsens to about a 50% resolution loss at the largest fluence. Comparing this behavior to the other options, it is clear that shortening the drift paths does retain a larger fraction of the deposited charge. The thin planar detector concept is quite attractive if the threshold of the readout chip is significantly reduced.

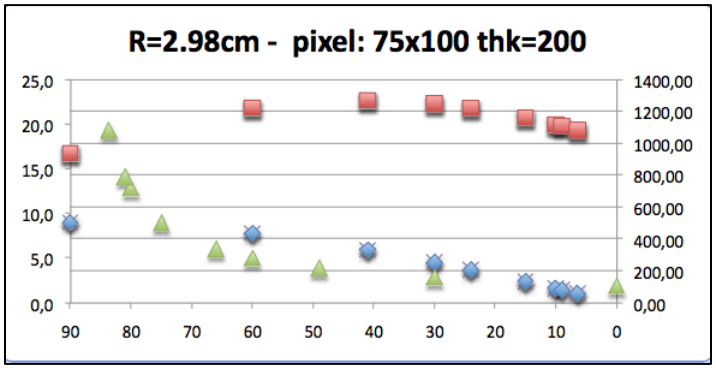
Swartz Morris

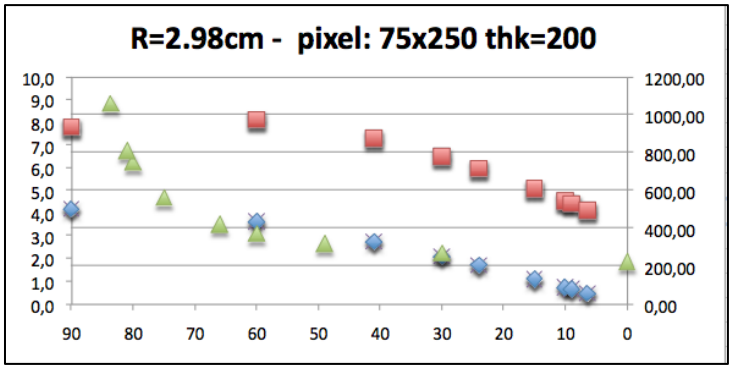
Pixel rate @L=($5x10^{34}$) for different pixel cells –thickness = 200 micron

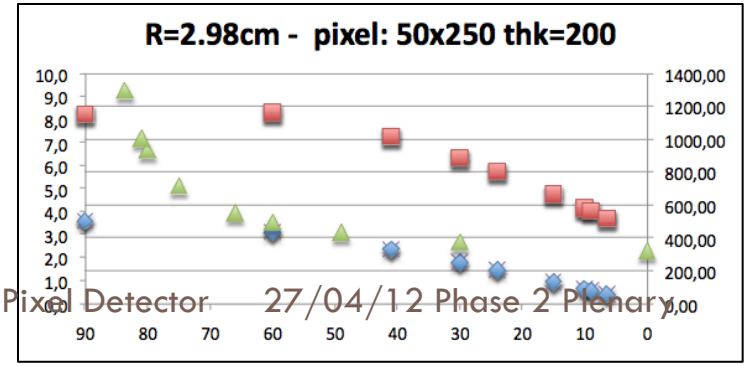
NB: green dots are the cluster size (theta is reversed)







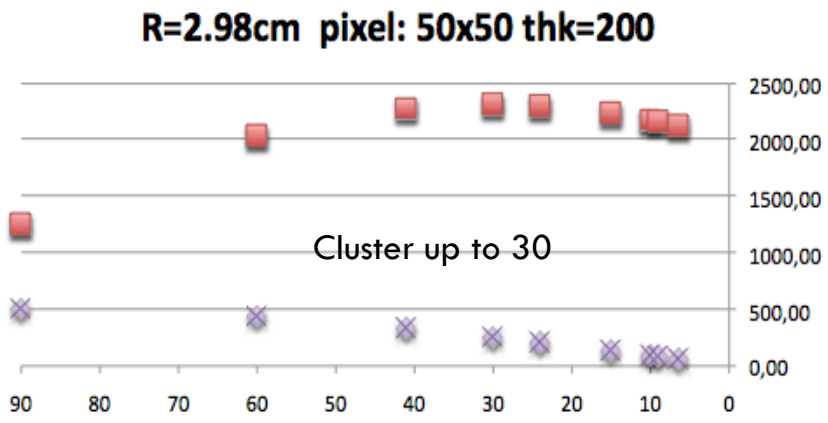


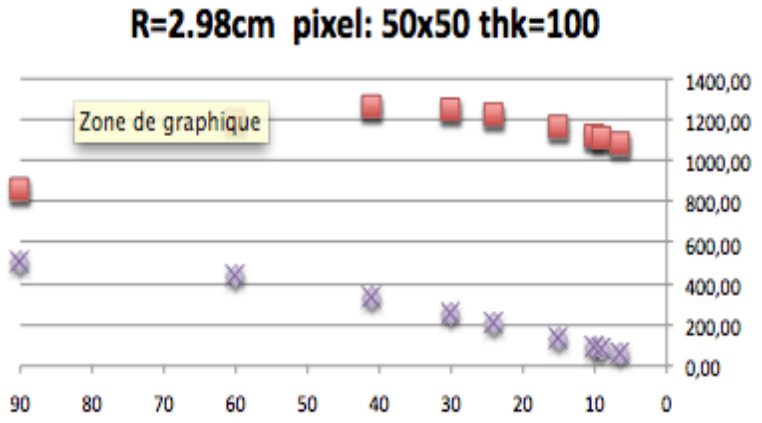


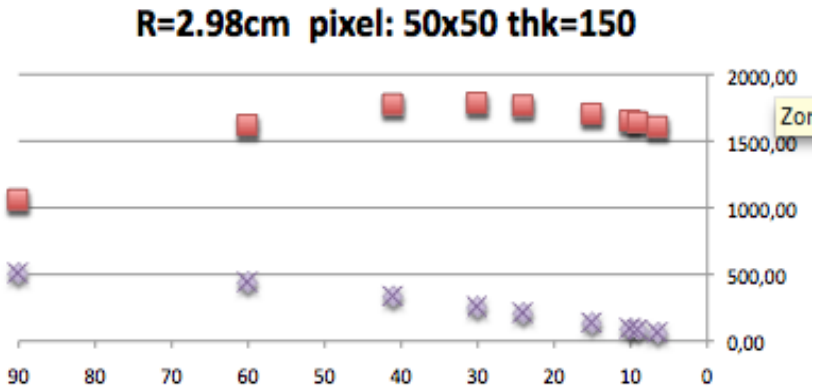
For lower thickness the length in z of the cluster is reduced

Rates goes from 1.0 to 1.2 GHz/cm^2 depending on pixel size

Case Study 1 (50x50)



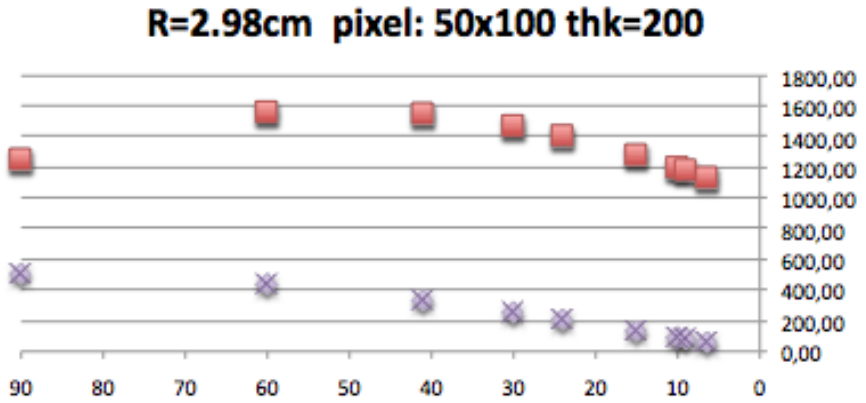


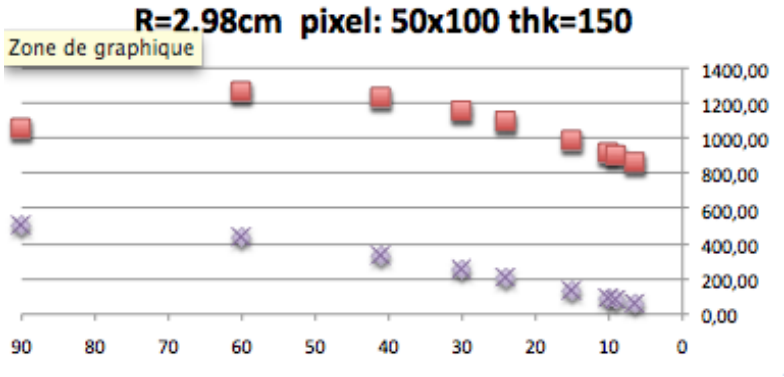


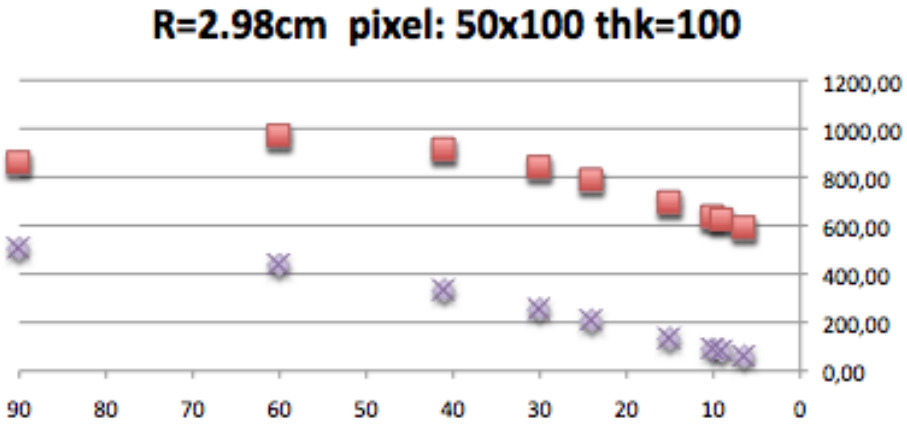
Cluster in Z up to 14

Comment: for planar cluster breakage very high. Should go really thin. In z seems too segmented

Case study 50x100







Technology to use

- Technology to use is under evaluation but strong interest for 65nm (if not 130nm)
- CERN started to use the 65nm and characterize it (one vendor) – logic and mixed-signal/RF circuits
  - No HBD needed (no enclosed transistor) – tested up to 200 Mrad
  - Better TID performance compared to 130nm
  - Work on analog block on-going – no problem seen so far
- CERN is moving to 65nm fast and several projects are going to this technology (Medipix, timepix, LP-GBT and others). Also FEI4 collaboration is moving to 65nm
- We have done in Torino a study with an architecture based on Trigger matching at pixel level and responding to HL-LHC luminosities
  - Preliminary exercise of synthesis on 130nm IBM: digital part take ~70% of the area (if all in one pixel) for a 75x100 micron2

Groups interested to ASIC development

- INFN
  - Torino started
  - Perugia
- FNAL
  - Interested to chip development
- Potentially CERN
  - Interested to development on 65nm
- Potentially Karlsruhe
- Potentially PSI (but later)

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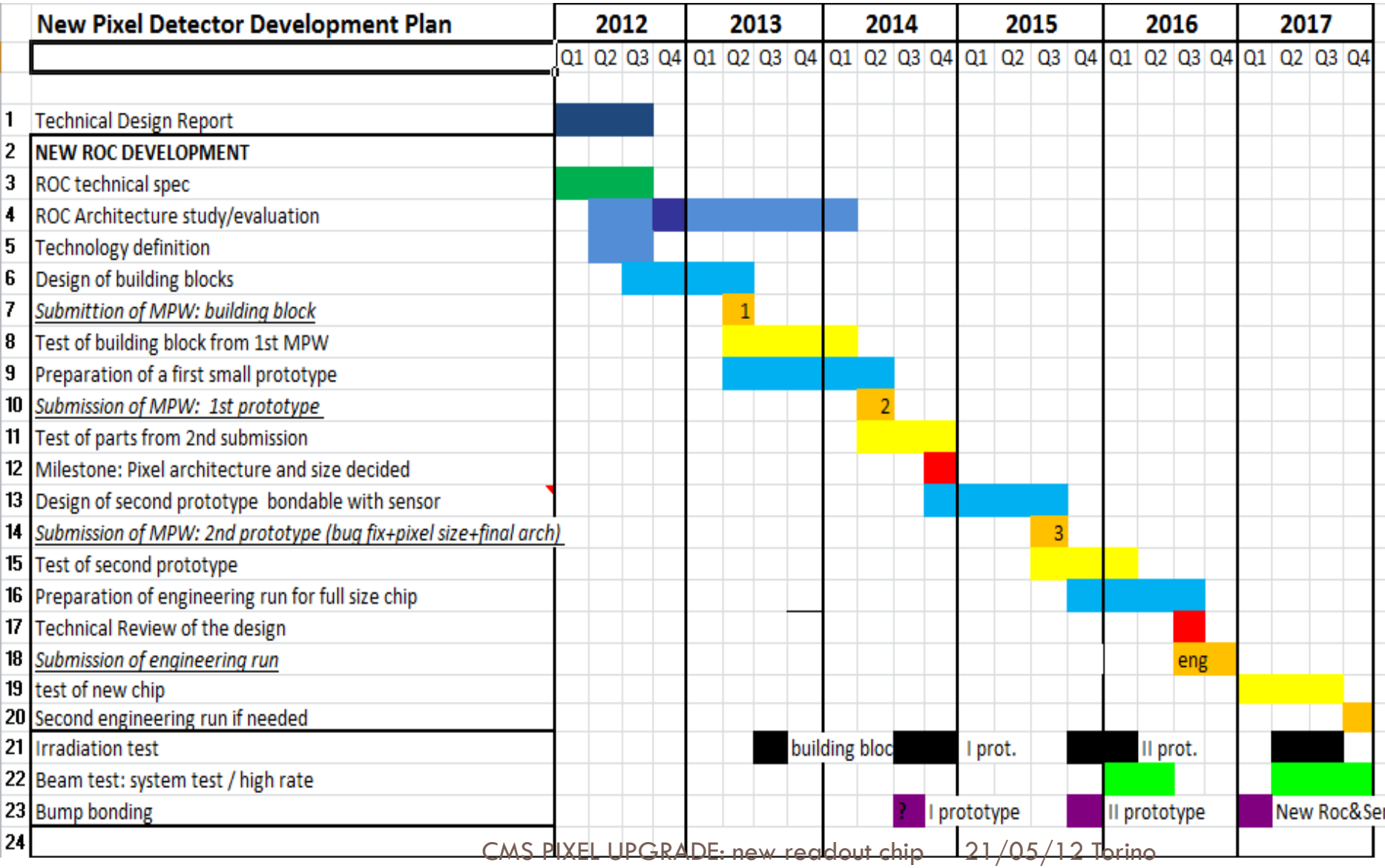
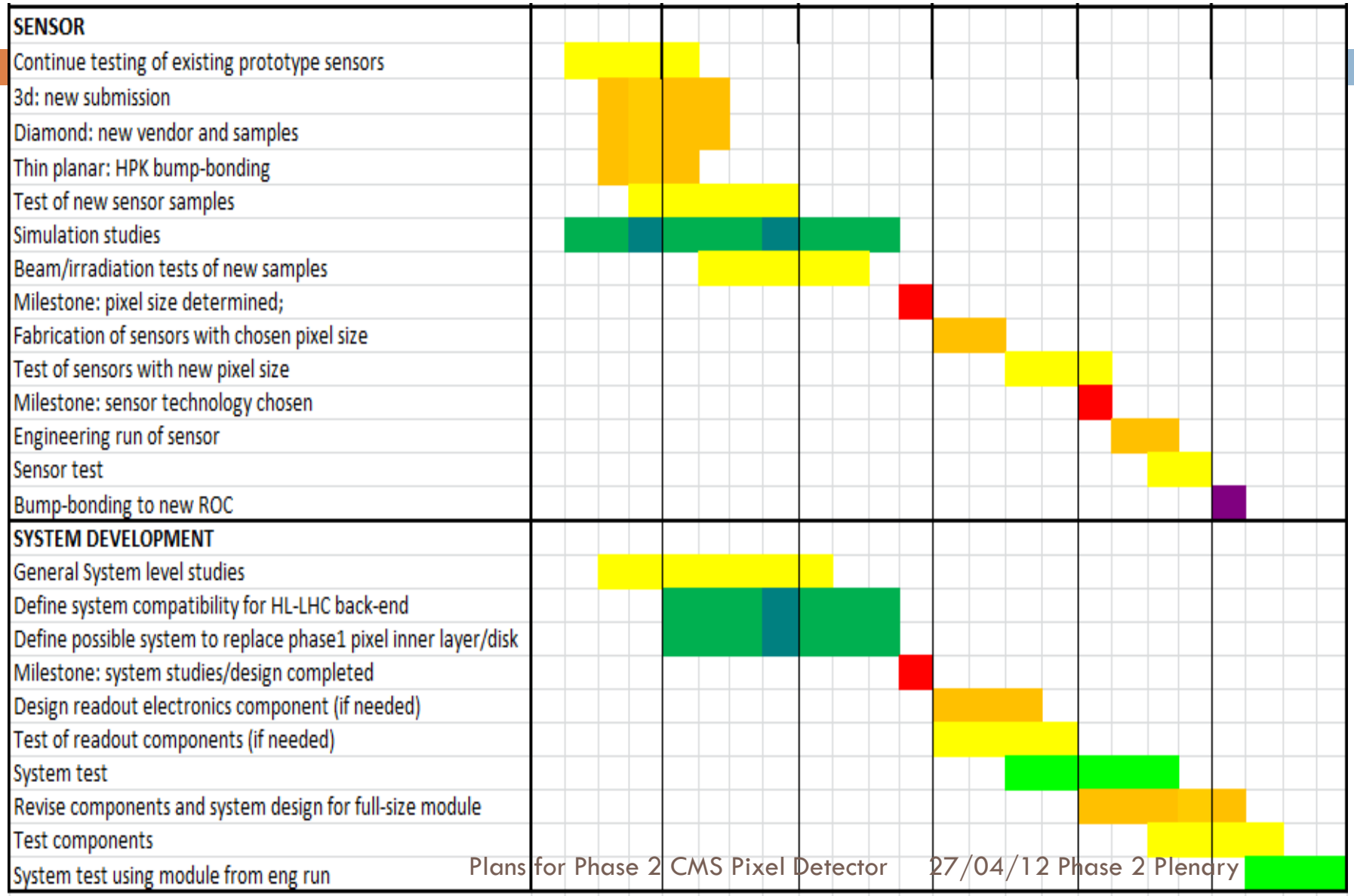
ROC -5 year Development Plan



Sensor & System 5- year Development Plan



Conclusion

- The phase 1 pixel detector will work well for a luminosity of $2x10^{34}$. With the further increase in luminosity as projected, we will need to have a serious and focused effort to develop a new pixel system.
- Good time to start a **completely new pixel chip**, optimizing the segmentation, the signal size, and the type of sensor to use
- Concurrently, continue the effort on sensor development as well as evaluate system architecture
- The project has its goals to address the challenges of Phase 2, but if the development is progressing well enough, there could be an opportunity to replace L1 between LS2 and LS3 using this new pixel system.
- Essential to form a strong collaboration of groups with experience on ASIC design