# A HL-LHC CMS PIXEL DETECTOR ASIC IN 65NM TECHNOLOGY

**Jorgen Christiansen CERN/PH-ESE**

1

# DRIVING PIXEL ASIC REQUIREMENTS

- Pixel size
  - Driven by physics and **what can be made by technology.**
- Connection to detector.
  - Bump bonding, Thinning, Polarity, Collected charge, etc.
- Analog performance
  - Thresholds, Noise, ADC/TOT, etc.
- Data (hit) rate, data buffering and triggering
  - Pixel trigger with ROI ?.
- Multiple modes: Triggered, Trigger less, Self triggered, Test, Calibration, etc.
  - This is what technology can "buy" us with "intelligent pixels". (if we do not want too small pixels)
- Low power
- Radiation tolerance (Dose, Neutrons, Hadrons, SEU)
- Readout
- Control
- System (hybrid) integration

# WHAT WE CAN GET FROM 65NM

- Radiation tolerance (dose, hadrons, SEU):
  - TID has now been well demonstrated
  - SEU to be handled with redundant logic

- Large amount of digital logic/memory:
  - Vital for small pixels, high date rates, buffering, flexibility.
  - Logic density: 250nm: 1, 130nm: ~4x, 65nm: ~16x
  - Speed: 250nm: ~1, 130nm: ~2x, 65nm: ~4x
    (Where high speed not needed one can get lower power by running at lower $V_{dd}$)

- Low power (digital):
  - Low supply voltage: $P \sim V_{dd}^2$
  - Multiple low power libraries ($V_{dd}$, High $V_t$, )
  - 250nm: 1, 130nm: ½ - ¼, 65nm: 1/8 - 1/16

- Many metal (cu) layers:
  - Power distribution, Signal distribution, Pixel readout busses, etc.



NMOS Vt shift

NMOS leakage
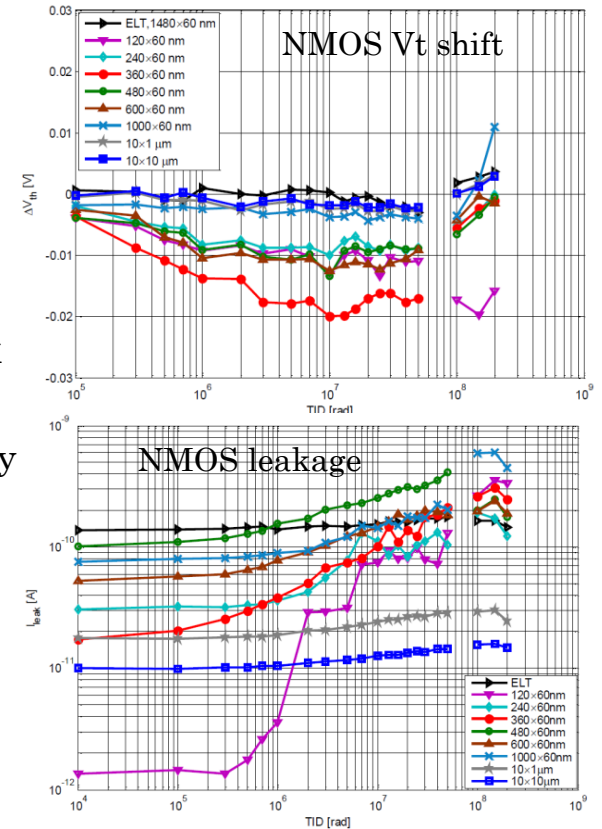
S. Bonacini, P. Valerio CERN
TWEPP2011

3

# 65nm CMOS technology

- Mature technology (~10 years), available and very well known technology with good technology support (tools, libraries, IPs, MPW, production). Known as a strong technology node that will be available many more years (automotive, industrial , ,)
  - High yield, accurate simulation models , , ,
  - Not an "exotic" 3D technology: Availability, Density, Yield , Design tools,
  - Coarse TSV's can be used at periphery if available and appropriate.
- Analog
  - Good low noise and low power amplifiers can be made for pixels (small dynamic range, limited linearity)
  - Triple well deep implant to isolate critical analog parts from digital within pixel cells (have shown very good results in 130nm)
- But we also get:
  - High NRE costs ( ~2 x 130nm for 4x higher density and ½- ¼ power)
  - Lower supply voltage (but this is what gives low power)
    - Critical power distribution architecture (Local DC-DC or serial powering)
  - Higher gate and transistor leakage: Can be handled with appropriate design approaches
- Pixel detectors are our IC technology drivers
- 65nm technology access, MPW runs, tools, radiation qualification, etc. via CERN and Europractice.

4

# HOW COULD A 65NM PIXEL ASIC LOOK LIKE

- ~50 um x ~50um Pixels ( 30 um x 70um ~same area)
  or 25x50um, but most likely not 25x25um (LCD/CLIC but low rate)
  - How small pixels are advantageous in high rate LHC environment ?.
    - Resolution limited by multiple scattering in beam pipe and pixel detector itself.
    - **Low power pixel ASIC critical** !
  - Small pixels: Consider binary readout (50um/$\sqrt{12}$ = ~14um, 25um /$\sqrt{12}$= ~7um)
  - "Large pixels": Use of ADC/TOT for interpolation
    - Large pixels allow extended buffering and flexibility
    - Also feasible in a 50x50um pixel cell if appropriate architecture.
- Pixel array size: > 20 x 20 mm (>200k pixels):
  - Limited by reticle size ( max 24 x 36 mm)
  - Not considering possible stitching ( Yield, cost, access , ,)
- ~2GHz hits/cm$^2$ (~500MHz/cm$^2$ track rate and cluster size = ~4)
  - ~50kHz hit rate per pixel -> no fast shaping needed, low power
  - Digital corrections for analog imperfections ( e.g. threshold variation, time walk)
- Modes: Triggered/Trigger less, TOT/Binary, Testing modes, ,
  - Trigger: Latency <25us (B-ID width: ~10bit) , Rate <1MHz (readout limited) (not both at same time as limited by buffering)
- "In-pixel" digital storage and processing (vital for high rate)

5

# 65NM PIXEL

- Analog FE + adjust DAC's: <~½ of 50x50 um pixel
  - First FE/DAC prototypes have been demonstrated (LCD-CERN, ATLAS-LBNL)
  - ~4 bit TOT amplitude measurement
    - TOT with basic master clock (40MHz)
      - Dead time loss: 50khz * 16(max)*25ns = 2% (average ~0.5%)
      - Shorter dead-time using time interpolation in pixels required
    - Or low power ADC (Turin) or Binary
- Remaining ~½. Single pixel can contain the following digital:
  - 1/3: Flip-flops/registers (1.8 x 3.8um) = ~45
  - 1/3 logic: NAND4 (1.8 x 1.4um) = ~125,
  - 1/3 SRAM (1.05 x 0.5um) = ~600 (in practice much less for small memory)

  (assuming 75% area utilization)

  (forgetting about area penalty to separate analog and digital)

  Marginal to implement buffering, logic, multiple modes, SEU protection, etc.

Local Pixel Regions (PR, or super pixels or , ,)  to optimize local clustering and enable efficient local digital processing.
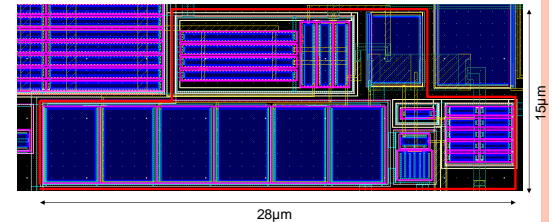


Preamplifier
P. Valerio CERN/LCD
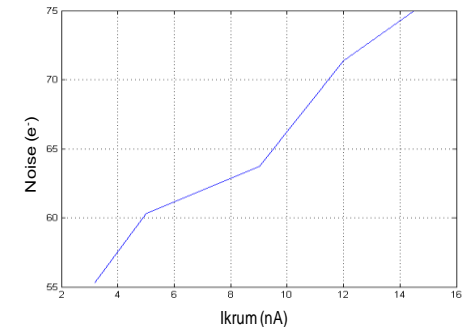
# 65NM PIXEL

- High density internal column data "busses" to get data out of pixel array.
- End of column date merging, checking, formatting for readout.
- High speed serial link for readout
  - 5-10 pixel chips feeding one (LP)GBT with local ~320Mbits/s serial links in high rate regions.
  - A (LP)GTB can collect date from up to 40 pixel chips in low rate regions.
- Full SEU protection on critical parts
  - Clear identification of critical and non critical parts vital
- Power density: ½ - 1 W/cm$^2$
  - Major design goal determining material for services (power, cooling)
- Design complexity will come from low power complex digital and low power, low noise analog
- Potential pixel trigger will have a significant impact on the digital architecture.
  - Required buffering and logic can clearly be included in a 65nm chip
  - System aspects critical (e.g. protocol, bandwidth, links)

# PIXEL REGION OPTIMIZATION

- Grouping pixels in regions is critical to have enough local pixel area for efficient buffering, logic, routing, low power features, different operating modes, , ,

- HEP pixel hits are naturally clustered
    - Cluster sizes: 1 – ~9 (3x3), Average ~4 (just an example)
      Strong dependence on pixel size, Si detector, radiation damage, track angle, detector angle, Lorentz angle from magnetic field, , .
    - Local clustering enables data reduction ("compression")

- Initial assumption: Central hit with max +1 periphery
    - "Arbitrary" distribution with Average = ~4.22
    - Elongated clusters to be looked at in more detail.
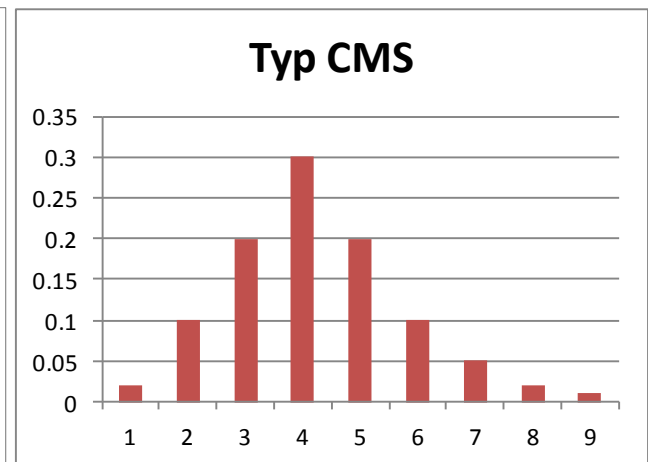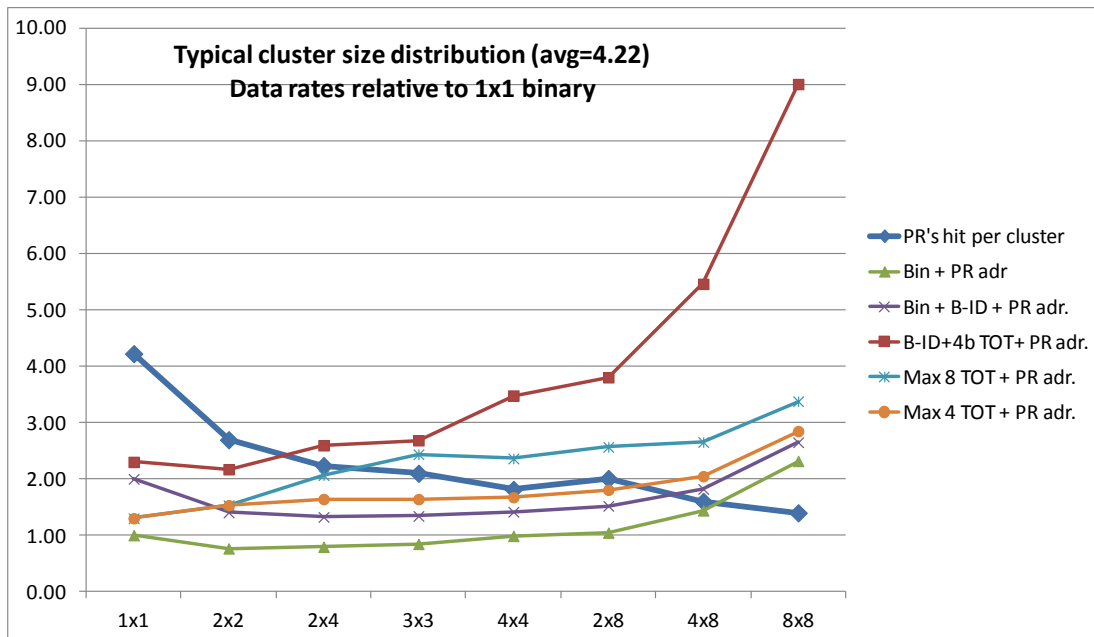      (Track angle, Lorentz angle)
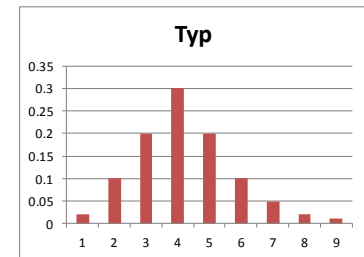
- Pixel Regions (PR):
    - PR = 1 x 1: ~422%
    - **PR = 2 x 2: ~260% (ATLAS FEI4)**
    - **PR = 2 x 4: ~220%**
    - PR = 3 x 3: ~206%
    - PR = 2 x 8: ~200%
    - **PR = 4 x 4: ~180%**
    - PR = 4 x 8: ~160%
    - PR = 8 x 8: ~140%
    - What about required data bandwidth ?
        - Data format for PR has a major impact.



8
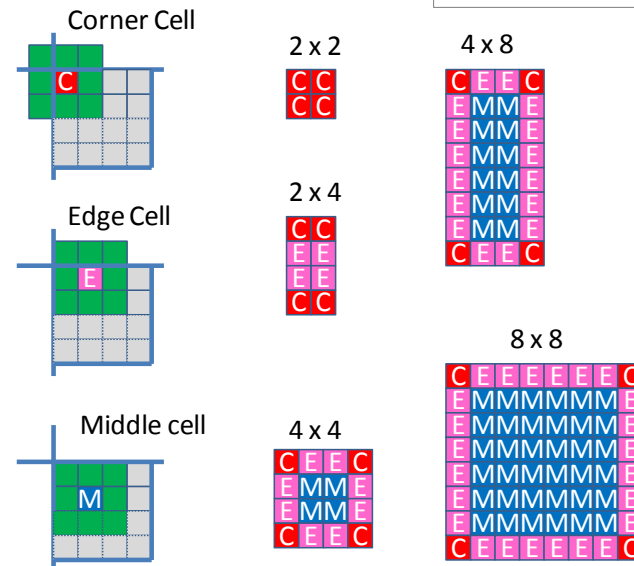
# PIXEL REGION OPTIMIZATION

- "Typical current CMS distribution": Average = 4.22
- PR's having data per cluster (particle)
- Readout data: relative to 1 x 1 binary
  - Binary hit map + pixel address
  - B-ID + Binary hit map + pixel address
  - B-ID + 4b TOT for all pixels + pixel address
  - Binary hit map + 4 pixels with TOT + pixel address
  - Binary hit map + 8 pixels with TOT + pixel address
  - (Variable TOT per pixel region. Framing overhead)



Typical cluster size distribution (avg=4.22)
Data rates relative to 1x1 binary

Legend: PR's hit per cluster, Bin + PR adr, Bin + B-ID + PR adr., B-ID+4b TOT+ PR adr., Max 8 TOT + PR adr., Max 4 TOT + PR adr.

Typ CMS

# Dependence on cluster size
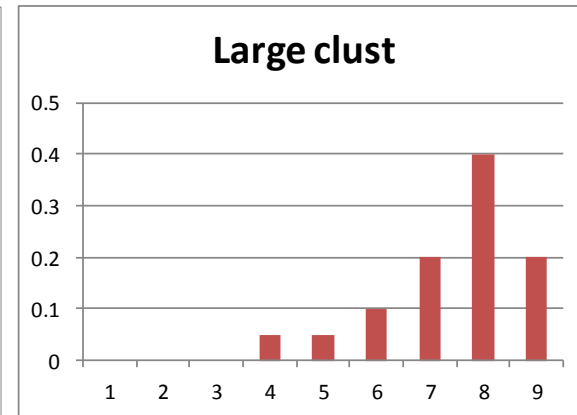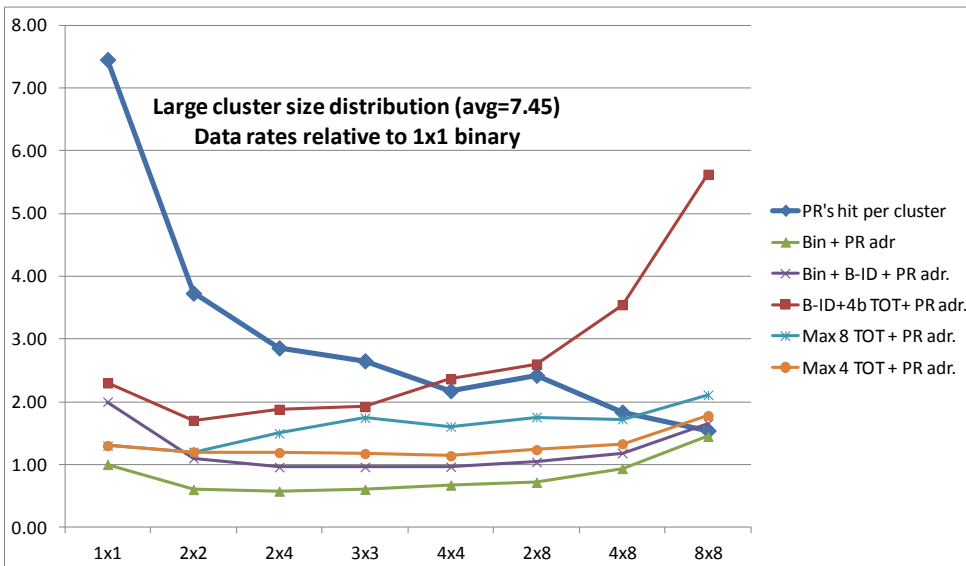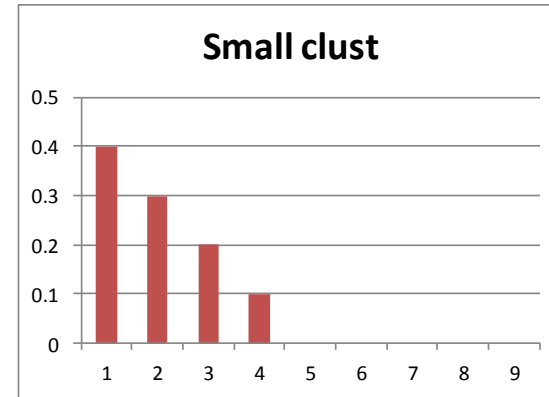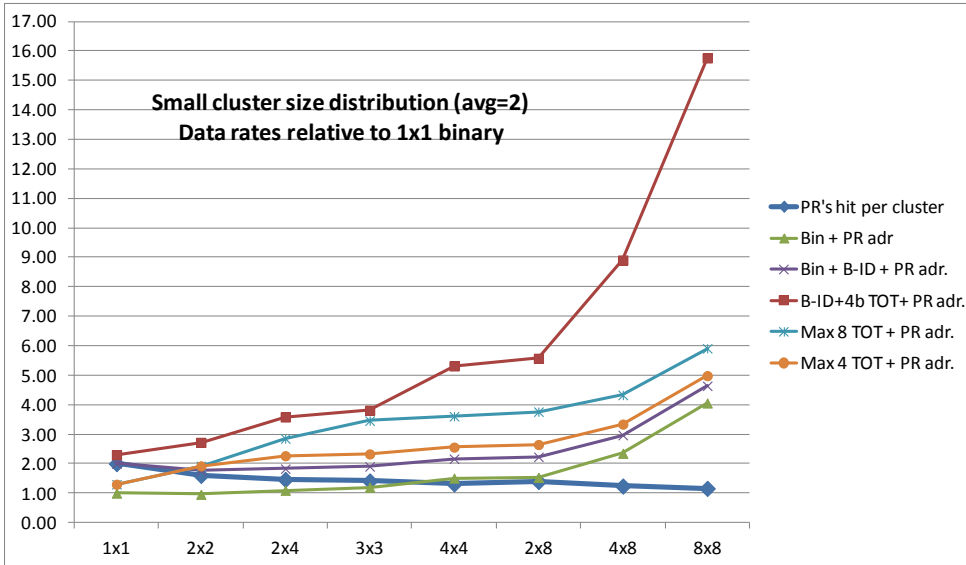
# PR OPTIMIZATION FOR MEMORY/LATENCY UNITS

- When using pixel regions less buffers are needed for L1 latency (6.4us, 500MHz/cm$^2$ track rate).
  - Each buffer is though a bit wider

A. Hits from same cluster can share B-ID information

B. For a given maximum loss rate (e.g. 10e-4) one deep buffer is much more efficient than small individual buffers



Required latency units in 4 x 4 area to have loss below 10e-4 (area)

- 16 * (1 x 1)
- 4 * (2 x 2)
- 1 * (4 x 4)

~2GHz/cm$^2$ hit rate



Cluster size = 4.22

- 4x4 1-sum
- 2x2 1-sum
- 1pixel 1-sum
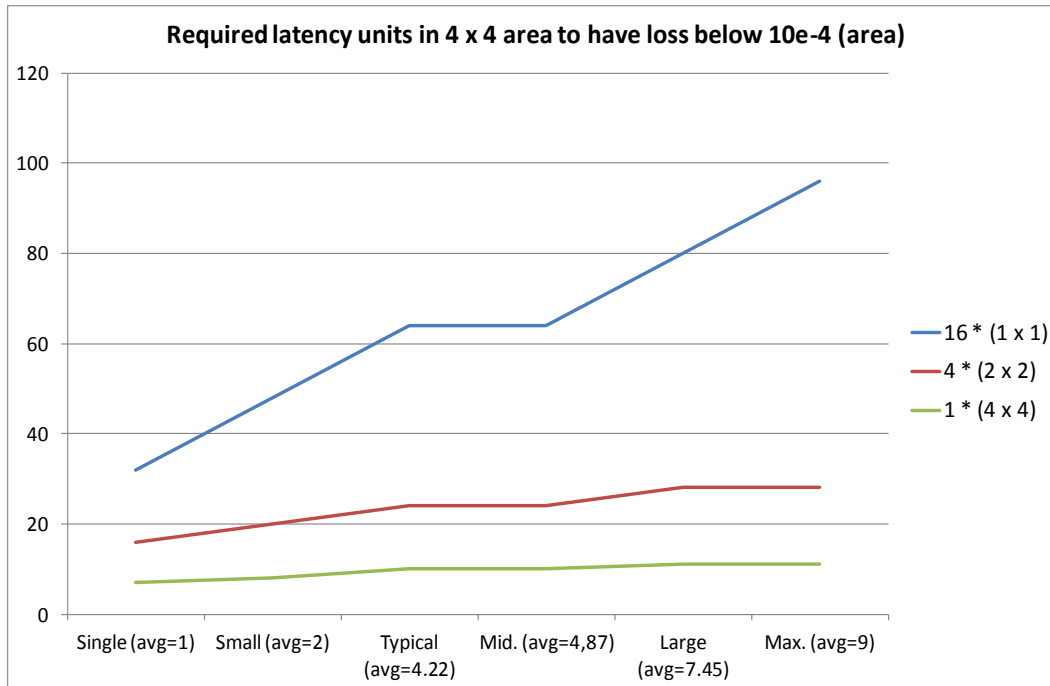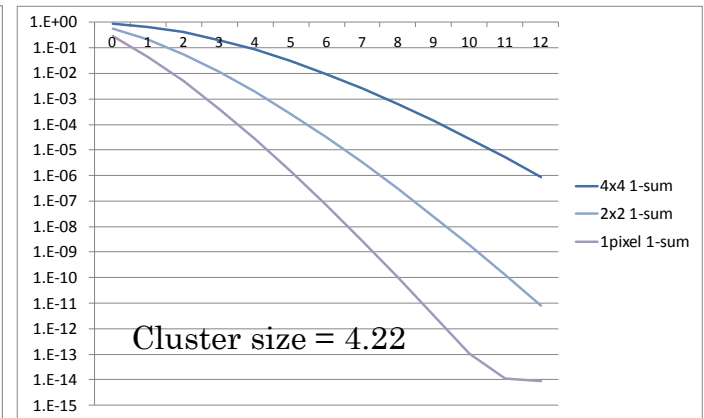
Probability for buffer overflow

11

# PR OPTIMIZATION FOR POWER CONSUMPTION

- Less buffers means less power (static)
- Less active "latency/buffer units" means less power (dynamic)

**Active latency units (power)**

500MHz/cm² track rate
16 pixels

Legend:
- 16 * (1 x 1)
- 4 * (2 x 2)
- 1 * (4 x 4)

X-axis: Single (avg=1), Small (avg=2), Typical (avg=4.22), Mid. (avg=4,87), Large (avg=7.45), Max. (avg=9)

~2GHz/cm² hit rate

Cluster size = 4.22

Legend:
- 4x4 Probability
- 2x2 Probability
- 1 pixel probability

Buffer occupancy probability

12
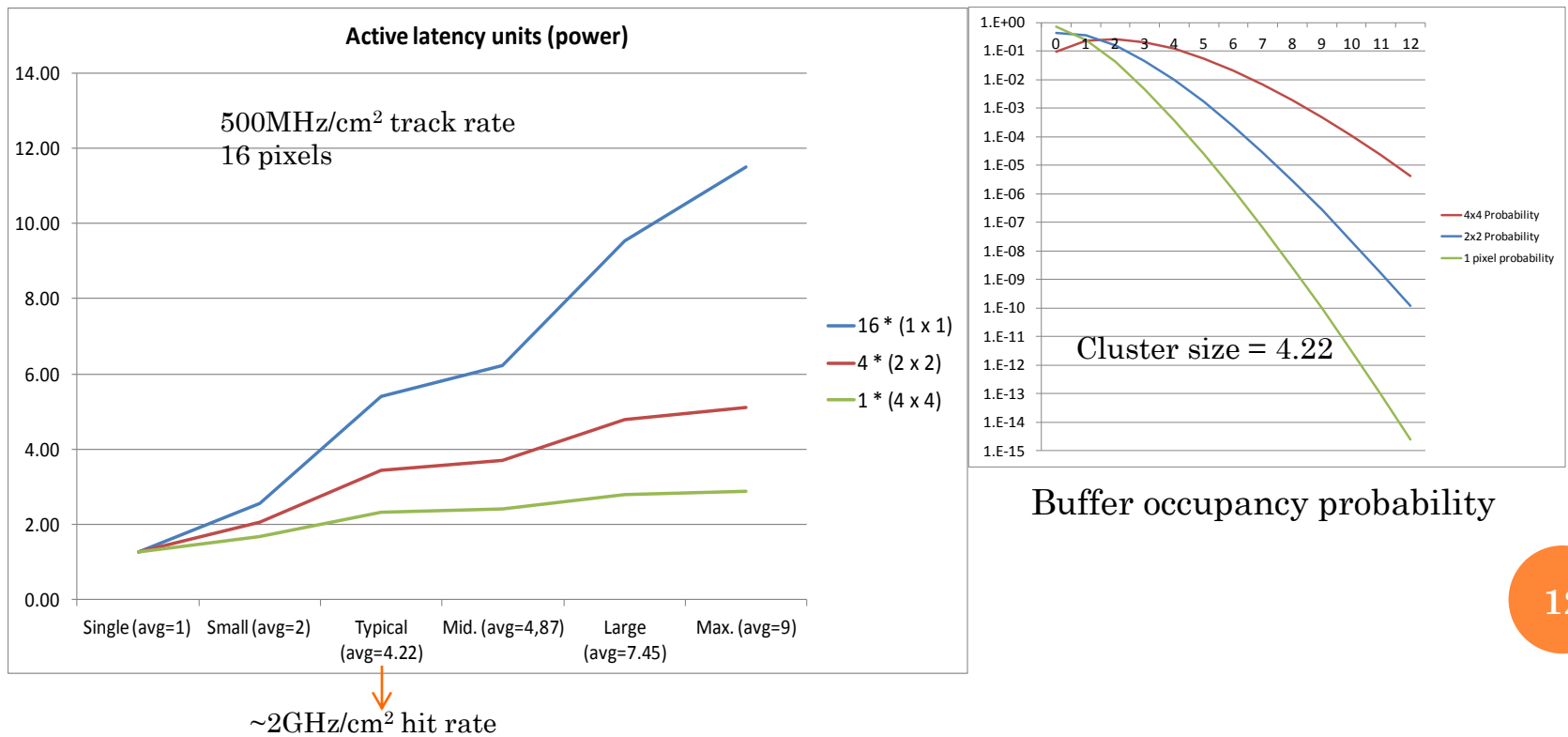
# PIXEL REGION OPTIMIZATION

- Pixel Regions of 4 x 4 seems like an initial good compromise.
  - Get sufficient Digital resources in each pixel region
    - ~½ for analog and required adjustment DAC's
    - ~½ for synthesized digital (75% utilization):
      1/3 registers (~720), 1/3 logic (~2000 NAN4), 1/3 SRAM (<10Kbit)
      **Now we can have quite sophisticated local pixel processing/storage !.**
  - Reduced buffering required
  - Reduced static and dynamic power (still to estimate total power reduction from this)
  - Do not carry superfluous data in readout
- Architecture should not be too highly optimized for a particular detector configuration, clustering, etc.
  - Use technology to build a pixel architecture that is flexible, high rate performance and low power.
  - Initial assumptions may not be correct.

But how to organize a mixed signal floor plan for 4x4 ?

# PIXEL REGION 4 X 4

- Maximize effective area for digital
  - Use of automated synthesis and P&R
- Analog low noise islands
  - Shielded minimum length low capacitance connections to bump pads.
  - Analog power
  - Common biases distribution
  - Minimize cross talk from digital
  - Substrate isolation with deep implant
- Surround analog islands with quiet logic (configuration, etc.)
- Organize digital:
  - Pixel hit processing (TOT) and merging
  - Buffering
  - Column bus interface
- Critical shielding of digital noise to sensor, bump pad and line to bump bad.
- Global routing optimization: Analog Power, Analog biases, digital power, timing control, configuration, readout, etc. ,



14

Pixel pad    analog    Quite digital Config. etc.    Active digital    Power + Analog bias    Readout    Timing, control
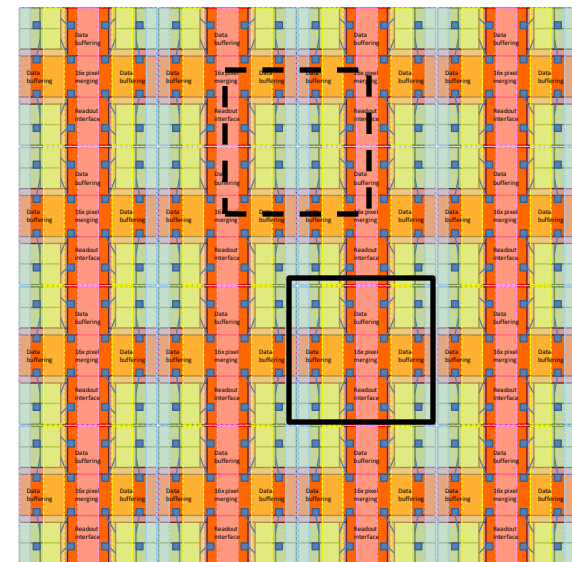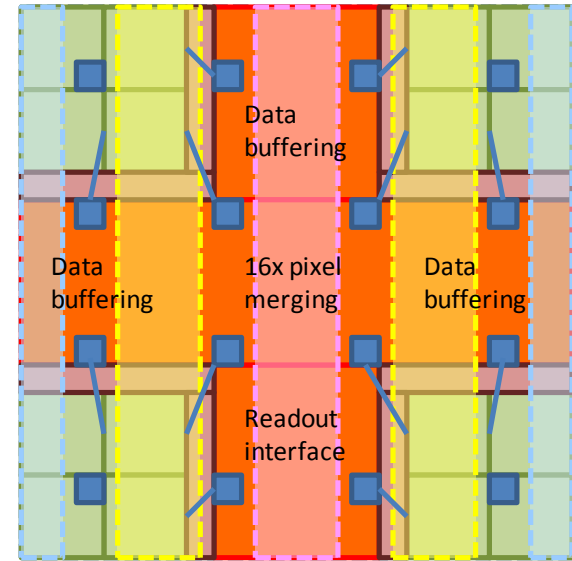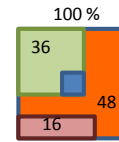
# PIXEL REGION 4 X 4



- Analog "stripes"
  - Good for distribution of analog references and analog power
  - Minimize crosstalk
- Digital "stripes"
  - Good for distribution of timing signals, column busses and digital power.
  - One regular digital zone for P&R digital
- Baseline for LHCb Velo pixel to be implemented in 130nm
  - High rate, trigger less

| ■ Pixel pad | ■ analog | ■ Quite digital Config, etc. | ■ Active digital | ⬚ Power + Analog bias | ⬚ Readout | ⬚ Timing, control |
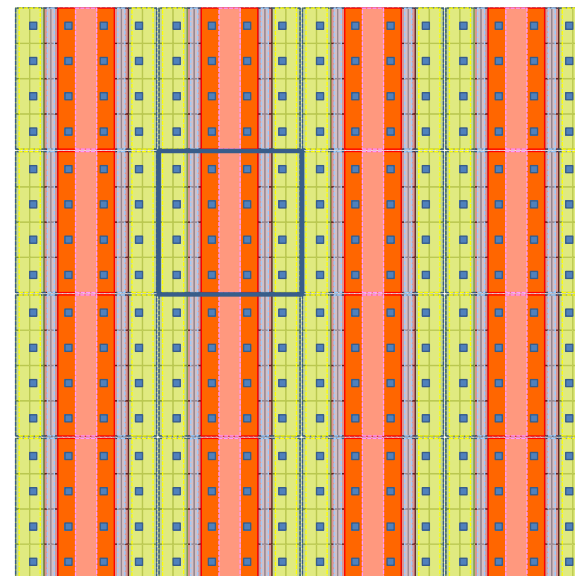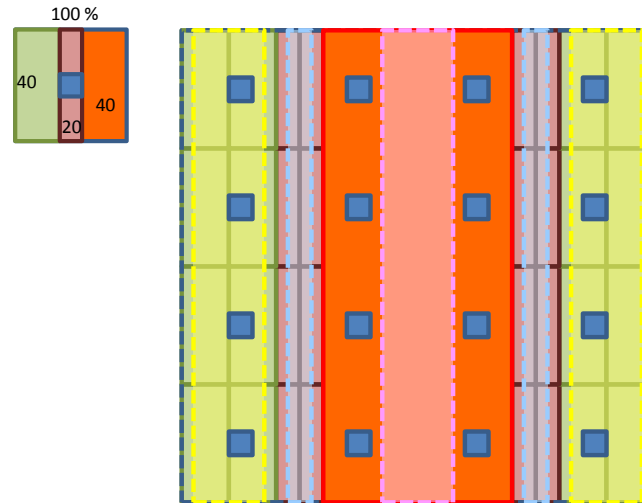
# Pixel region 2 x 4

- Also an appropriate Pixel Region organization from point of view of cluster information and mixed signal layout.

- Enough area for flexible digital + buffering ?

100 %

40  |  40
20
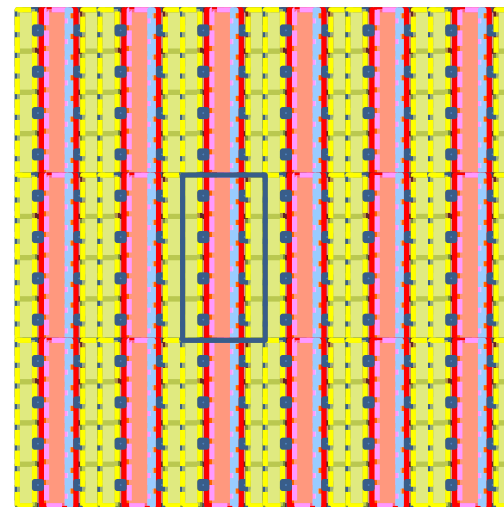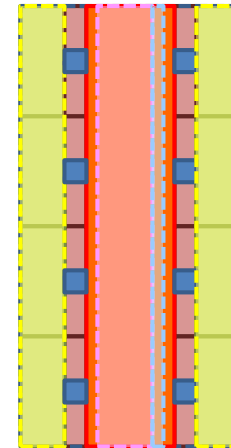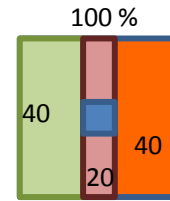
| Pixel pad | analog | Quite digital Config, etc. | Active digital | Power + Analog bias | Readout | Timing, control |

# GENERAL 4 X 4 ARCHITECTURE

Pixel array: ~128 Col.
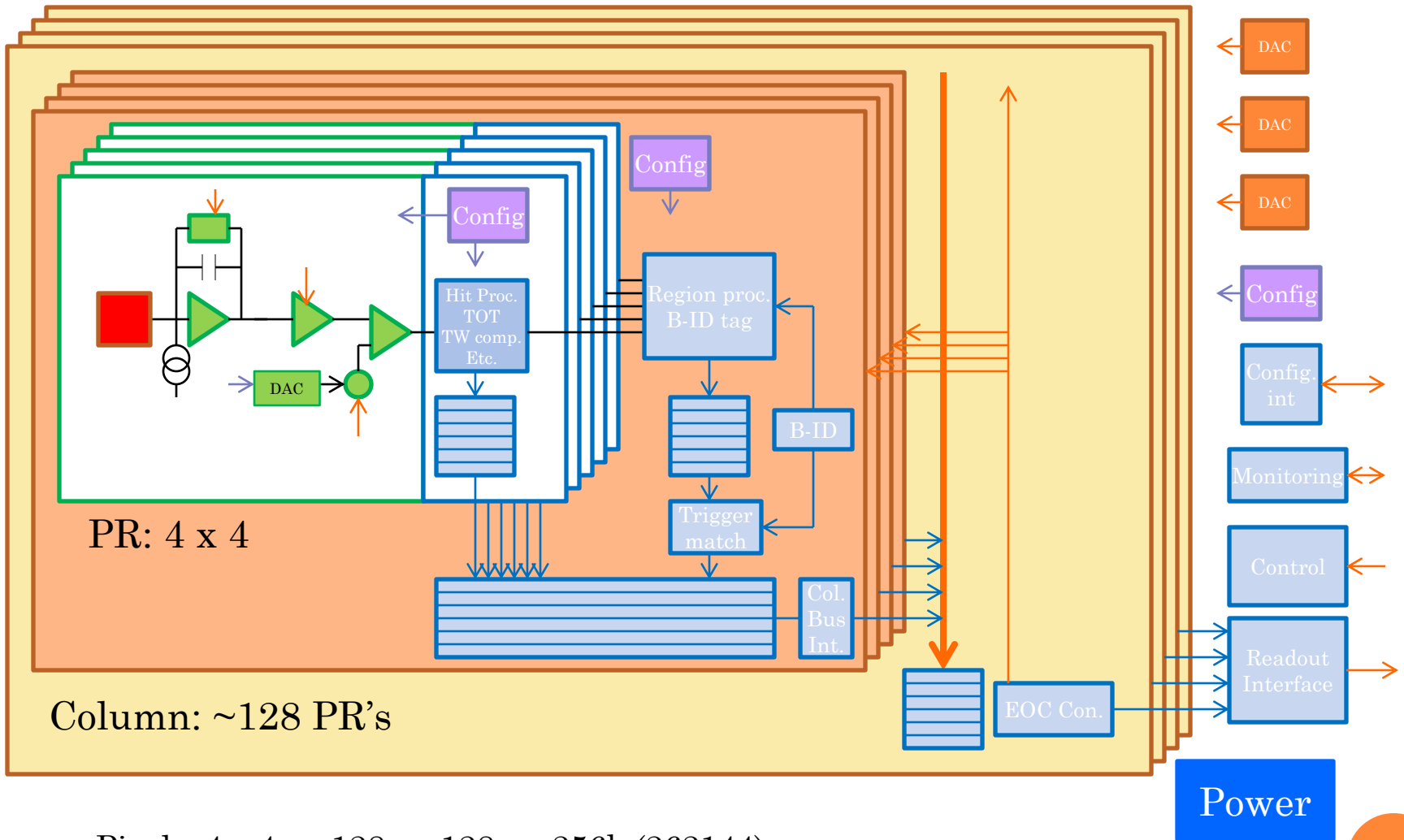


- Pixels: 4 x 4 x ~128 x ~128 = ~256k (262144)
- Obviously resembles FEI4
  - And any other data driven (HEP) chip/system: System on a chip

17

# BASIC CMS HL-LHC ASSUMPTIONS

- Cluster size: ~4 (worst case)
- Rate: Worst case HL-LHC
  - Layer 1: ~500MHz/cm$^2$ tracks -> ~2GHz/cm$^2$ hits
  - Layer2: **~½** of layer 1
  - Layer3: ~½ of layer 2 -> **~¼** of layer 1
  - Layer4: ~½ of layer 3 -> **~1/10** of layer 1 (50MHz/cm$^2$ tracks, 200MHz/cm$^2$ hits)
  - End-caps ?
- Pixel chip: ~4cm$^2$
- Pixel size: ~50x50um = 2500um$^2$ (or ~30umx75um)
- Pixel regions: 4 x 4
- Pixels per chip: ~256k (262144)
- Tracks/hits per chip per Bx:
  - Layer 1: 50 tracks per Bx (200hits/Bx)
  - Layer 4: 5 tracks per Bx (20hits/Bx)
- L1 Trigger rate: 100kHz (200kHz)

18

# READOUT

- (LP)GBT user bandwidth: 3.2 Gbits/s (6.4Gbits/s a possible future option)
  - **10 E-links @ 320Mbits/s**
  - 20 E-links @ 160Mbits/s
  - (40 E-links @ 80Mbits/s)
- Event header: 32 bit event header (B-ID , E-ID, ?)
- PR Binary: 16b hit map, 14b PR address.
  - Layer 1: ~275Mbits/s,        11.6 (10) pixel chips per LPGBT
  - Layer 4: ~30Mbits/s,         105 pixel chips per LPGBT
- PR Full TOT: 16x4b TOT, 14b PR address
  - Layer 1: ~710Mbits/s,        ~4.5 (5) pixel chips per LPGBT
  - Layer 4: ~74Mbits/s,         43 pixel chips per LPGBT
- PR Max 4 TOT: 16b hit map, 4 x 4b TOT, 14b PR address
  - Layer 1: ~420Mbits/s,        7.62 (5 or 10) pixel chips per LPGBT
  - Layer 4: ~45Mbits/s,         71 pixel chips per LPGBT
- Individual pixels: 4b TOT, 18b pixel address
  - Layer 1: ~470Mbits/s,        6.85 (5 or 10) pixel chips per LPGBT
  - Layer 4: ~50Mbits/s,         65 pixel chips per LPGBT
- **PR Variable TOT per PR: hits x (4bit pixel ID + 4bit TOT), 14b PR address (framing/encoding overhead to be added)**
  - **Layer 1: ~300Mbits/s,        10 pixel chips per LPGBT**
  - Layer 4: ~33Mbits/s,         97 pixel chips per LPGBT
- A pixel hybrid with 2 x 5 pixel ASIC's and a LPGBT could be a universal building block for all pixel layers
  - Data rate at the limit for layer 1 worst case:  option of 10G LPGBT  or 2 LPGBTs
  - 1 E-link at 320Mbits/s per pixel ASIC
  - 2nd. E-link at 320Mbits/s as reserve

# Pixel hybrid



320Mbits/s links

Pixel Hybrid

Opto/power hybrid for material and radiation reasons ?

Pixel ASIC

4cm

10cm

Power

LPGBT

~1m ?
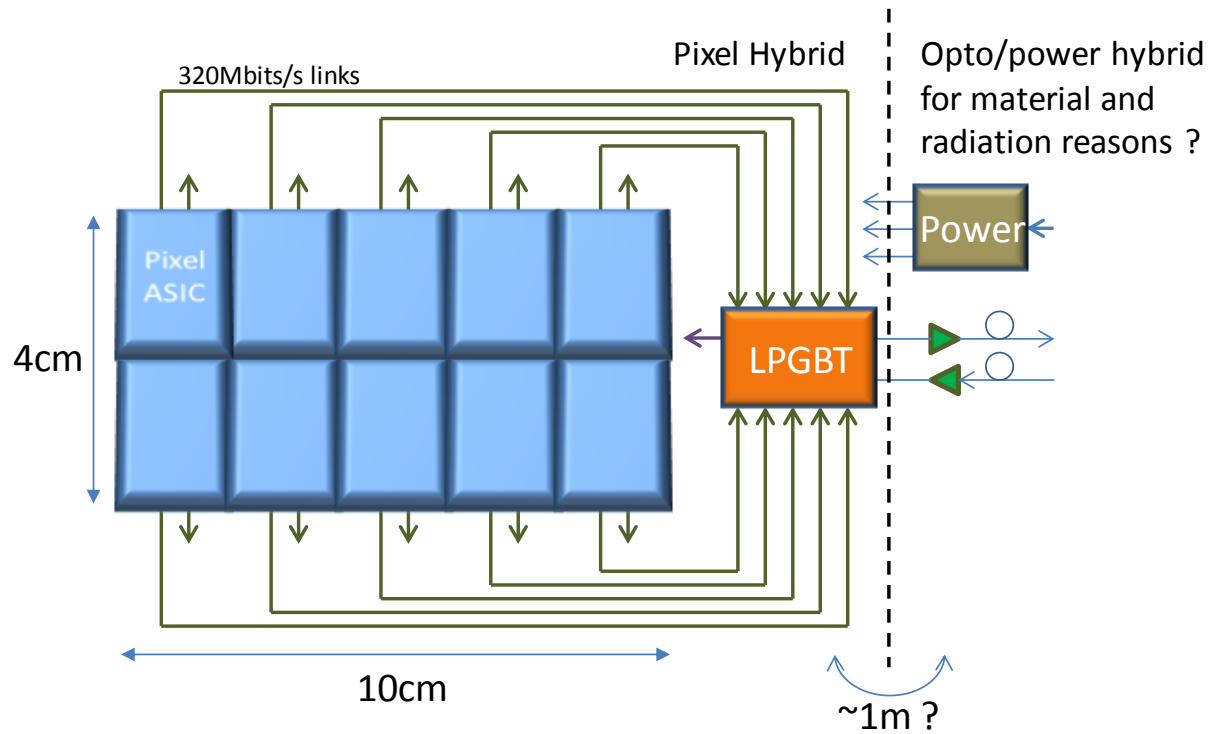
# SYNC PIXEL TRIGGER DATA FOR L0

- Fast coarse "strip" information
  - Fast OR along pixel region (or pixel) columns
- Tracks per bunch crossing:
  - Layer1: 50 per chip !
  - Layer4: 5 per chip
- Clustered "strips" along pixel columns
  - Pixel regions: 128b hit map per chip
    128b x 40MHz = **5Gbits/s per chip**
    - Useful if ~50 out of 128 bits set in layer1 ?
    - At this high rate no encoding can compress data (layer4: 5 out of 128. 5hits x 7b encoded = 35b)
  - Pixel: 512b hit map
    512b x 40MHz = **20Gbits/s per chip !.**
- Double pixel layer with Pt cut seems difficult
  - Easy to put logic within pixel chip but very hard to get data out and make a viable system

Fast Or

Clustering

128 pixel region columns
(512 pixel columns)

21
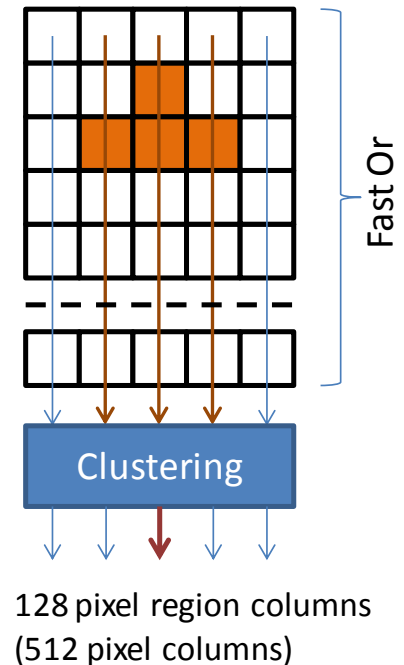
# PIXEL TRIGGER WITH ROI

- L0 trigger from calo and muon within ~3us.
- L0 rate: 1MHz ? (assuming x10 high rate than now)
- ROI percentage: 10 % ? At ASIC level (just a guess)
  ROI rate: 1MHz x 0.1: 100KHz per pixel ASIC.
- L1 latency: >3us ? (total L0 + L1 = ~6us),
  Seems critical as off-detector processing complicated.
- ROI data: Single pixel address per track: 9 + 9 bit.
    - Local clustering without considering TOT.
    - Simple local logic
- Pixel ROI data: Relative low data rate per pixel ASIC
    - Layer 1: 1MHz x 0.1 x (50 tracks x (9+9) + 16) = ~91Mbits/s
    - Layer 4: 1MHz x 0.1 x (50/10 tracks x (9+9) + 16) = ~11Mbits/s
- Buffering
    - L0 in pixel cell
    - L1 in pixel cell (or EOC?)
    - Shared (or separate ?) buffers
- Colum data busses: Shared or separate between ROI and readout ?
- Readout: Shared or separated ?.
    - Separated: Allocate bandwidth as required by two paths
    - 4 links with programmable speed ( 80/160/320 Mbits/s)
      and programmable use (L0 ROI data or L1 readout data)
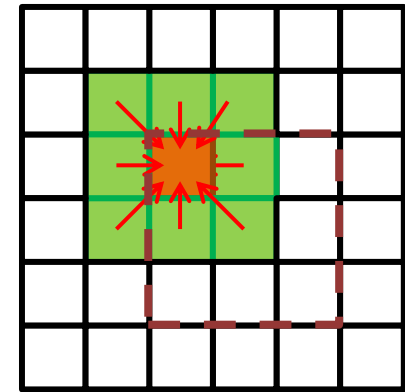
Local clustering
(across pixel regions)

22

# PIXEL TRIGGER AND READOUT DATA FLOW

**256k pixels**

Bx (40MHz)

Thres.

Fast Column or ?

(L0 trigger pixel data: sync column Or 128b @40MHz = 5.12Gbits/s)

B-ID

**128 columns**

**16k pixels regions**

~100b x 8 (16)

Bx clock, Reset, L0, L1, ROI, Etc.

Fast control

**1 E-link 320/160/80 Mbits/s**

L0 (1MHz) ~3.2 us

ROI request (10%) = 100kHz

Cluster extract ?

MUX

MUX

Config. Monitor

~100b x 8 (16)

L1 trigger ROI data: 90 -11 Mbits/s

>1Gbits/s

L1 (100kHz) >6.4 us

Switch

**4 E-links 320/160/80 Mbits/s**

MUX

MUX

>1Gbits/s

Readout data: 320 – 40 Mbits/s

23

# POWER – SERVICES – EQUIPMENT SAFETY

A. Guaranteed absolute maximum power consumption (over window of ~1sec)
- Considering worst case:
  - Possible wrong configuration data
  - Exceptionally high background and trigger rates for short time
- Unless counting on detector safety system to handle this without damage.

B. Some kind of average maximum power under normal working conditions.

○ This is what determines cooling and power infrastructure.
(with some safety factor).

There may be a significant difference between the two approaches for a chip that is highly data driven that will have effects on services and their related material.

# LOW POWER ANALOG

- Chip Global: "Non critical" as shared across ~256k pixels
  - DAC's, Biasing, ADC for monitoring
- Pixel Local: Critical, **~ ½ of total power ?**
  - Minimal power for required Noise and speed.
  - Threshold variation compensation with local DAC
  - Time walk compensation based on TOT
    - Time-walk may be the major determining factor for analog power
  - Discriminator with dynamic biasing (a la FEI4)
  - Initial gueestimate: 4uA x 1V x 256k / 4cm$^2$ = **~1/4 W/cm$^2$**
    - ATLAS FEI5 estimate: 5uA
    - LCD proto: 1.5uA (pre-amp) + 4uA (disc) + ? (local DAC)
    - **Possible to decrease this ?**
      (and keep timewalk requirements)

# LOW POWER DIGITAL

- Global
  - Clock distribution to array
    - Use both edges ?
    - Low voltage differential ? (but the clock receivers will take power)
    - Pixel regions gives less destinations
    - Hard to imagine that intelligent pixel regions can be made async when system/pixel sync vital for correct time tagging and trigger matching/association.
- General
  - High Vt libraries
  - Non minimum L library for leakage reduction (if appropriate and available)
  - Low Vdd for low speed logic (all except fast serial readout)
    - System aspects
    - Power conversion efficiency
  - Power optimized synthesis and P&R
  - Power optimized SEU protection (only critical parts)
    - Non clocked (async) configuration with SEU protect.
    - Do not do full TMR but only detect critical error states that may have long term effects (corrupted config. Pixel Region, EOC or chip out of system sync) and reset and resync ASAP.
      - Estimate rate and data loss from this.
  - Clock gating where ever possible
  - Power down:
    - Static: Non used features: Test, calibration, modes, TOT, trigger matching, buffers for low rate use
    - Dynamic: Not obvious for HL-LHC but to be studied
- EOC and pixel column bus: Not so critical as shared across column pixels
  - Power down if no triggered events waiting for readout: Estimate ratio for this and possible power savings.

# LOW POWER DIGITAL PIXEL REGIONS

- Pixel regions reduces
  - Required buffer depth ( factor >4)
  - Active latency units ( factor: 2-4 depending on cluster size)
  - Major part of local dynamic digital power in high rate triggered application.
- Clock gating of non active units:
  - TOT, latency units
- Async (self clocked): SEU correction of config.
- Dynamic power down ?: Estimate leakage power
  - Only power active latency units + 1 (ready for arrival of new hits)
- TOT (TOA) measurement:
  - Use of local (PR) delay chain on hit signal(s) to decrease dead time with low power (and possible option of ~ns time of arrival option)
  - TOA for background reduction ?(resolution ?, data reduction ?)

# STATISTICAL POWER ESTIMATOR

- Simple statistical power estimator to estimate/optimize at global level before detailed circuits available.
  - Few basic power numbers from detailed estimations/simulations
    - Static power: Analog, leakage
    - Energy per hit: analog, PR logic
    - Energy per trigger
    - Energy per triggered pixel data
    - Energy per "bit" read out
  - Basic statistical "monte carlo numbers"
    - Hit rates, clustering, TOT
    - Trigger rates
    - Triggered data to read out.

28

# WHAT IS NEEDED TO BUILD SUCH A PIXEL CHIP

- Access to technology:
  - MPW and Production
  - Radiation qualified
  - Tool kit
  - Libraries and (IP's)
- A design community (collaboration) to build it.
  ASIC centric (or bottom up) view:
  - ASIC designers (such an ASIC design is a **major** effort)
    - Specification, Architecture, Architecture simulation/verification, Design, Prototypes, Test, Radiation qualification, Test beams, Production, Production test
    - Analog
    - Digital
  - Electronics system designers
    - System integration, bump bonding, hybrid, powering, readout, control, test hardware.
  - Software: DAQ, controls, data analysis/verification
    - Lots of software require for test systems for partial prototypes, full chip prototypes, test beams,
  - Si pixel detector specialists
    - Definition of Si signal, radiation effects, clustering, , ,
    - Appropriate Si detector (multiple options ?)
  - Experiment specialists
    - Required resolution, Hit rates , Monte Carlo , ,
  - Mechanics
    - Support, cooling, services , ,

29

# ASIC DESIGN

- Digital
  - Definition and simulation of general architecture
    - HDL reference model and simulation/verification environment
    - Model for Monte Carlo simulations
  - SEU handling strategy
  - Pixel region optimization/synthesis/P&R/verification
  - End of column logic synthesis/P&R/verification
  - Control interface synthesis/P&R/verification
  - Readout interface synthesis/P&R/verification
- Analog
  - Pre-amp – shaper
  - Discriminator
  - Local correction DAC's
  - Global setting DAC's
  - Band-gap reference
  - Monitoring ADC, temperature sensor,
  - Power regulator / on-chip DC/DC
- Chip assembly from basic building blocks
- Design verification
- Chip testing, system testing
- Production preparation

# LOW POWER

- Low power optimization (obviously) critical
- Analog: ~1/2
  - Sacrifice some analog performance
  - Recover on digital when ever possible
    - Local threshold adjust
    - Time walk compensation
  - Binary/TOT/ADC
- Digital: ~1/2 (Can easily be more if not highly optimized)
  - Dynamic
  - Static (Increasing in 65nm)
  - Architecture ( Pixel regions, etc.)
  - Extensive clock gating (or async)
    - (local power down)
  - Clock distribution to full array to be highly optimized.
    - Alternative schemes to be evaluated
  - Use of low power libraries and synthesis
  - Decreased supply voltage for slow parts (most parts slow)
    - Careful with introducing additional power supply voltages as it may complicate the system significantly

# ASIC DESIGN

- THIS IS A MAJOR JOB THAT WILL REQUIRE CLOSE COLLABORATION BETWEEN CHIP DESIGNERS IN MULTIPLE INSTITUTES
  - Guesstimate: ~4 **full time experienced** chip designers for~ 4 years (for the ASIC design part)
  - Profiting from other developments in 65nm: Medipix X, LCD pix, LPGBT, ATLAS pixels, AIDA IP blocks, ,

- Physicist/electronics engineers for
    - Define physics performance parameters
    - Verify physics performance (Monte Carlo, etc)
    - Si pixel detector and bump bonding
    - Test systems: Hardware, software
    - Test beams and analysis

# DIGITAL DESIGN METHODOLOGY

- Top down architecture and bottom up critical circuits.
- Top down architecture
  - High level model that can be incrementally refined
    - Appropriate to try different architectures (for power and area)
    - Same tool (set) from high level to final implementation
      - From Monte Carlo to detailed area and power ?
  - Proposal
    - System Verilog/VHDL at transaction level and RTL level
    - (C++ for plug-in in monte carlo simulations)
- Bottom up
  - Mixed signal Spice/Verilog

# ARCHITECTURE/DESIGN DEVELOPMENT/VERIFICATION TOOLS

- Appropriate high level (global architecture) and low level (gate and analog) optimization/design/simulation environment vital for a design of this complexity.
  - One tool(set) must cover whole range
- High level: System C, C++,
  - Good for high level architecture optimization
    - Very efficient for compute heavy applications (e.g. DSP)
  - High level synthesis and links to low level not sufficiently good for a design that must be heavily optimized at the bit level (256k pixels !)
- Mid level: Register Transfer Level (RTL)
  - Verilog: Popular among ASIC designers in industry
    - Very good links to the ASIC design tools
    - **System Verilog: Additional features**
      - High level transaction based simulation for architecture optimization.
      - Built in verification features
    - Verilog-AMS: Mixed mode analog and digital simulations
  - VHDL: Popular among FPGA/board designers and in universities
    - Links with ASIC design tools and high level modeling ?.
    - Can be used together with system Verilog (but does not make much sense)
- Low level: Synthesis, Gate level, Layout, SPICE, P&R, DRC , ,
  - Common design database if many blocks developed simultaneously in different sites.

# ARCHITECTURE DETAILS (THIS IS WHERE THE DEVIL(S) ARE)

- Pixel & EOC & Readout buffering
- Pixel column data bus (Classical busses not appropriate in 65nm)
- EOC data merging
- Readout, Control, Monitoring interfaces.
- Data merging/control among multiple pixel chips.
  - Use (LP)GBT directly for this
    - GBT for fast control and data merging
    - GBT-SCA for slow control and monitoring ?
  - Separate module controller/ data merger
    - Build this function in to pixel chips
- Assuring that chip/systems remains operational and synchronized no matter what:
  - Buffer overflows
    - Large correlated events
    - Sequence of events.
    - Trigger sequences (and defined system limitations)
    - Etc.
  - Redundancy
    - SEU !
    - Chip yield (very large chip)
    - Readout/control/monitoring links
- Test and calibration features.
  - Design verification and qualification
  - Production testing
  - In-situ testing/verification
- Monitoring
- ETC.

# STARTING THE ASIC WORK

- Get together CMS groups and ASIC engineers interested to work together on such an ASIC design.
  - ASIC design long, complicated and expensive so the bottom-up work must start very soon to have a 65nm pixel ASIC available in ~4 years to enable a new CMS pixel detector to be designed, built, and tested for installation in ~2018 – 2020 (Phase 2).
- Identify groups interested in 65nm pixel ASIC
  - Medipix, LCD (CLIC), ATLAS pixel, ?
- Get additional manpower resources from Marie-curie training program (or other EU program)
  - A combined proposal with Medipix/LCDpix would have all the right ingredients for EU success !.
    - Critical to indentify European companies to "participate"
  - Efficient synergy/sharing with other 65nm projects vital.
  - Multisite
  - Next bid ~Nov. 2012.
    2013: Most likely no call
    2014 - : Framework 8 program
- ASIC costs: Swiss franc = ~ $
  - Small chip prototypes 2013-2014: 200 – 300k
  - Full chip prototype(s) 2014-15: 1 (2) x ~1M
  - Production 2016-2017: ~200k (~1 m$^2$ with 50% yield, 12" wafer ~6k) (bump bonding and detector will be dominating production costs)

  This is obviously only one (but key) part of a pixel detector.

# DESIGN CONTRIBUTIONS/BLOCKS
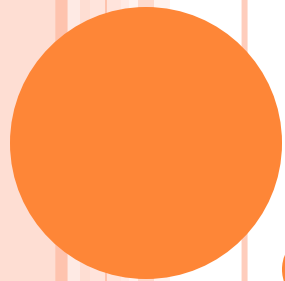
- Analog (rather independent blocks)
    - Pre-amp and shaper
    - Discriminator
    - Local adjust DAC (4-6bit)
    - Global DAC's (10b)
    - Bandgap reference
    - Monitoring ADC (10 – 12b) + sensors (power supplies, temperature, leakage current, DAC read back, etc.)
    - PLL
    - General approach to minimize digital -> analog noise
- Digital (highly interdependent – hard to split)
    - Global: architecture and verification test bench
        - Pixel cell
        - EOC
        - SEU protection
    - Readout interface
    - Control and Config
    - Testability
    - Special SEU immune cell (e.g. DICE)
    - RTL – local Synthesis
- Global (highly interdependent – hard to split)
    - Full chip simulation/verification (with both analog and digital)
    - Global synthesis with global signals and busses
    - Place and route: analog, digital, clock distribution, power distribution, etc.
    - Design verification: Simulation with parasitics, LVS, DRC, Power distribution

# SCHEDULE AND CHIP SUBMISSIONS

- MPW1: First basic analog building blocks
  - 2013/14: ~50k
- MPW2: Complete analog blocks
  - 2014/15: 50k
- MPW3: Full pixel cells, pixel regions and folded column with basic End of column
  - 2015: 100 – 200k
- ENG1: Full design submission
  - 2016: 1M
- (ENG2): Pray that we do not need this
- Production
  - 2017: 250k

# SUMMARY

- 65nm CMOS technology very attractive/appropriate for long term (Phase 2) pixel developments.
  - Density, performance, low power, radiation tolerance
  - Affordable MPW runs
  - Not relying on risky exotic technologies
  - (Expensive NRE for full final chip)
- Performance and density enables high resolution, high rate and flexible pixel ASIC
- The use of local pixel regions appears highly advantageous for a HL-LHC pixel detector
- An ASIC design community will need to get started within ~1 year to enable a phase2 CMS pixel detector upgrade for 2018-2020.

39

# BACKUP SLIDES

40

# Div information on 65nm and pixels

- TWEPP
  - 65nm radiation tolerance:
    - https://indico.cern.ch/contributionDisplay.py?contribId=4&sessionId=44&confId=120853
  - ATLAS paper in TWEPP2012 to come
- NIMA:
  - **Front-end electronics in a 65 nm CMOS process for high density readout of pixel sensors.** Volume 650, Issue 1, 11 September 2011, Pages 163–168
    - http://pdn.sciencedirect.com/science?_ob=MiamiImageURL&_cid=271580&_user=107896&_pii=S0168900210026264&_check=y&_origin=article&_zone=toolbar&_coverDate=11-Sep-2011&view=c&originContentFamily=serial&wchp=dGLbVlV-zSkWz&md5=3d6fc718e8f45e8893fbf2f3ed396a48/1-s2.0-S0168900210026264-main.pdf
- LCD
  - 65nm pixel:
    - http://indico.cern.ch/conferenceDisplay.py?confId=184553
- CERN ESE seminars:
  - Designing with 65nm (to come June 5)
    - https://indico.cern.ch/conferenceDisplay.py?confId=173640
  - Pixel detector readout architectures:
    - https://indico.cern.ch/conferenceDisplay.py?confId=173056
  - FEI4:
    - https://indico.cern.ch/conferenceDisplay.py?confId=121650
- CMS meetings
  - FEI4:
    - https://indico.cern.ch/conferenceDisplay.py?confId=155512
- ATLAS presentations
  - ATLAS upgrade week Stanford March 2012.

41

# 130nm

- Advantages:
  - Well know technology in HEP
  - Available building blocks
  - "Low" NRE costs (~1/2 of 65nm)
  - Buy the FEI4
    - Unlikely that a CMS design would be significantly different/better that FEI4
- Disadvantages:
  - Density (~1/4 of 65nm)
  - Digital power consumption (~2x compared to 65nm)
  - Long term availability