Experience with FE-I4 chip

Description of what i learnt about this chip

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FE-I4: many challenges

The FE-I4, designed for the IBL, was a HUGE!!! effort due to many different issues:

- "New" technology (IBM 0.13 μm), at least for the time being...
  - Open Access/CDBA (new or more stable, and reliable, version of Cadence?)
  - New Design Kit (T3 isolation was introduce during the design cycle)
  - Analog/Digital isolation
  - Lack of experience
- Huge size of the chip (≈ 2x2 cm)
  - Needed special IBM approval with additional checks
  - Power/clock distribution across the chip (Pads only on one side of the chip)
- New digital architecture
  - Full custom/Std cells discussion, for the digital logic inside the Pixel region
  - Redundancy, SEU, Testability, Yield considerations during design development
  - Timing verification of the whole chip (external company involved)
- Worldwide distributed group of people working on the chip
  - LBNL, Bonn, Nikhef, Genova, Marseille, (≈10 people working together)
  - Cliosoft SoC (CVS like, but tools aware) software to overcome this issue

FE-I4: technology issues

"New" technology (IBM 0.13 μm), at least for the time being...

- We chose to go for the newer, even if less supported, software/Design kit.

  Cadence 6.x (OA version) and T3 support in the Design Kit.

  This has proven to be the good choice in the long term!
- Analog/Digital isolation solved using T3.

  All digital blocks were put inside T3

  Separate power supplies for periphery/digital/analog blocks

Huge size of the chip (≈ 2x2 cm):

- Power distribution:

  Shielding and power using last metal layers imply low resistivity and

  less voltage drop allowing good distribution (<10 mV drop) over two centimeters!
- Clock distribution:

  Try to avoid high instant power consumption on all transistors switching at the

  same time (could be as high as many amps of current) avoiding too much skew.

  Added a clock delay circuitry to distribute clock rising edges over time

FE-I4: Regional architecture

The FE-I4 has been built with a new architecture:

- 80 x 336 pixels (50 x 250 μm^2) organized in double columns
- Chips size is almost 2 x 2 cm^2All the digital control blocks are
- All pixels are arranged in 2 x 2 pixel regions
- Analog signals sampled with the 40 MHz system clk which is distributed along the double columns
- Hits (with a 4 bit ToT) sampled locally inside the pixel region
- To reduce Time Walk in each region only signals crossing a user selectable digital threshold are used for timing whilst small signals are associated to big ones inside the digital region
- 1 DC has ≈ 800 transistors (200 memory cells)

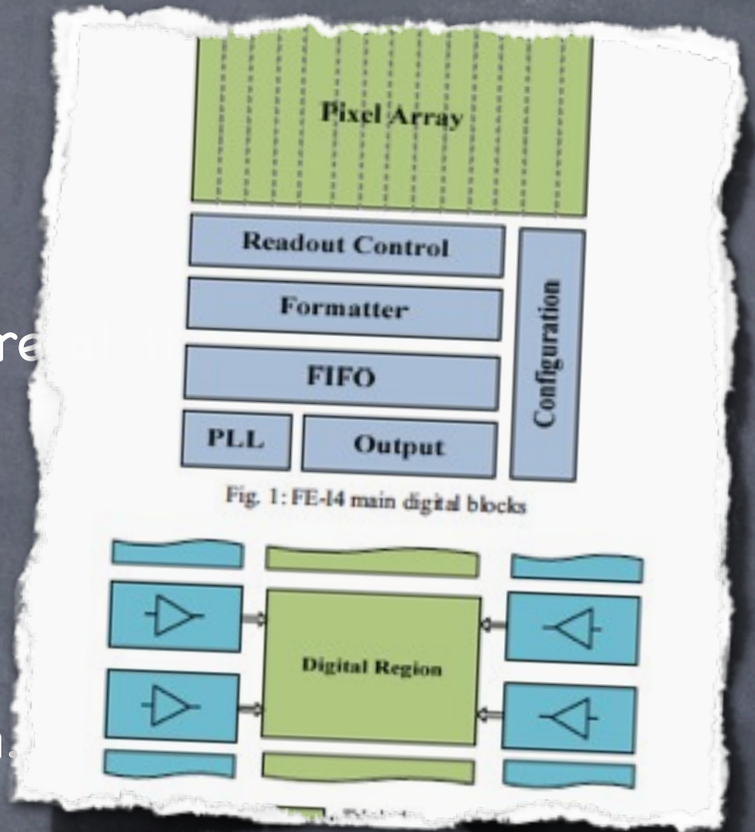
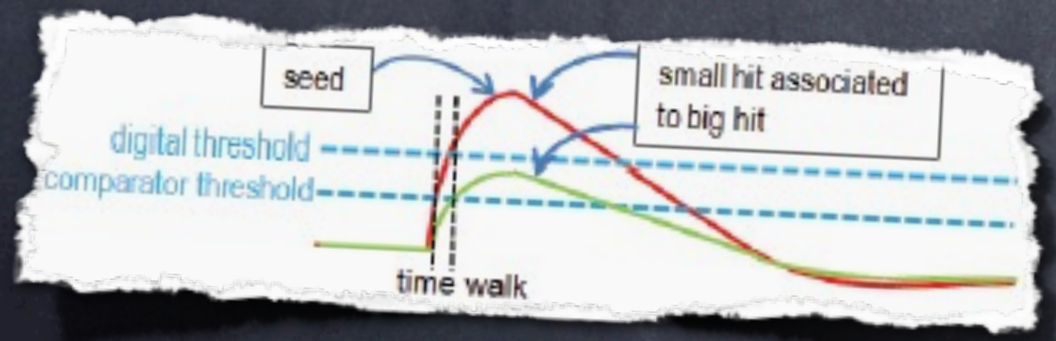
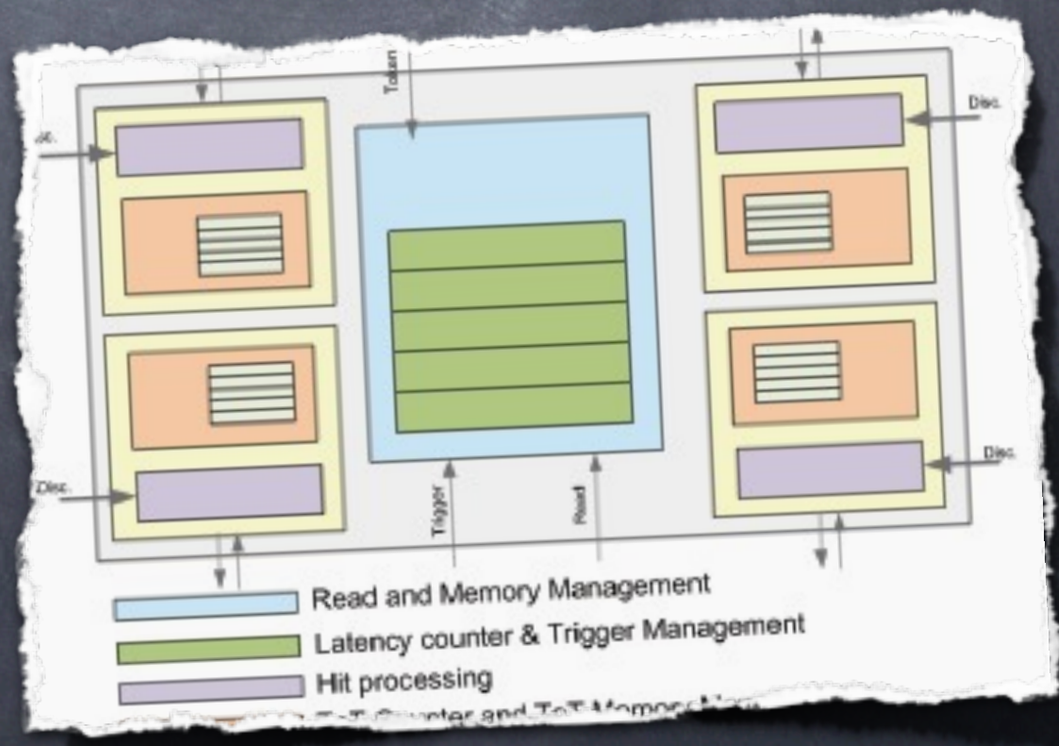


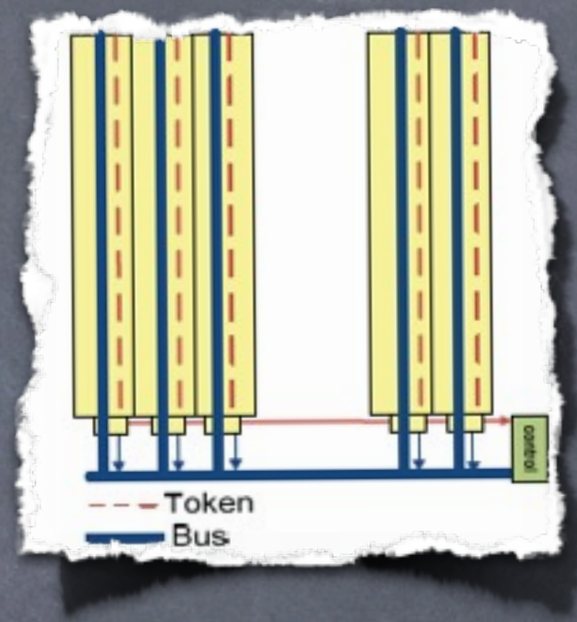
Fig. 1: FE-I4 main digital blocks



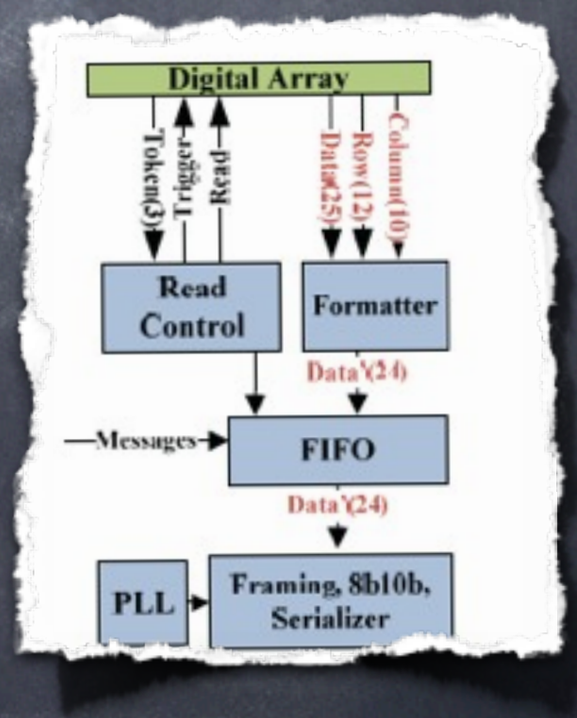


FE-I4: Regional architecture

- Data readout is triggered
- Data which is not triggered is deleted inside the digital region without transferring it to the periphery, avoiding bus congestion
- Simple EoC control logic, based on a simple token mechanism
- The data bus, inside each DC, consists of 25 bits (16 ToT + 4 neighbor bits + 5 Hamming error protection codes) implemented with OR gates.



- Error correction techniques on the data bus are used to reduce single points of failure
- The 11 bit address bus (8 address + 4 protection bits) is organized as a thermal gray encoder to minimize area and maximize yield
- An on chip PLL allows to format and read out data at 160 MHz
- The derandomizing FIFO is used to sync the two clock domains
- The Output Encoder provides data framing and 8b10b data encoding for improved signal transmission
- This architecture has been proven to scale very well with data rate and with chip area, even for sLHC harsh conditions.



FE-I4: collaborative model

Worldwide distributed group (≈10) of people working together on the chip:

- many people, distributed in different institutes, distributed worldwide...
  - Real challenge being able to manage a distributed design environment with different tools, databases of the design, different licensing issues (some groups have access to full GDS, some only to abstracts), in some places more than one person works on the same design.
- Found a really good solution:
  Cliosoft SoS (www.cliosoft.com/products/sos.shtml)
  - Powerful yet easy to use and setup tool
  - It is a CVS like tool that is built around CAE tools -> therefore you can share ALL design information of the project in an easy way
  - Server/Client with local caches accessible by local users that is very flexible and reliable
    Many Gbyte of data always transparently in sync
  - Relatively cheap solution (≈1000 Euro/year/person)

Conclusions

It works!!!

Yield ≈ 75% (so far)

similarities with this project

- New technology.
- Highly distributed design environment
- Lot of digital circuitry embedded with "some" analog blocks